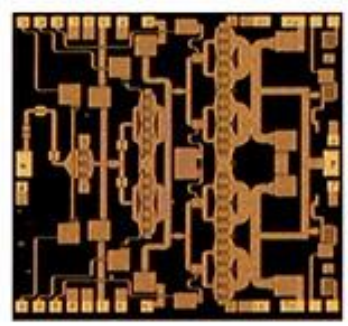
TGA4548

17 - 20 GHz 10 W GaN Power Amplifier



2.95 x 2.80 x .10 mm Die Size

Product Overview

Qorvo's TGA4548 is a high frequency, high power MMIC amplifier fabricated on Qorvo's production 0.15um GaN on SiC process (QGaN15). The TGA4548 operates from 17 – 20 GHz and typically provides 10 W saturated output power with power-added efficiency of 30% and large-signal gain of 22 dB. This combination of high frequency performance provides the flexibility designers are looking for to improve system performance while reducing size and cost. The TGA4548 also has an integrated power detector to support system diagnostics and other needs.

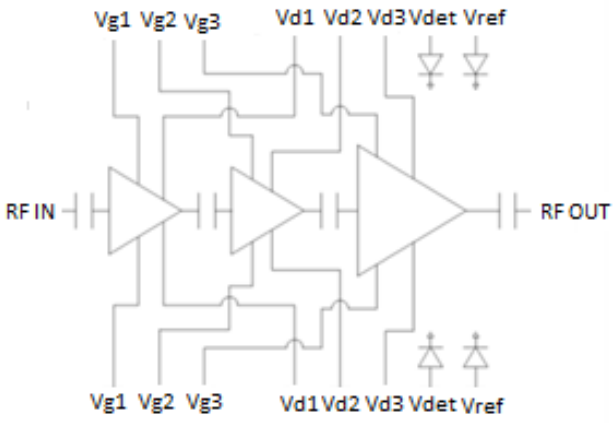
The TGA4548 is matched to 50Ω with integrated DC blocking capacitors on both RF I/O ports simplifying system integration. The frequency coverage and operational flexibility allows it support satellite communication as well as point to point data links.

The TGA4548 is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Functional Block Diagram



Key Features

- Frequency Range: 17 – 20 GHz
- Power: 40 dBm Psat
- Small Signal Gain: 27 dB
- Large Signal Gain: 22 dB
- Integrated Power Detector
- PAE: 30% at P_{IN} = 12 dBm
- Bias: VD1 = VD2 = VD3 = +28 V, ID1 + ID2 + ID3 = 300 mA
- Chip Dimensions: 2.95 x 2.80 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Point-to-Point Radio
- Satellite Communications

Ordering Information

Part No.	ECCN	Description
TGA4548	3A001.b.2.c	Waffle tray with 25 pcs
TGA4548S2		Sample waffle tray with 2 pcs
TGA4548EVB		Evaluation board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-8 to 0 V
RF Input Power, CW, 50 Ω, T=25 °C	26 dBm
Dissipated Power (P_{DISS}), CW, 85°C	43 W
Storage Temperature	−55 to +150 °C
Mounting Temperature (30 seconds)	320 °C
Channel Temperature (T_{CH})	275 °C
Drain Current (I_{D1}), Top or Bottom	500 mA
Drain Current (I_{D2}), Top or Bottom	500 mA
Drain Current (I_{D3}), Top and Bottom	2 A
Forward Gate Current (I_{G1}), Top or Bottom	3 mA
Forward Gate Current (I_{G2}), Top or Bottom	12 mA
Forward Gate Current (I_{G3}), Top and Bottom	48 mA
Reference Power Detect (I_{ref})	4 mA
Power Detect Diode (I_{det})	4 mA

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		+28		V
Operating Temp. Range	−40	+25	+85	°C
I_{DQ}		300		mA
V_G		-2.6		V
I_D drive (at +38dBm Pout)		930		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

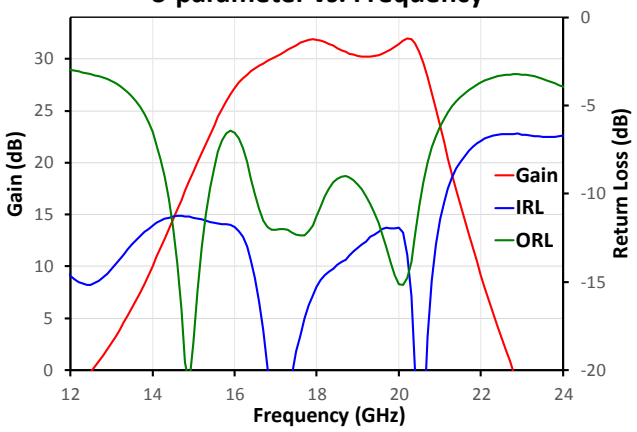
Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		17		20	GHz
Small Signal Gain			27		dB
Input Return Loss			15		dB
Output Return Loss			12		dB
Output Power at Saturation, Psat			40		dBm
Power Added Efficiency, PAE			30		%
Third Order Intermodulation, IM3	Pout = +34 dBm/tone		-25		dBc
Gain Temperature Coefficient	T_{diff} = (85 – (-40)) °C		-0.061		dB/°C
Power Temperature Coefficient	T_{diff} = (85 – (-40)) °C, P_{in} = +5 dBm		-0.044		dBm/°C

Notes:
1. Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2=ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z0 = 50 Ω

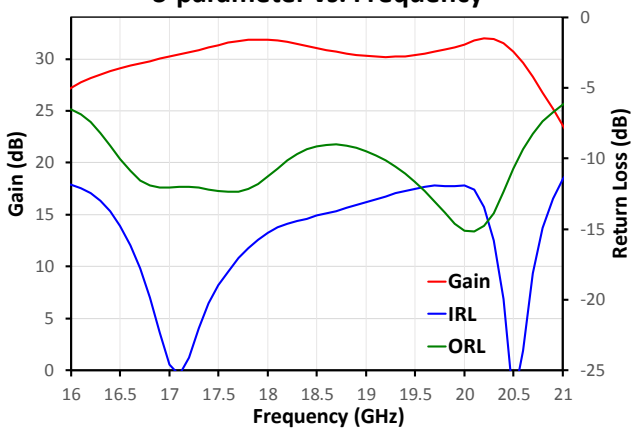
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

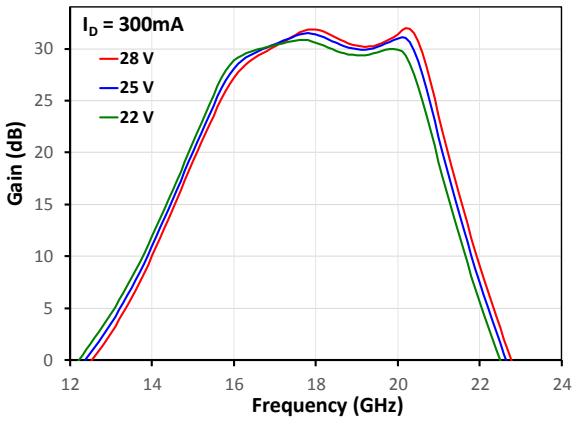
S-parameter vs. Frequency



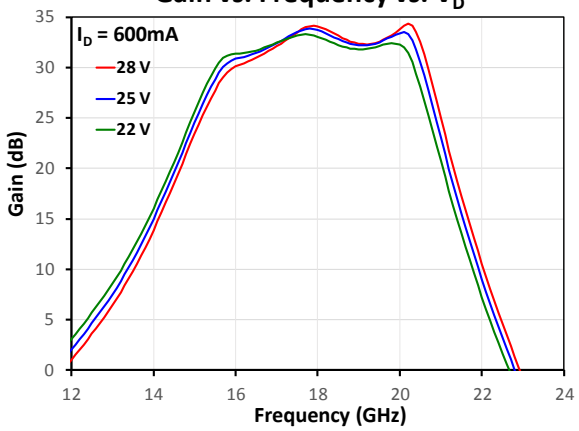
S-parameter vs. Frequency



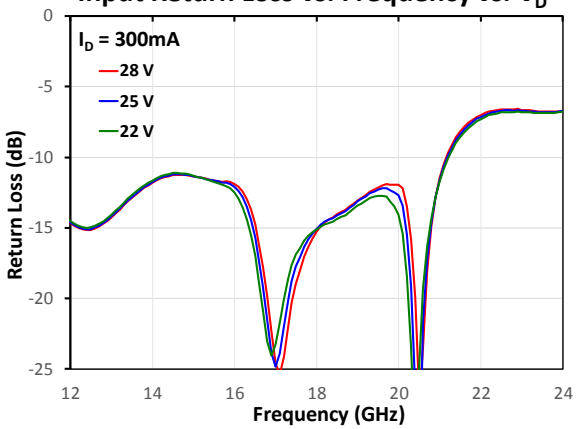
Gain vs. Frequency vs. V_D



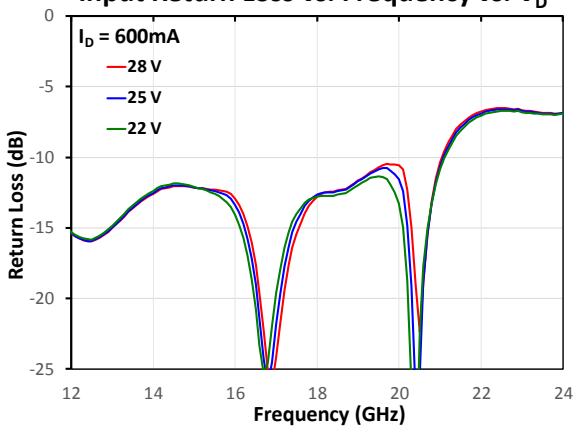
Gain vs. Frequency vs. V_D



Input Return Loss vs. Frequency vs. V_D



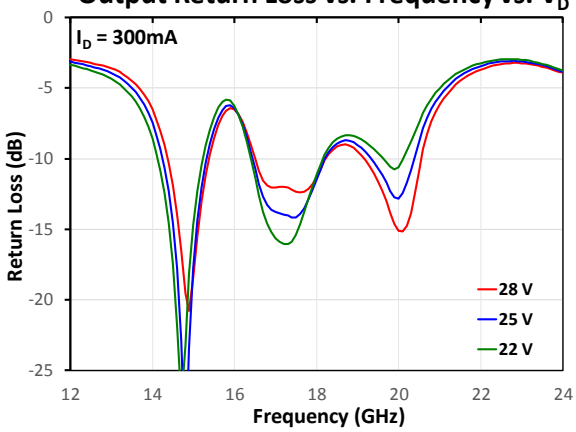
Input Return Loss vs. Frequency vs. V_D



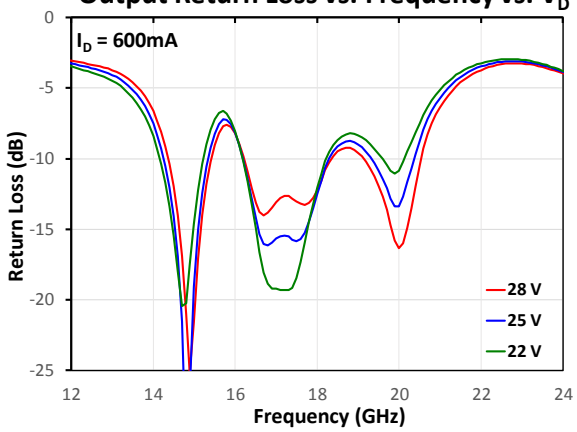
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

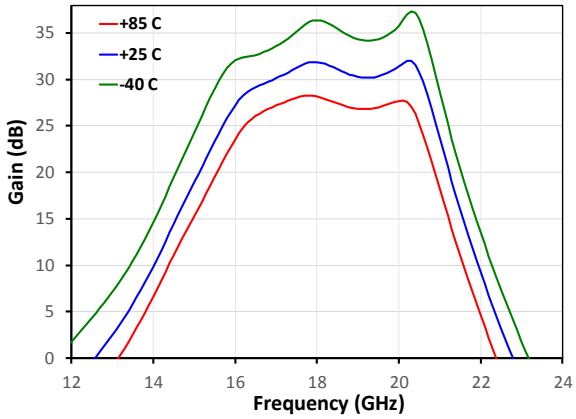
Output Return Loss vs. Frequency vs. V_D



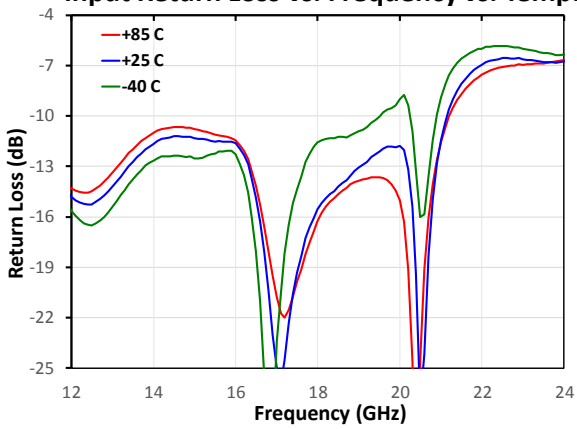
Output Return Loss vs. Frequency vs. V_D



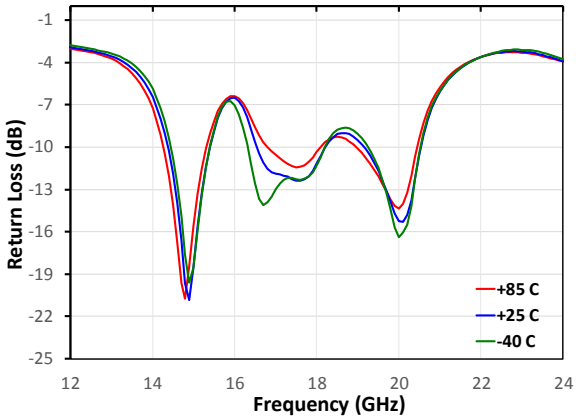
Gain vs. Frequency vs. Temp.



Input Return Loss vs. Frequency vs. Temp.



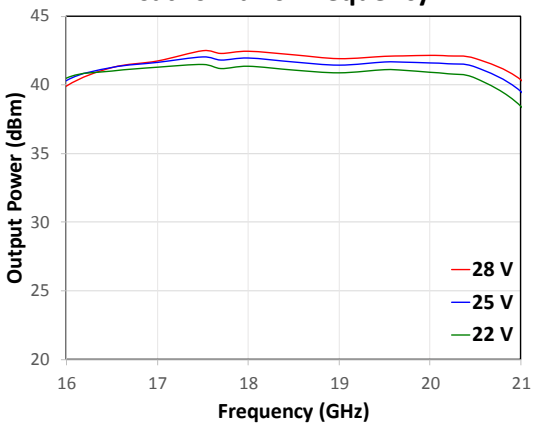
Output Return Loss vs. Frequency vs. Temp.



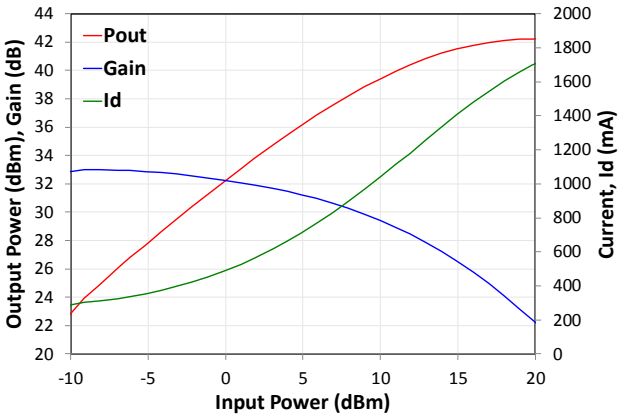
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

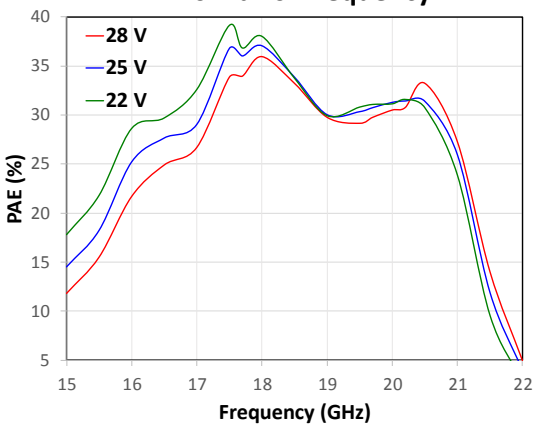
Psat vs. Vd vs. Frequency



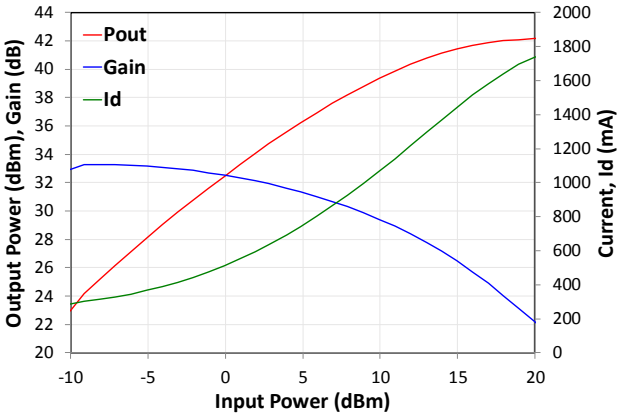
Pout, Gain, Id vs. Pin @ 17.7 GHz



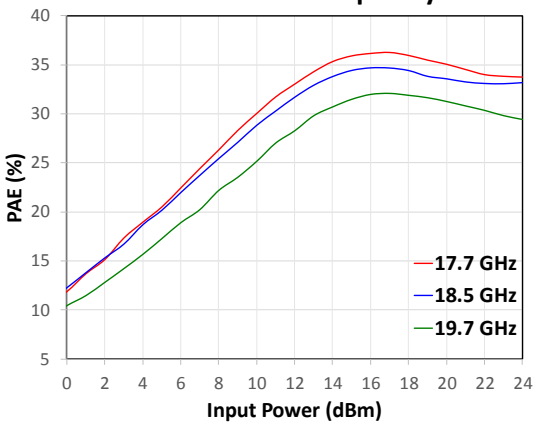
PAE vs. Vd vs. Frequency



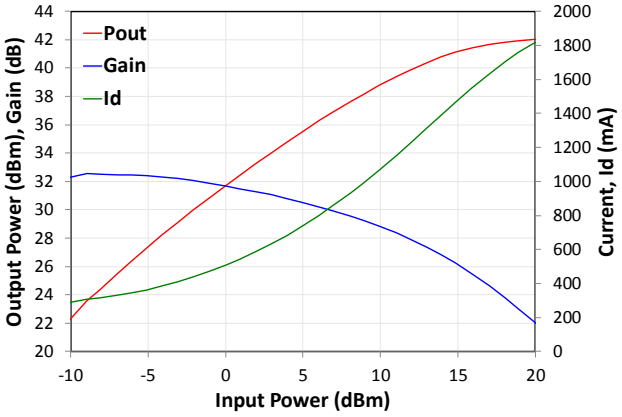
Pout, Gain, Id vs. Pin @ 18.5 GHz



PAE vs. Pin vs. Frequency



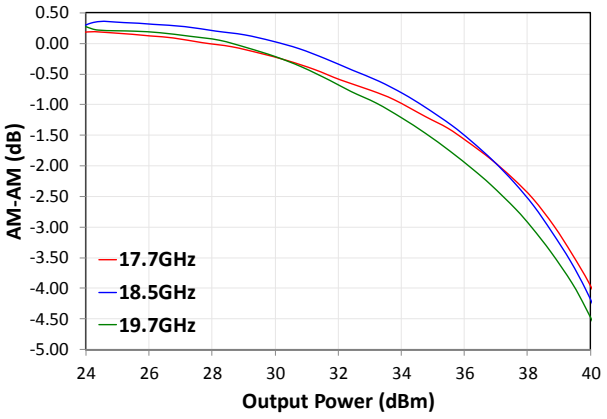
Pout, Gain, Id vs. Pin @ 19.7 GHz



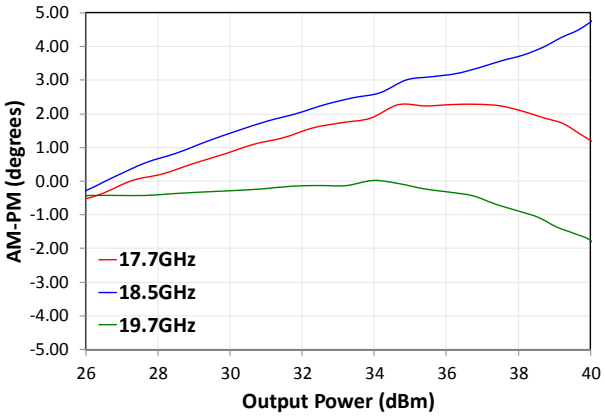
Performance Plots

Test conditions unless otherwise noted: VD1=VD2=VD3=28V, ID1+ID2+ID3=300mA, VG1=VG2=VG3=-2.6V typical, Temp = +25 °C, Z_0 = 50 Ω

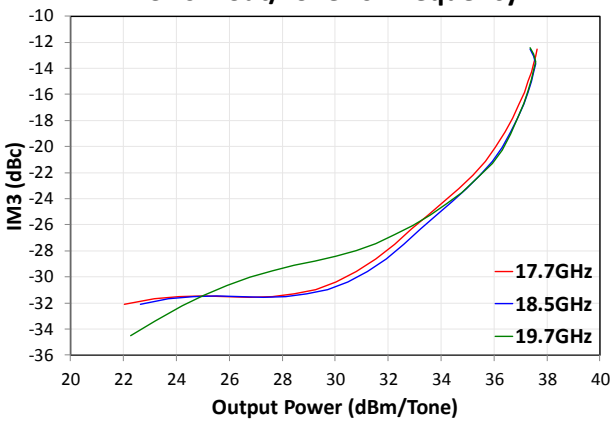
AM-AM vs. Pout vs. Frequency



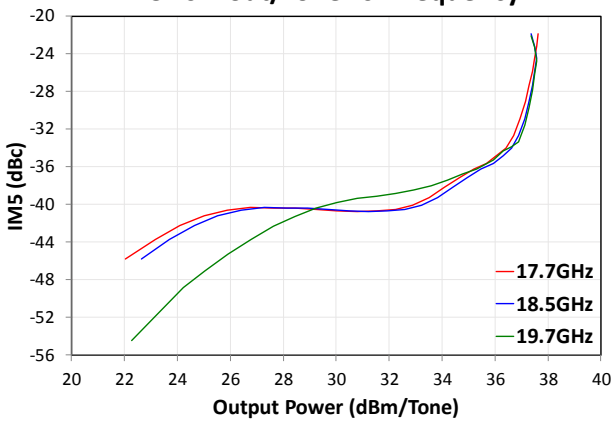
AM-PM vs. Pout vs. Frequency



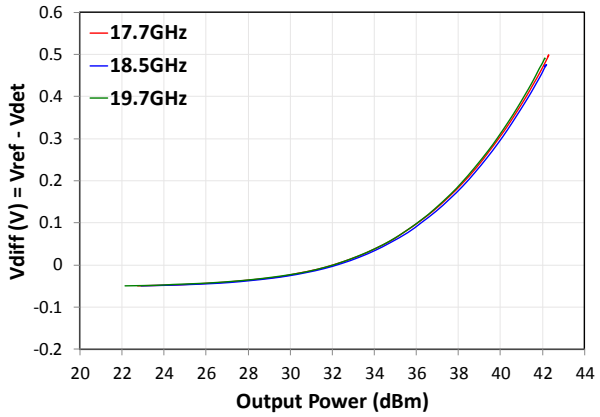
IM3 vs. Pout/Tone vs. Frequency



IM5 vs. Pout/Tone vs. Frequency



Power Detector vs. Pout vs. Frequency



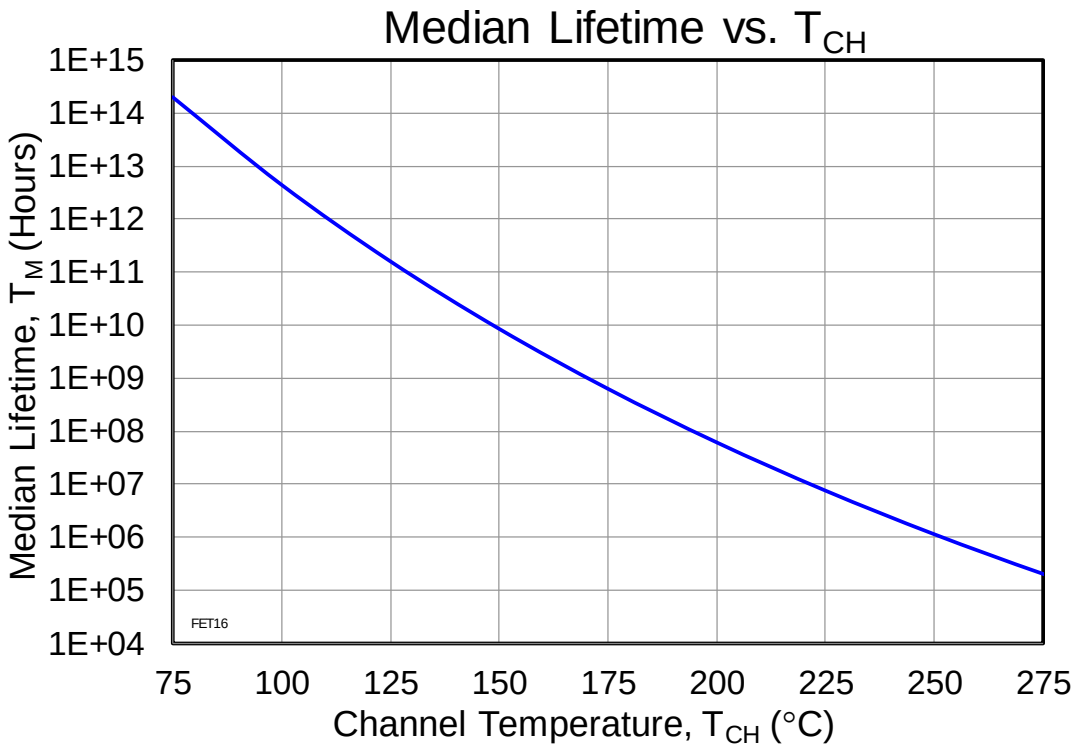
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, V_D = +28 V, I_D = 300 mA, P_{OUT} = 25 dBm, P_{DISS} = 8.4 W	3.57	ºC/W
Channel Temperature, T_{CH} (Under RF)		115	°C
Median Lifetime (T_M)		5.7×10^{11}	Hrs
Thermal Resistance (θ_{JC}) (1)	CW $T_{baseplate}$ = +85 °C, V_D = +28 V, I_D = 1700 mA, P_{OUT} = 40 dBm, P_{DISS} = 37.6 W	4.17	ºC/W
Channel Temperature, T_{CH} (Under RF)		240	°C
Median Lifetime (T_M)		2.4×10^{6}	Hrs

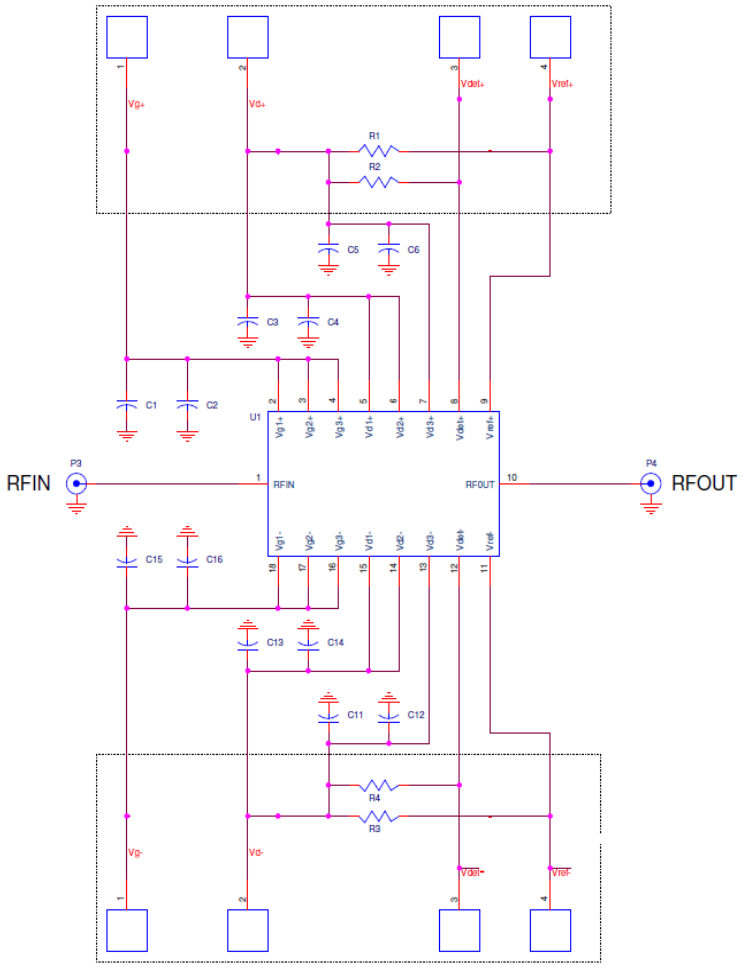
Notes:
1. Channel operating temperature will directly affect the device median lifetime (Tm). For maximum life, it is recommended that the channel temperatures be maintained at the lowest possible levels.

Median Lifetime

Test Conditions: V_D = +28 V; Failure Criteria is 10% reduction in I_{D_MAX}



Application Circuit



Notes:

1. VG1, VG2, and VG3 can be biased from either side, and the non-biased side can be left open. VD1, VD2, and VD3 must be biased from both sides.

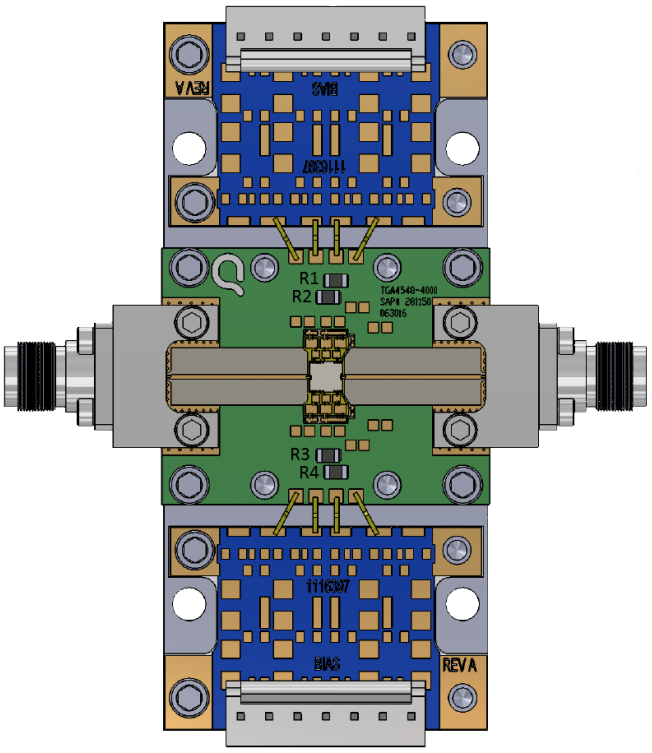
Bias Up Procedure

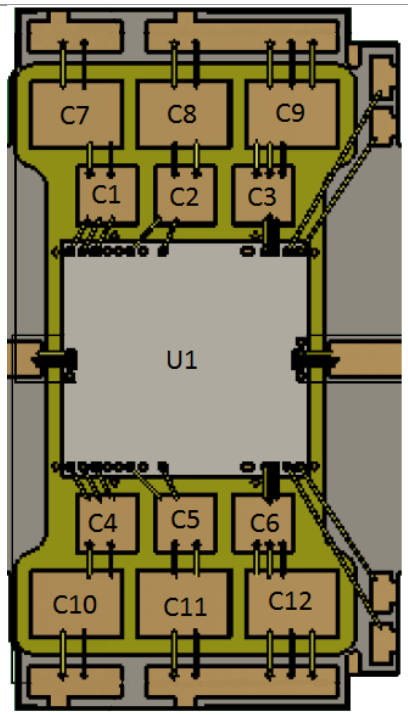
1. Set I_D limit to 3000 mA, I_G limit to 20 mA
2. Apply −5 V to V_G
3. Apply +28 V to V_D; ensure I_{DQ} is approx. 0 mA
4. Adjust V_G until I_{DQ} = 300 mA (V_G ~ −2.3 V Typ.).
5. Turn on RF supply

Bias Down Procedure

1. Turn off RF supply
2. Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly





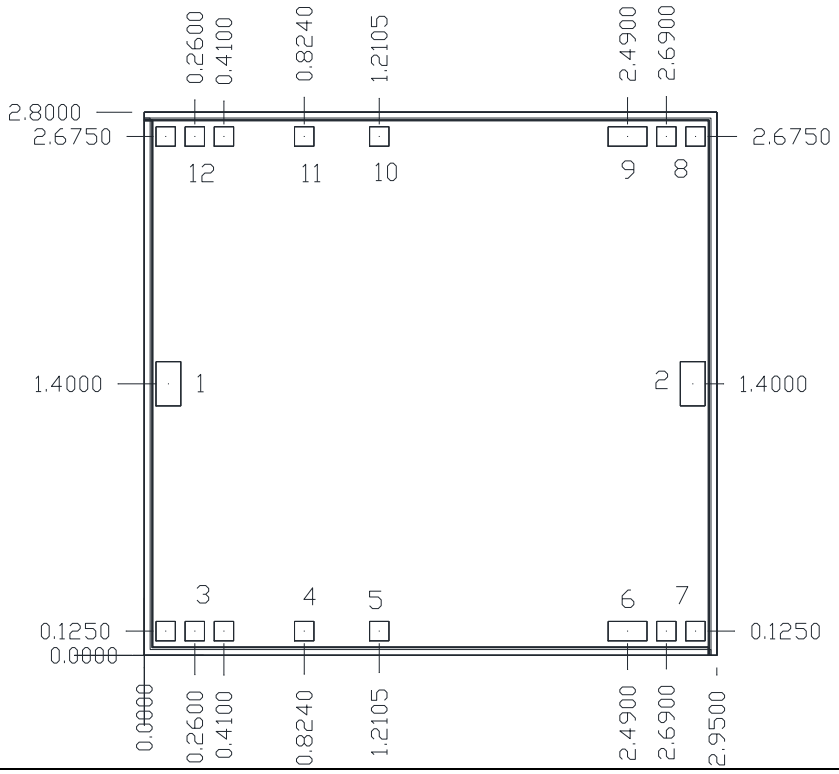
Note: PCB is a multilayer

1. All 4 metal thicknesses are 0.5 oz
2. Upper core 1 is Rogers 4003C
3. Pre-Preg is an epoxy coated glass fabric

Bill of Material – TGA4548 Evaluation board

Reference Des.	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board	Qorvo	
U1	n/a	17 – 20 GHz Power Amplifier	Qorvo	TGA4548
C1-C6	100pF	Cap, 100pF	various	
C7-C12	0.01uF	Cap, 0.01uF	various	
R1-R4	20kΩ	Res 20K OHM 1/8W +/-1% 0805 NON-ROHS	various	

Mechanical Information



Notes:
Units: millimeters
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF IN	0.100 x 0.200	RF Input; matched to 50 Ω, DC blocked
3, 12	V_{G123}	0.100 x 0.100	Gate voltage for stage 1, 2, & 3, bias network is required; see Application Circuit on page 8 as an example.
4, 11	V_{D1}	0.100 x 0.100	Drain voltage for stage 1, bias network is required; see Application Circuit on page 8 as an example.
5, 10	V_{D2}	0.100 x 0.100	Drain voltage for stage 2, bias network is required; see Application Circuit on page 8 as an example.
6, 9	V_{D3}	0.200 x 0.100	Drain voltage for stage 3, bias network is required; see Application Circuit on page 8 as an example.
7, 8	V_{DET}, V_{REF}	0.100 x 0.100	Power detector and reference voltage
2	RF OUT	0.100 x 0.200	RF Output; matched to 50 Ω, DC blocked

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012

Caution!
ESD-Sensitive Device

Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.
Solder profiles available upon request. Use of no-clean solder to avoid washing after soldering is recommended.

Contact plating: NiAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Important Notice

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