Winbond Electronics Corp.

64K × 16 CMOS FLASH MEMORY

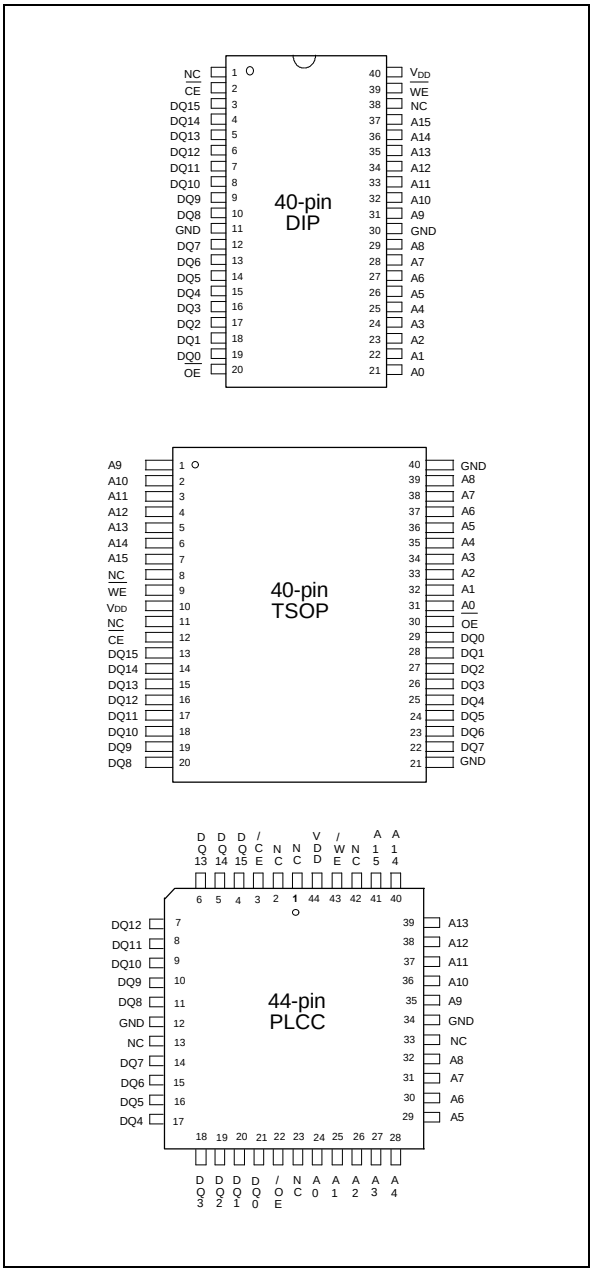
GENERAL DESCRIPTION

The W29C102 is a 1-megabit, 5-volt only CMOS flash memory organized as 64K × 16 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29C102 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

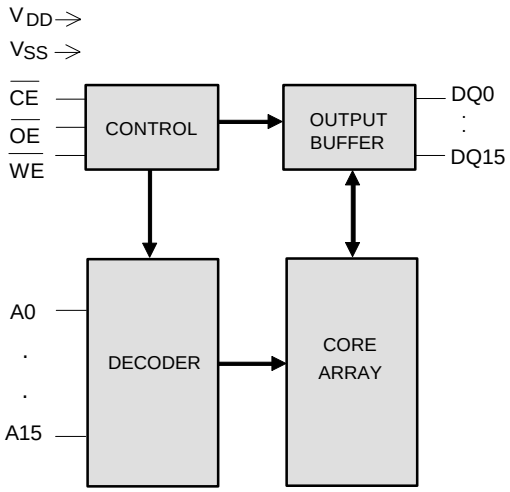
FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
  - 128 words per page
  - Page program cycle: 10 mS (max.)
  - Effective word-program cycle time: 39 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 70/90/120 nS
- Typical page program/erase cycles: 1K/10K
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic program timing with internal V_{PP} generation
- End of program detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard word-wide pinouts
- Available packages: 40-pin 600 mil DIP, TSOP and 44-pin PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A15	Address Inputs
DQ0–DQ15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C102 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Page Write Mode

The W29C102 is programmed on a page basis. Every page contains 128 words of data. If a word of data within a page is to be changed, data for the entire page must be loaded into the device. Any word that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing $\overline{CE}$ and $\overline{WE}$ low and $\overline{OE}$ high. The write procedure consists of two steps. Step 1 is the word-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the word-load cycle, the addresses are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. If the host loads a second word into the page buffer within a word-load cycle time (T_{BLC}) of 200 µS, after the initial word-load cycle, the W29C102 will stay in the page load cycle. Additional words can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional word is loaded into the page buffer. A_7 to $A15$ specify the page address. All words that are loaded into the page buffer must have the same page address. A_0 to A_6 specify the word address within the page. The words may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 words of data, are written simultaneously into the memory array. The typical programming time is 5 mS. The entire memory array can be written in 2.6 seconds. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-word program commands (with specific data to a specific address) to be performed before the data load operation. The three-word load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C102 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-word command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-word program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the

software data protection feature. To reset the device to unprotected mode, a six-word command sequence is required. See Table 3 for specific codes and Figure 10 for the timing diagram.

Hardware Data Protection

The integrity of the data stored in the W29C102 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 2.5V.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} has reached its sense level, the device will automatically time-out 5 mS before any write (erase/program) operation.

Data Polling (DQ_7 & DQ_{15})- Write Status Detection

The W29C102 includes a data polling feature to indicate the end of a programming cycle. When the W29C102 is in the internal programming cycle, any attempt to read DQ_7 and/or DQ_{15} of the last word loaded during the page/word-load cycle will receive the complement of the true data. Once the programming cycle is completed. DQ_7 will show the true data.

Toggle Bit (DQ_6 & DQ_{14})- Write Status Detection

In addition to data polling, the W29C102 provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ_6 and/or DQ_{14} will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

5-Volt-only Software Chip Erase

The chip-erase mode can be initiated by a six-word command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-word command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (00DAh). A read from address 0001H outputs the device code (004Fh). The product ID operation can be terminated by a three-word command sequence.

In the hardware access mode, access to the product ID is activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

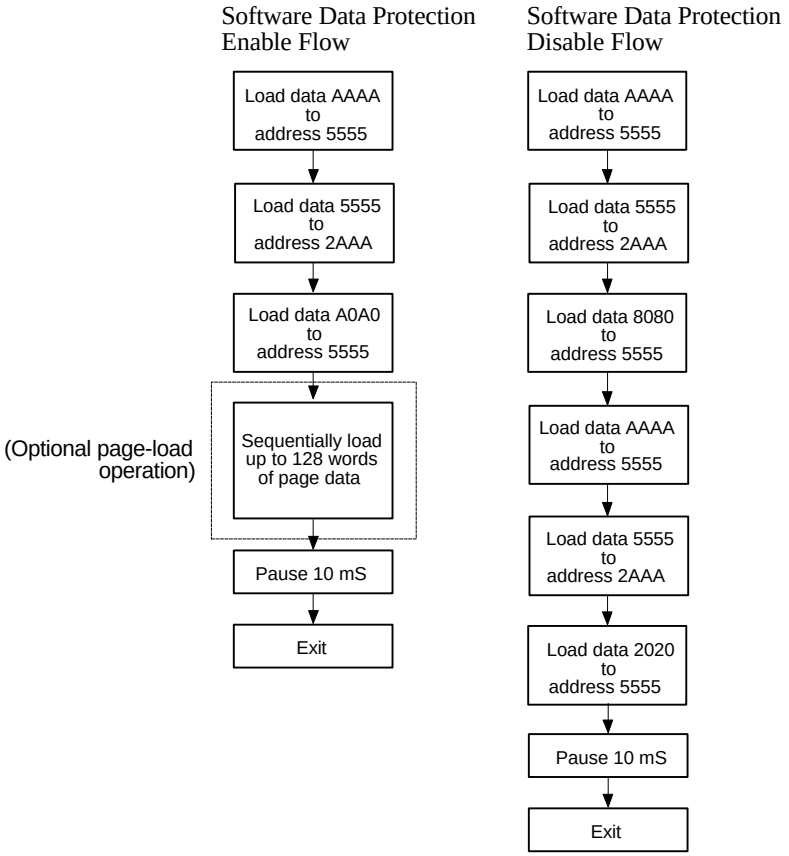
(V_{HH} = 12V)

MODE	PINS				
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
5-Volt Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1–A15 = V_{IL}; A9 = V_{HH}	Manufacturer Code 00DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1–A15 = V_{IL}; A9 = V_{HH}	Device Code 004F (Hex)

Command Codes for Software Data Protection

BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAAAH	5555H	AAAAH
1 Write	2AAAH	5555H	2AAAH	5555H
2 Write	5555H	A0A0H	5555H	8080H
3 Write	-	-	5555H	AAAAH
4 Write	-	-	2AAAH	5555H
5 Write	-	-	5555H	2020H

Software Data Protection Acquisition Flow

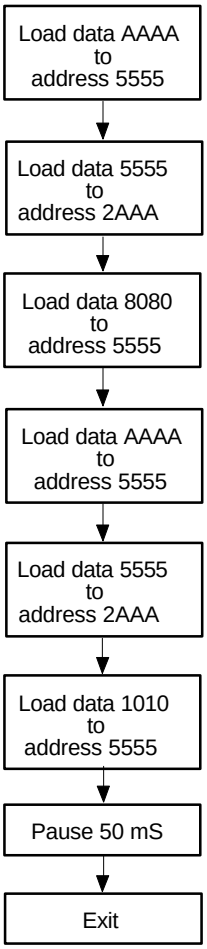


Notes for software program code:
Data Format: DQ15–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAAAH
1 Write	2AAAH	5555H
2 Write	5555H	8080H
3 Write	5555H	AAAAH
4 Write	2AAAH	5555H
5 Write	5555H	1010H

Software Chip Erase Acquisition Flow

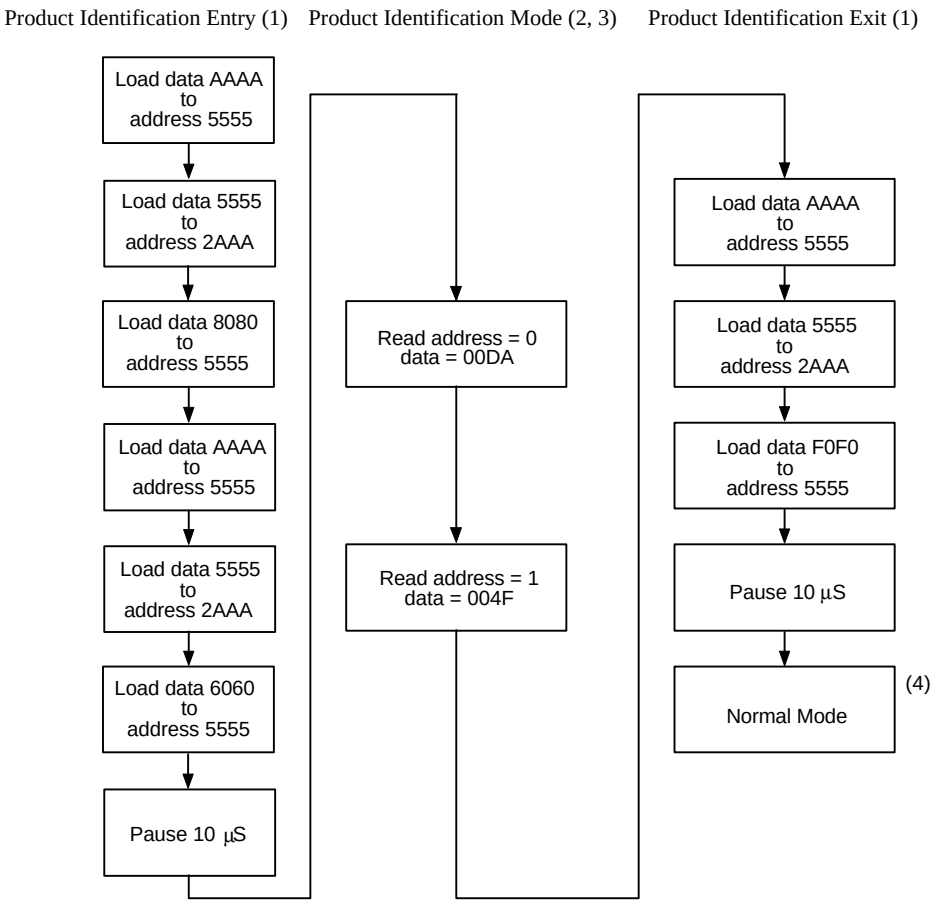


Notes for software chip erase:
Data Format: DQ15–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Product Identification

BYTE SEQUENCE	ALTERNATE SOFTWARE (5) PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H	2AAAH	55H
2 Write	5555H	90H	5555H	80H	5555H	F0H
3 Write	-	-	5555H	AAH	-	-
4 Write	-	-	2AAAH	55H	-	-
5 Write	-	-	5555H	60H	-	-
	Pause 10 µS		Pause 10 µS		Pause 10 µS	

Software Product Identification Acquisition Flow



Notes for software product identification:
(1) Data format: DQ15–DQ0 (Hex); address format: A14–A0 (Hex).
(2) A1–A15 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.
(3) The device does not remain in identification mode if power down.
(4) The device returns to standard operation mode.
(5) This product supports both the JEDEC standard 3 byte command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 byte command code sequence be used.

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except $\overline{OE}$	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 and $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$=$\overline{OE}$= V_{IL}, $\overline{WE}$= V_{IH}, all I/Os open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	25	60	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all I/Os open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all I/Os open Other inputs = V_{DD} -0.3V/GND	-	20	200	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V
Output High Voltage CMOS	V_{OH2}	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU. READ}$	100	µS
Power-up to Write Operation	$T_{PU. WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

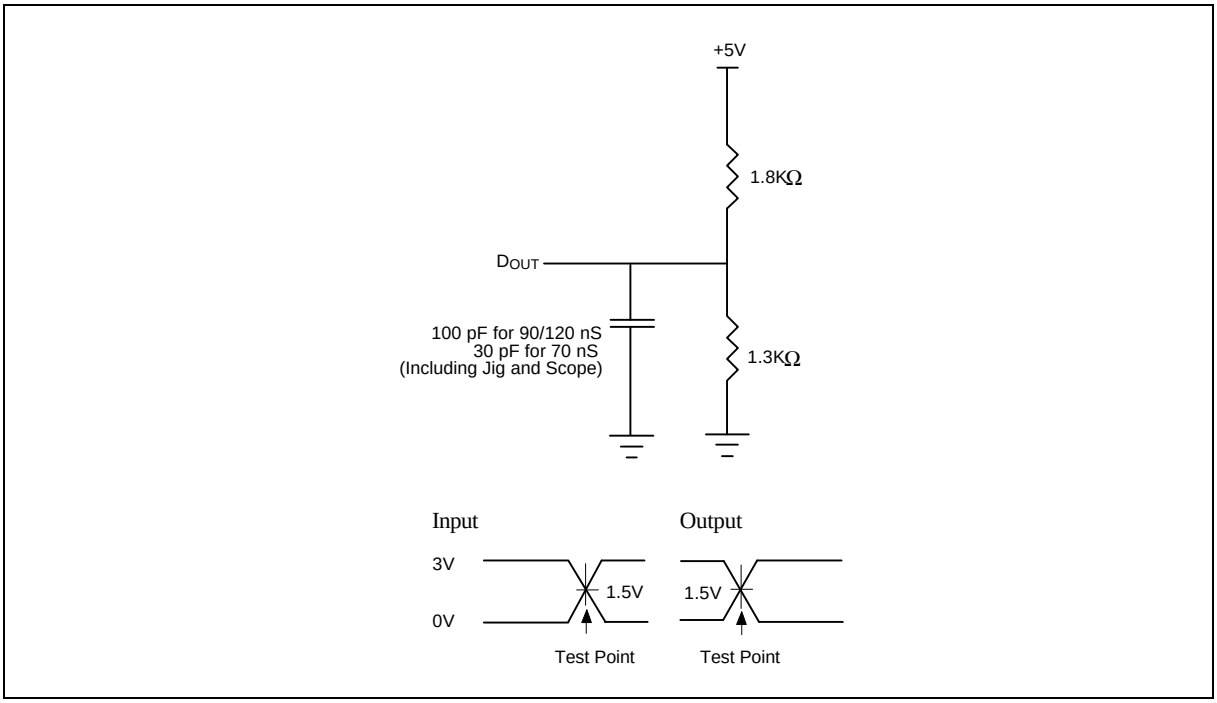
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pf
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pf

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF for 90/120 nS C_L = 30 pF for 70 nS

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W29C102-70		W29C102-90		W29C102-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	120	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	-	120	nS
Address Access Time	T_{AA}	-	70	-	90	-	120	nS
Output Enable Access Time	T_{OE}	-	35	-	45	-	60	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	25	-	25	-	30	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	25	-	25	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	0	-	nS

Byte/Page-write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	T_{WC}	-	-	10	mS
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	70	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	70	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	0	-	-	nS
Byte Load Cycle Time	T_{BLC}	-	-	150	µS

Notes:

All AC timing signals observe the following guidelines for determining setup and hold times:

(a) High level signal's reference level is V_{IH}.

(b) Low level signal's reference level is V_{IL}.

AC Characteristics, continued

$\overline{\text{DATA}}$ Polling Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
$\overline{OE}$ Hold Time	T_{OEH}	10	-	-	nS
$\overline{OE}$ to Output Delay (2)	T_{OE}	-	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

Notes:

(1) These parameters are characterized and not 100% tested.

(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

Toggle Bit Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
$\overline{OE}$ Hold Time	T_{OEH}	10	-	-	nS
$\overline{OE}$ to Output Delay (2)	T_{OE}	-	-	-	nS
$\overline{OE}$ High Pulse	T_{OEHP}	150	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

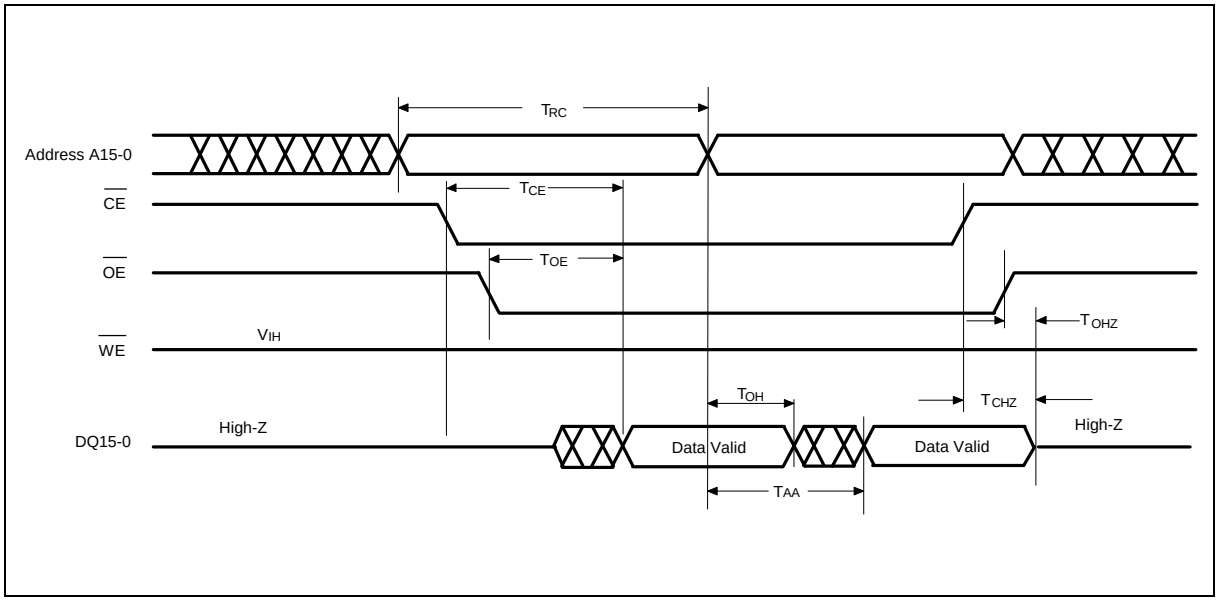
Notes:

(1) These parameters are characterized and not 100% tested.

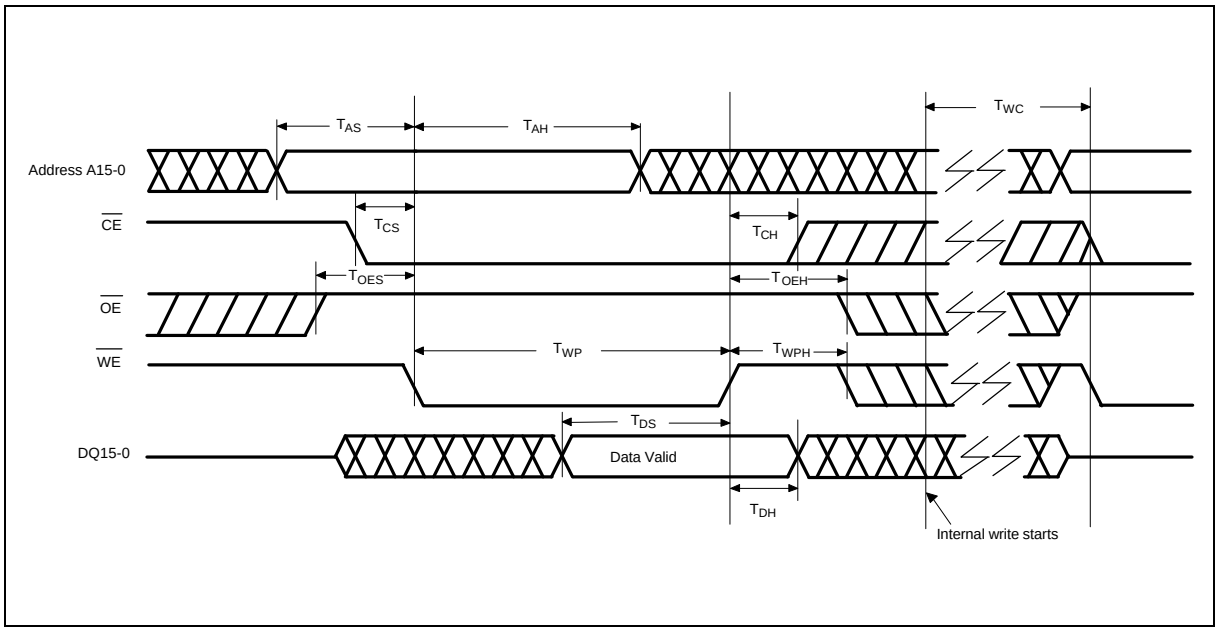
(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

TIMING WAVEFORMS

Read Cycle Timing Diagram

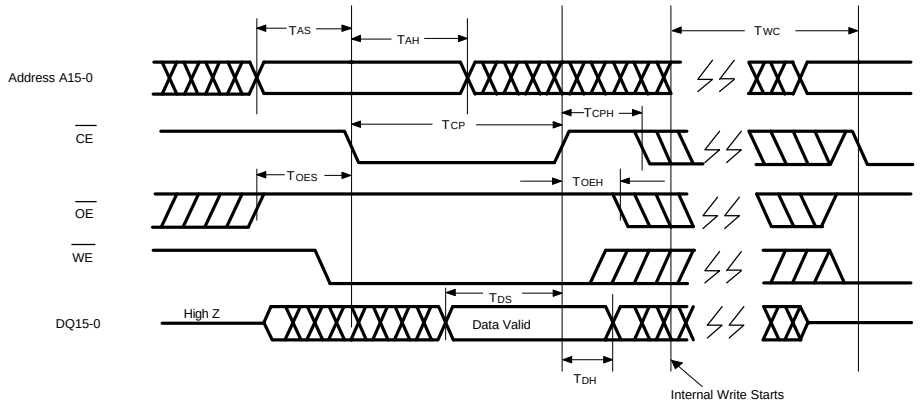


$\overline{WE}$ Controlled Write Cycle Timing Diagram

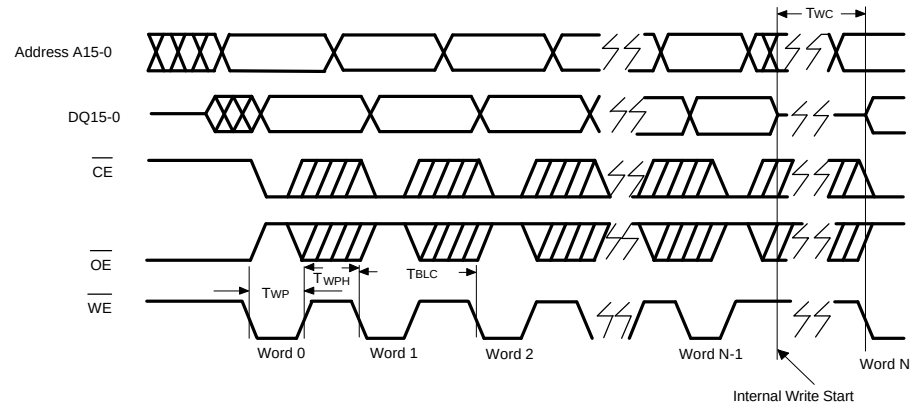


Timing Waveforms, continued

$\overline{CE}$ Controlled Write Cycle Timing Diagram

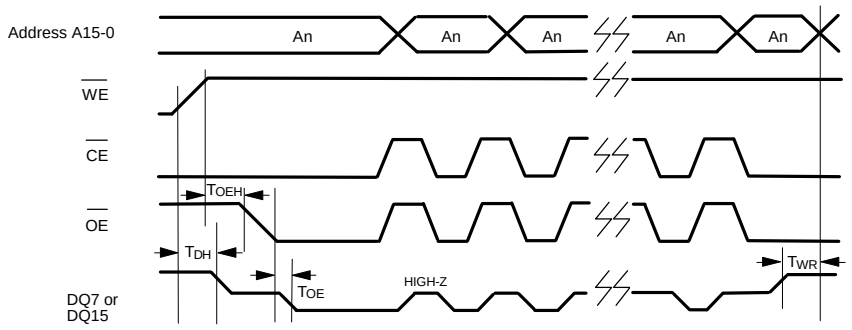


Page Write Cycle Timing Diagram

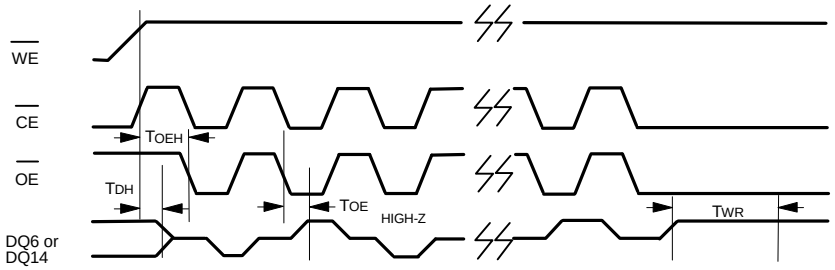


Timing Waveforms, continued

DATA Polling Timing Diagram



Toggle Bit Timing Diagram

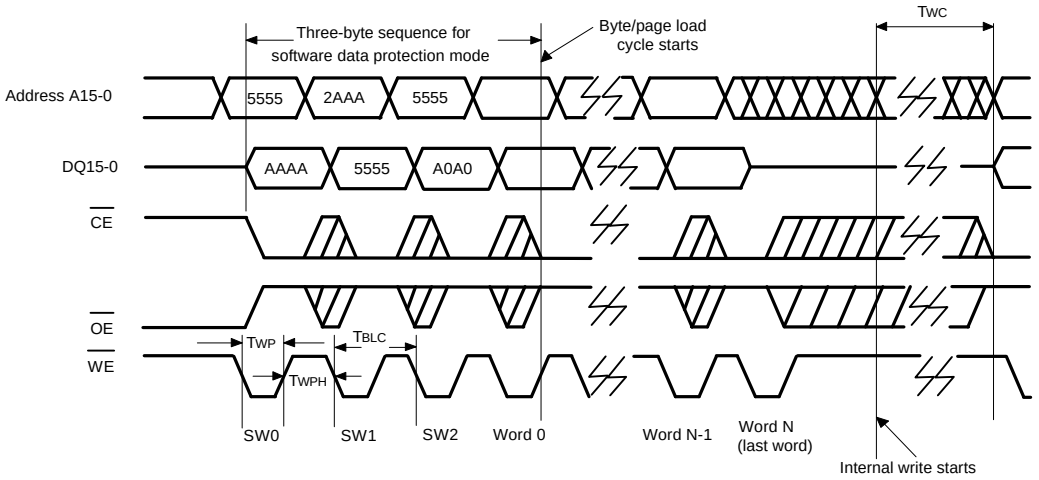


Notes:

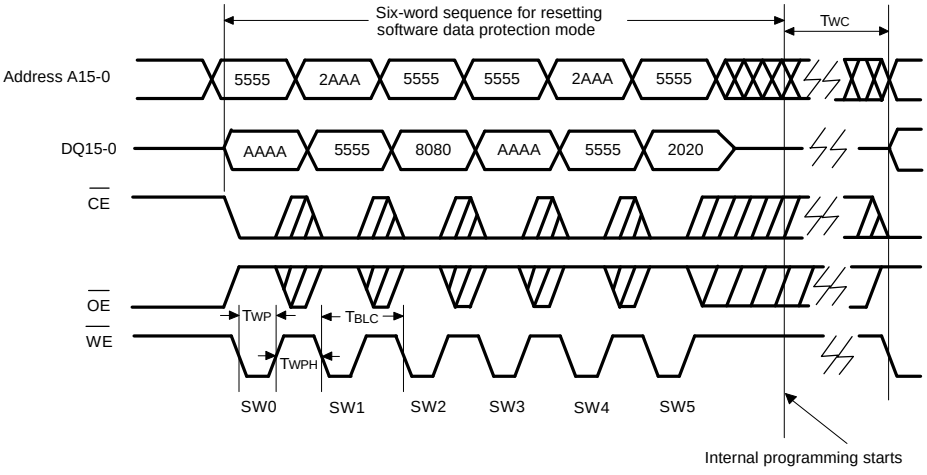
1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of DQ6 and DQ14 may vary.
3. Any address location may be used but the address should not vary.

Timing Waveforms, continued

Page Write Timing Diagram Software Data Protection Mode

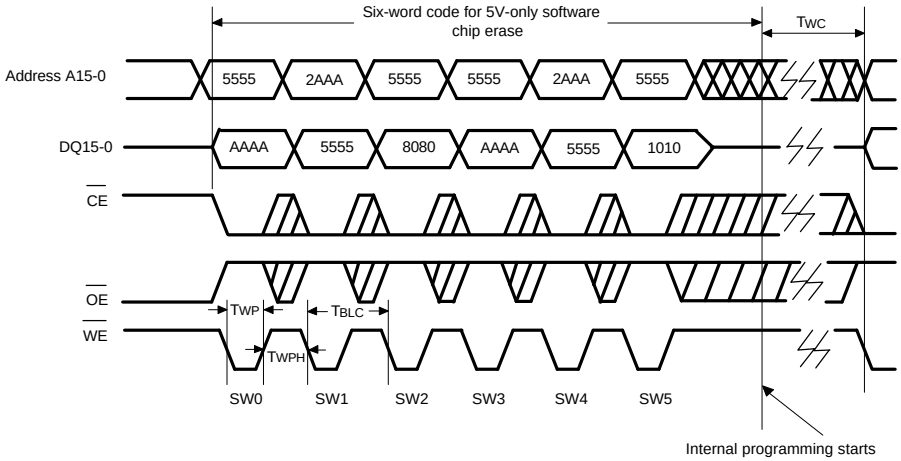


Reset Software Data Protection Timing Diagram



Timing Waveforms, continued

5-Volt-only Software Chip Erase Timing Diagram



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY VDD CURRENT MAX. (μA)	PACKAGE	CYCLE
W29C102-70	70	60	200	600 mil DIP	1K
W29C102-90	90	60	200	600 mil DIP	1K
W29C102-12	120	60	200	600 mil DIP	1K
W29C102Q-70	70	60	200	40-pin TSOP (10 mm × 14 mm)	1K
W29C102Q-90	90	60	200	40-pin TSOP (10 mm × 14 mm)	1K
W29C102Q-12	120	60	200	40-pin TSOP (10 mm × 14 mm)	1K
W29C102T-70	70	60	200	40-pin TSOP (10 mm × 20 mm)	1K
W29C102T-90	90	60	200	40-pin TSOP (10 mm × 20 mm)	1K
W29C102T-12	120	60	200	40-pin TSOP (10 mm × 20 mm)	1K
W29C102P-70	70	60	200	44-pin PLCC	1K
W29C102P-90	90	60	200	44-pin PLCC	1K
W29C102P-12	120	60	200	44-pin PLCC	1K
W29C102-70B	70	60	200	600 mil DIP	10K
W29C102-90B	90	60	200	600 mil DIP	10K
W29C102-12B	120	60	200	600 mil DIP	10K
W29C102Q-70B	70	60	200	40-pin TSOP (10 mm × 14 mm)	10K
W29C102Q-90B	90	60	200	40-pin TSOP (10 mm × 14 mm)	10K
W29C102Q-12B	120	60	200	40-pin TSOP (10 mm × 14 mm)	10K
W29C102T-70B	70	60	200	40-pin TSOP (10 mm × 20 mm)	10K
W29C102T-90B	90	60	200	40-pin TSOP (10 mm × 20 mm)	10K
W29C102T-12B	120	60	200	40-pin TSOP (10 mm × 20 mm)	10K
W29C102P-70B	70	60	200	44-pin PLCC	10K
W29C102P-90B	90	60	200	44-pin PLCC	10K
W29C102P-12B	120	60	200	44-pin PLCC	10K

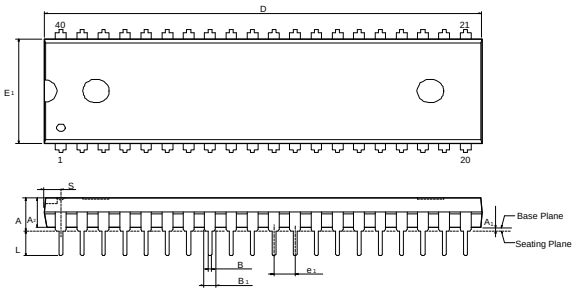
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Winbond Electronics Corp.

PACKAGE DIMENSIONS

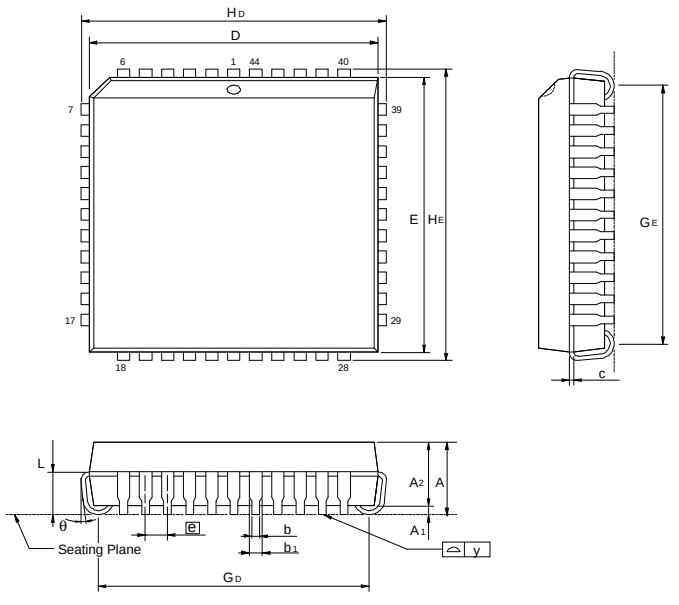
40-pin PDIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

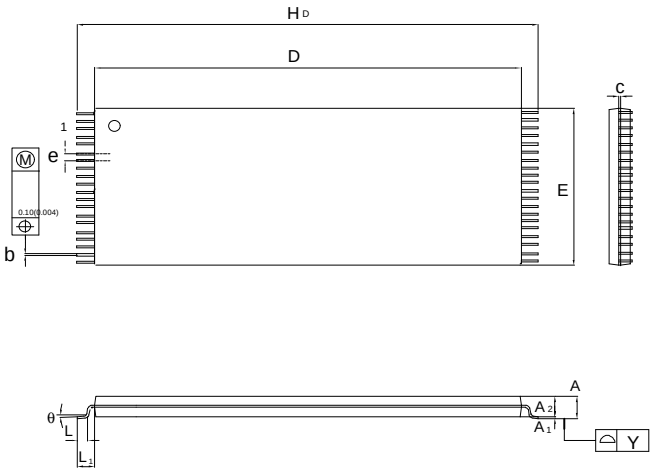


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

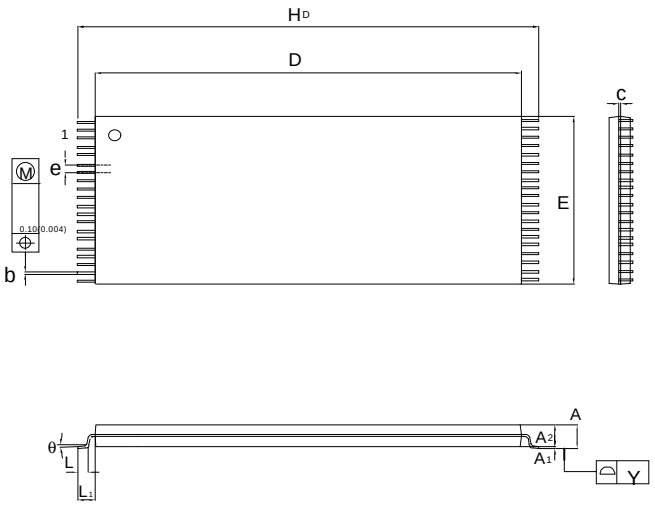
40-pin TSOP (10 mm × 14 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A 1	0.002	—	0.006	0.05	—	0.15
A 2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.484	0.488	0.492	12.30	12.40	12.50
E	0.390	0.394	0.398	9.90	10	10.10
H D	0.543	0.551	0.559	13.80	14.00	14.20
e	—	0.020	—	—	0.50	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L 1	—	0.031	—	—	0.8	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

40-pin TSOP (10 mm × 20 mm)



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A 1	0.002	—	0.006	0.05	—	0.15
A 2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.72	0.724	0.728	18.3	18.4	18.5
E	0.390	0.394	0.398	9.90	10	10.10
H D	0.780	0.787	0.795	19.8	20.0	20.2
e	—	0.020	—	—	0.50	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L 1	—	0.031	—	—	0.8	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A3	Mar. 1998	6	Add. pause 10 mS
		7	Add. pause 50 mS
		8	Correct the time from 10 mS to 10 μS
		11	Change V_{DD} from 5% to 10% for 70 nS

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