Boost and Dual LDOs with POK

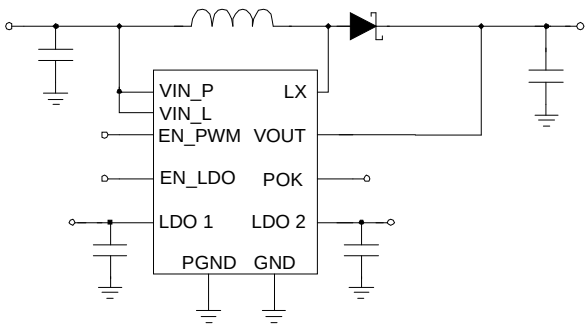
Features

- **Wide Input Voltage from 3V to 5.5V**
- **Built-in Soft-start**
- **Boost Converter Fixed Output Voltage:**
  APW7251:13.5V
  APW7251A:12.3V
- **<1uA Quiescent Current During Shutdown**
- **Boost Converter in PFM Mode**
- **Internal Switch Current Limit : 250 mA**
- **High Efficiency at 3.3V to 18V/10mA**
- **Dual LDOs With POK**
- **High PSRR: 70dB at 1KHz**
- **Low Dropout Voltage:**
  - 450mV at 150mA (LDO1_1.8V)
  - 100mV at 150mA (LDO2_3.3V)
  - 100mV at 150mA (LDO2_3.2V_APW7251A)
- **2x2mm TQFN-12 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Touch Panel**

Simplified Application Circuit



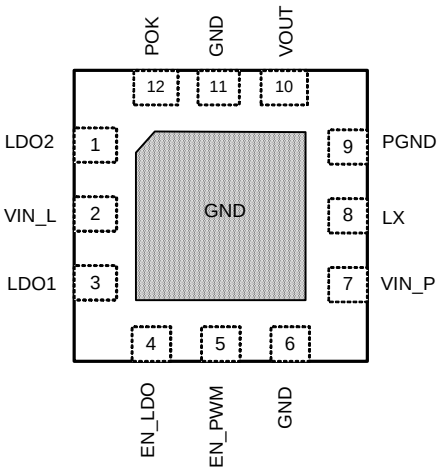
General Description

The APW7251 contains a PWM Boost converter, a 1.8V linear regulator and a 3.3V linear regulator.

The PWM boost converter is a high frequency step-up DC/DC converter. Its output voltage is set by an internal feedback divider at 13.5V and 12.3V.

The regulator is a P-channel low dropout linear regulator with POK which needs only one input voltage from 3 to 5. 5V, and delivers current up to 10mA to set output voltage. Typical dropout voltage is 450mV at 150mA loading for 1. 8V output, and 100mV at 150mA loading for 3.3V output. The APW7251 has power-on-reset and soft start functions to prevent wrong operation and limit the surge current during power-on or start-up. It also has thermal shutdown function to protect the device against over-temperature.

Pin Configuration



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7251/A □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
QB : TQFN 2x2-12
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW7251 QB:



X- Date Code

APW7251A QB:



X- Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN to GND Voltage		-0.3 ~ 6	V
V_{SW}	SW to GND Voltage	>20ns	-0.3 ~ V_{IN}+0.3	V
		<20ns	3 ~ 8	V
	EN, POK,Vout to GND Voltage		-0.3 ~ 7	V
T_J	Maximum Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature Range		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air TQFN2x2-12	165	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
$V_{INP/L}$	VINP/L to GND Voltage	3 ~ 5.5	V
C_{IN}	Input Capacitor	2.2	µF
C_{OUT}	Output Capacitor	2.2 ~ 4.7	µF
C_{LDO1}, C_{LDO2}	LDO1, LDO2 Output Capacitor	1	µF
L	Inductor	10 ~ 22	µH
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN_P/L}$=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7251A			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
$V_{IN_P/L}$	Input Voltage Range	TA = -40 ~ 85°C, T_J = -40 ~ 125°C	3	-	5.5	V
I_{PWMDC}	Input DC Bias Current	V_{EN_PWM} = 5V	-	1	-	mA
I_{PWMSD}		V_{EN_PWM}=0V	-	20	30	uA
I_{LDODC}		V_{EN_LDO} = 5V	-	200	500	µA
I_{LDOSD}		V_{EN_LDO}=0V	-	0.1	1	µA
UNDER-VOLTAGE LOCKOUT						
	UVLO Threshold Voltage	$V_{IN_P/L}$ Rising	2.2	2.5	2.9	V
	UVLO Hysteresis Voltage		-	200	-	mV
SOFT START AND SHUTDOWN						
T_{SS}	Soft Start Time	V_{OUT} rising from 0 to 90%, R_{LOAD}=50Ω	-	60	-	µs
V_{TEN_PWM}	EN_PWM Voltage Threshold	V_{EN_PWM} Rising	0.4	0.7	1	V
	EN_PWM Voltage Hysteresis		-	0.1	-	V
V_{TEN_LDO}	EN_LDO Input Logic HIGH		0.4	0.7	1	V
	EN_LDO Voltage Hysteresis		-	0.1	-	V
I_{LEN_PWM}	EN_PWM Leakage Current	V_{IN} = 5V, V_{EN_PWM} = 5V	-1	-	1	µA
I_{LEN_LDO}	EN_LDO Leakage Current	V_{IN} = 5V, V_{EN_LDO} = 5V	-1	-	1	µA
OVER TEMPERATURE PROTECTION						
	Over Temperature Threshold		-	150	-	°C
	Over Temperature Hysteresis		-	40	-	°C
POWER OK AND DELAY						
	Rising POK Threshold Voltage	V_{LDO2} rising	2.36	2.6	2.73	V
	Rising POK Threshold Voltage Hysteresis	V_{LDO2} falling	-	200	-	mV
	POK Low to High Delay Time		-	8	-	ms
	POK Output LOW Voltage	POK sink 5mA	-	0.25	-	V

Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN_P/L}$=5V. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions		APW7251A			Unit
				Min	Typ	Max	
PWM							
R_{ON}	Power Switch On Resistance			-	0.8	-	Ω
	LX Minimum Off Time			-	450	-	ns
I_{LIM}	Power Switch Current Limit			0.1	0.20	0.3	A
	LX Leakage Current	V_{EN_PWM} = GND, V_{EN_LDO} = GND		-1	-	1	μA
	Boost Converter Output Voltage	T_A = 25°C, APW7251		-	13.5	-	V
		T_A = 25°C, APW7251A		-	12.3	-	V
	Boost Converter Output Voltage Accucacy	T_A = 25°C		-3	-	+3	%
F_{SW}	Switching Frequency			-	880	-	kHz
LDO REGULATOR							
	Output Voltage Accuracy	$I_{LDO1/2}$ =1mA to 150mA, T_A= -40 ~ 85°C		-3	-	+3	%
V_{LDO1}	LDO1 Output Voltage			-	1.8	-	V
V_{LDO2}	LDO2 Output Voltage			-	3.3	-	V
	LDO2 Output Voltage	APW7251A		-	3.2	-	V
	Line Regulation	$I_{LDO1/2}$ =1mA, $V_{IN_P/L}$=$V_{LDO1/2}$+0.3V to 5.5V, or $V_{IN_P/L}$=2.5V to 5.5V		-	-	0.2	%/V
	Load Regulation	$I_{LDO1/2}$=1mA to 150mA		-	-	0.6	%
V_{DROP1}	V_{LDO1} Dropout Voltage	I_{LDO1}=150mA		-	450	-	mV
V_{DROP2}	V_{LDO2} Dropout Voltage	I_{LDO2}=150mA		-	100	-	mV
PSRR	Power Supply Rejection Ratio	$I_{LDO1/2}$=50mA, $C_{LDO1/2}$=1μF	f=1kHz	-	70	-	dB
			f=10kHz	-	60	-	
			f=100kHz	-	35	-	
	Output Noise	$I_{LDO1/2}$=1mA, BW=10 to 100kHz, $C_{LDO1/2}$=10μF		-	100	-	$μV_{RMS}$
	$V_{LDO1/2}$ Discharge Resistance	V_{EN_LDO}=0V		-	3	-	KΩ
I_{LIMIT}	LDO1 Current limit Threshold			200	350	-	mA
	LDO2 Current limit Threshold			450	700	-	mA
I_{SHORT}	Short Circuit Output Current			-	50	-	mA

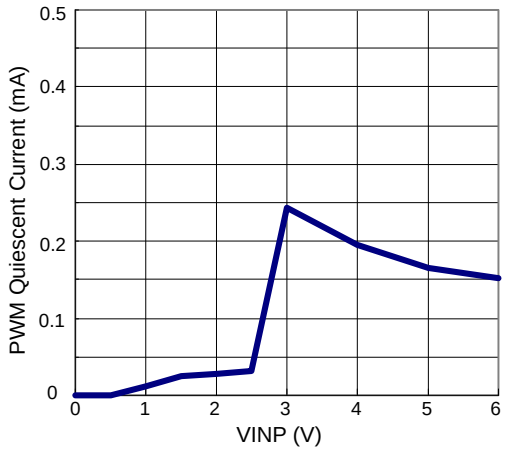
Pin Description

TDFN2x2-12	NAME	FUNCTION
1	LDO2	Regulator output pin. Output Voltage is 3.3V
2	VIN_L	Supply voltage pin.
3	LDO1	Regulator output pin. Output Voltage is 1.8V
4	EN_LDO	Enable control pin. Pulling this pin to ground forces the device into shutdown mode reducing the supply current to less than 1μA. This pin should not be left floating.
5	EN_PWM	Enable control pin. Pulling this pin to ground forces the device into shutdown mode reducing the supply current to less than 1μA. This pin should not be left floating.
6, 11	GND	Signal Ground. Connecting this pin to PGND.
7	VIN_P	Supply voltage pin.
8	LX	Switch Pin. Connect this pin to inductor/diode here.
9	PGND	Power Ground of the Low-Side Gate Driver. Use a separate track to connect this pin to Source of the low-side MOSFET. The Source of the low-side MOSFET must be connected to system ground with very low impedance. Connecting this pin to GND.
10	VOUT	Output Sense Pin. An internal divider sets the output voltage of boost converter at 13.5V. Connect the output of the boost converter to VOUT pin to form a feedback loop.
12	POK	Power Good Output. Connecting a resistor to supply voltage pin. This pin should not be left floating.

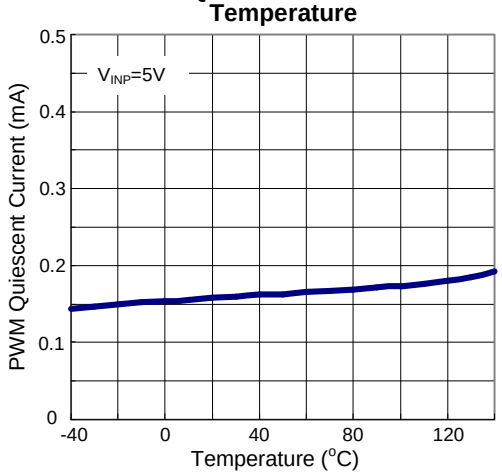
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Typical Operating Characteristics

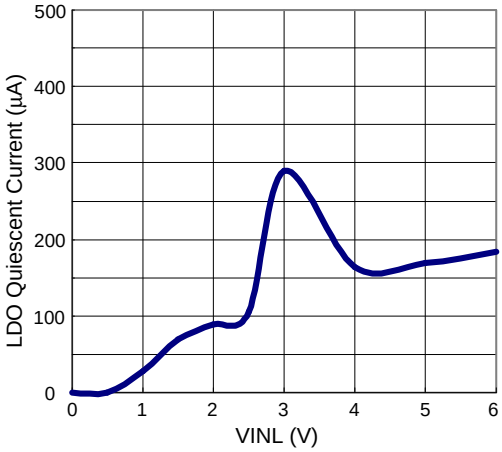
PWM Quiescent Current vs. VINP



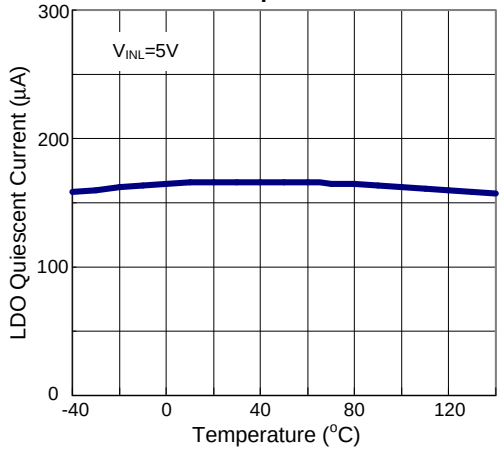
PWM Quiescent Current vs. Temperature



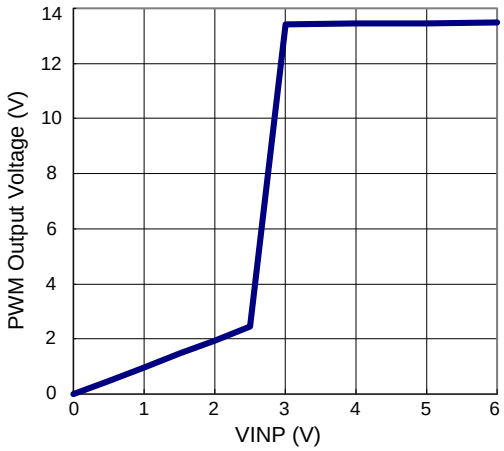
LDO Quiescent Current vs. VINL



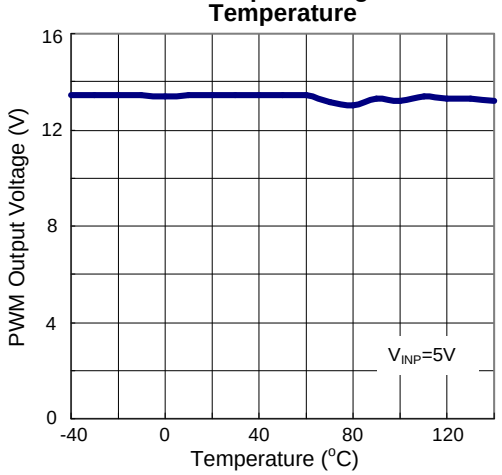
LDO Quiescent Current vs. Temperature



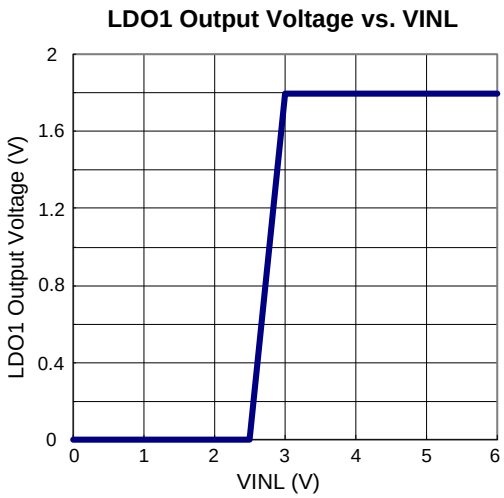
PWM Output Voltage vs. VINP

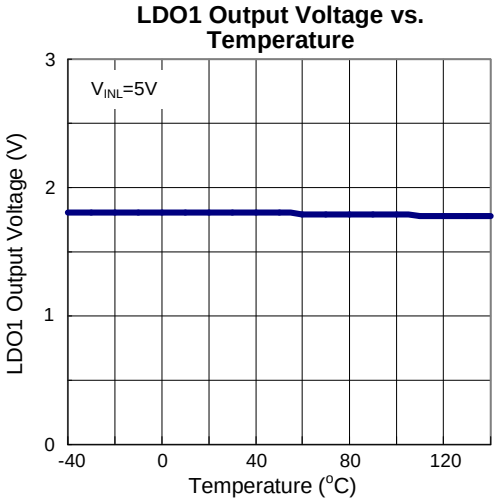


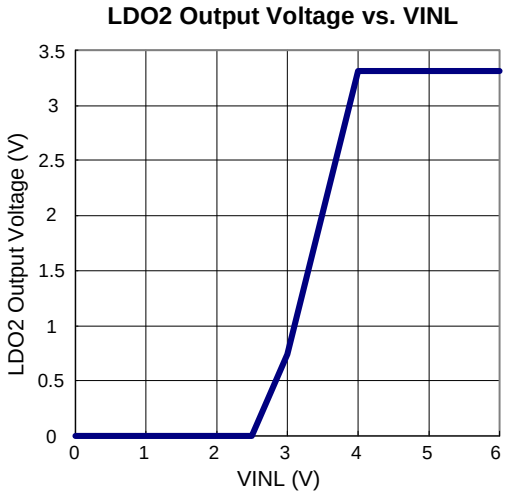
PWM Output Voltage vs. Temperature

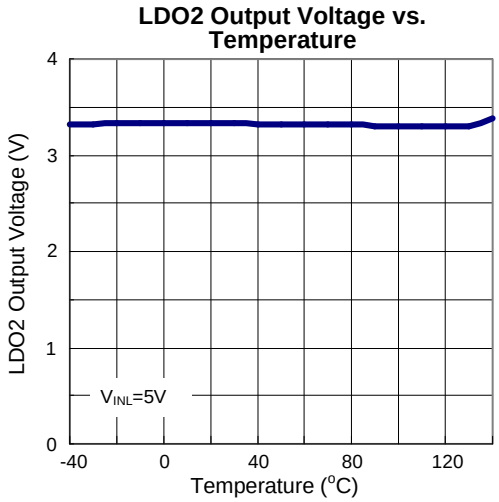


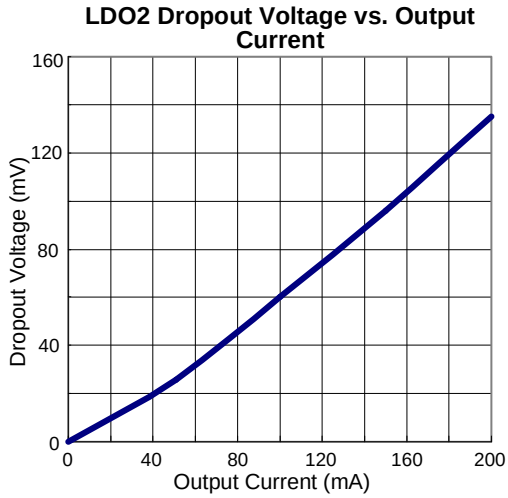
Typical Operating Characteristics





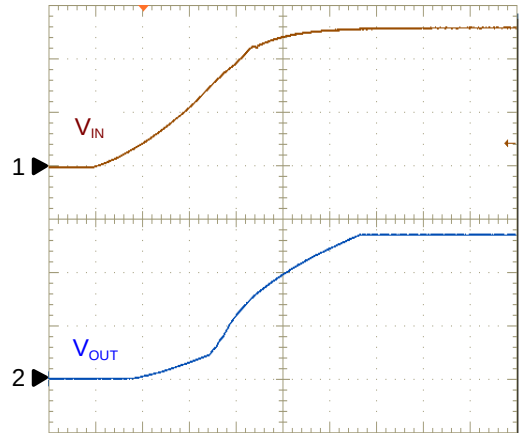






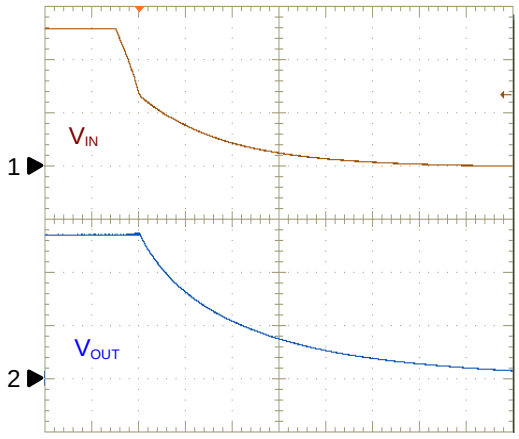
Operating Waveforms

PWM Power On



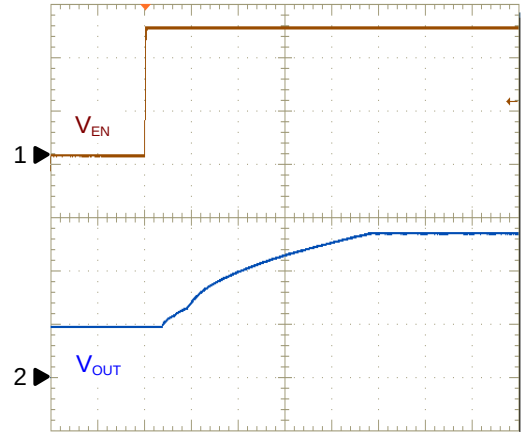
C_{IN}=4.7µF,C_{OUT}=2.2µF
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},5V/Div, DC
TIME:4ms/Div

PWM Power Off



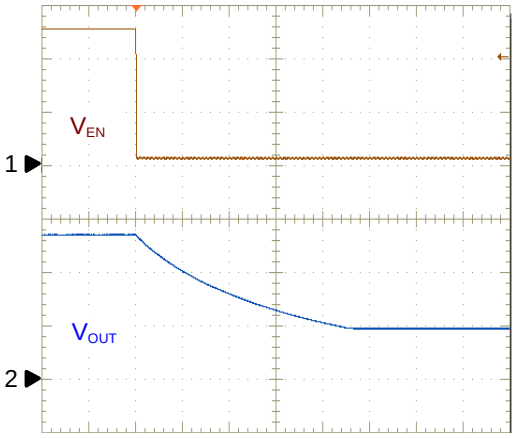
C_{IN}=4.7µF,C_{OUT}=2.2µF
CH1:V_{IN},2V/Div, DC
CH2:V_{OUT},5V/Div, DC
TIME:400ms/Div

PWM Enable Response



C_{IN}=4.7µF,C_{OUT}=2.2µF
CH1:V_{EN},2V/Div, DC
CH2:V_{OUT},5V/Div, DC
TIME:2ms/Div

PWM Disable Response

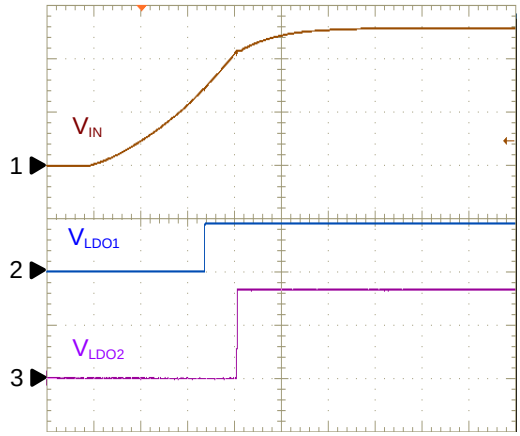


C_{IN}=4.7µF,C_{OUT}=2.2µF
CH1:V_{EN},2V/Div, DC
CH2:V_{OUT},5V/Div, DC
TIME:200ms/Div

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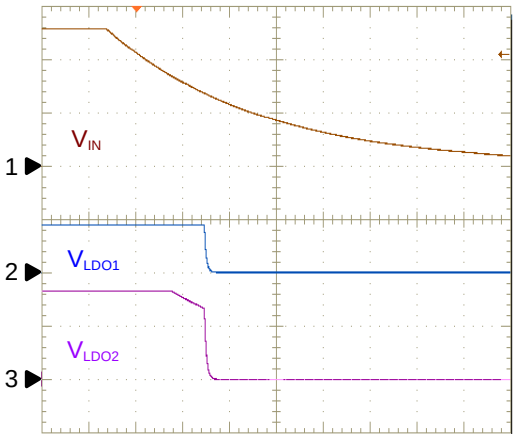
Operating Waveforms

LDO Power On



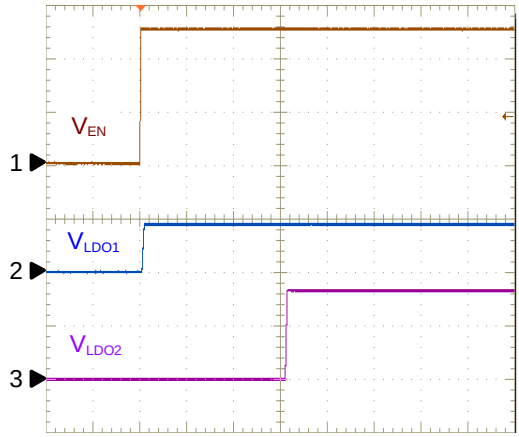
C_{IN}=1µF,C_{LDO1}=2.2µF,C_{LDO2}=2.2µF
CH1:V_{IN},2V/Div, DC
CH2:V_{LDO1},2V/Div, DC
CH3:V_{LDO2},2V/Div, DC
TIME:4ms/Div

LDO Power Off



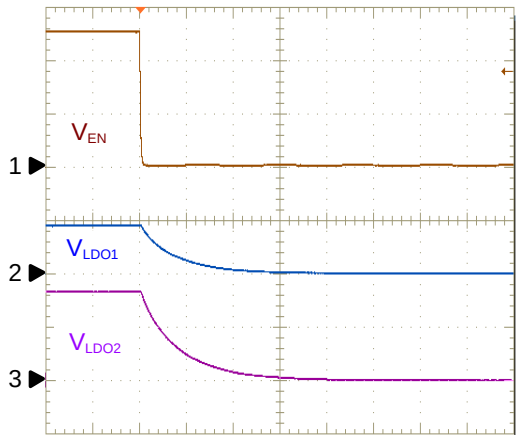
C_{IN}=1µF,C_{LDO1}=2.2µF,C_{LDO2}=2.2µF
CH1:V_{IN},2V/Div, DC
CH2:V_{LDO1},2V/Div, DC
CH3:V_{LDO2},2V/Div, DC
TIME:200ms/Div

LDO Enable Response



C_{IN}=1µF,C_{LDO1}=2.2µF,C_{LDO2}=2.2µF
CH1:V_{EN},2V/Div, DC
CH2:V_{LDO1},2V/Div, DC
CH3:V_{LDO2},2V/Div, DC
TIME:1ms/Div

LDO Disable Response

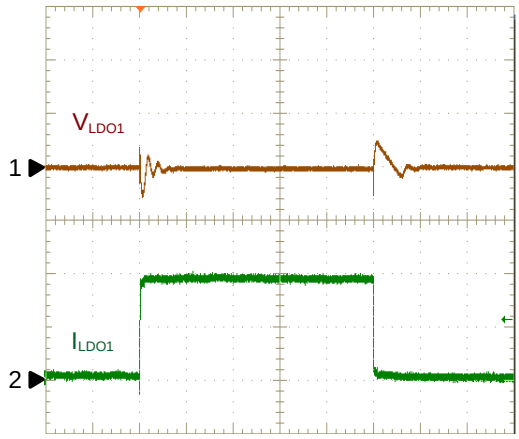


C_{IN}=1µF,C_{LDO1}=2.2µF,C_{LDO2}=2.2µF
CH1:V_{EN},2V/Div, DC
CH2:V_{LDO1},2V/Div, DC
CH3:V_{LDO2},2V/Div, DC
TIME:10ms/Div

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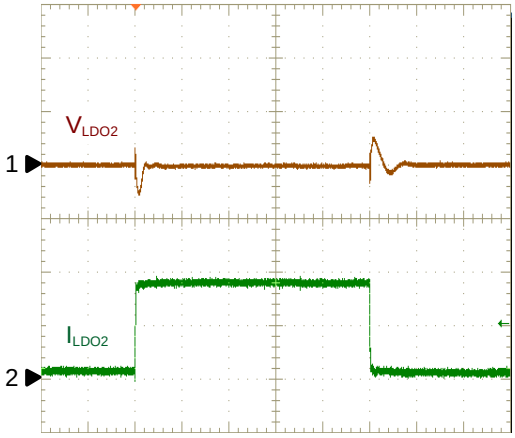
Operating Waveforms

LDO1 Load Transient Response



C_{IN}=1µF,C_{LDO1}=2.2µF
I_{LDO1}=1mA to 100mA to 1mA
CH1:V_{LDO1},50mV/Div, DC,Offset=1.8V
CH2:I_{LDO1},50mA/Div, DC
TIME:10µs/Div

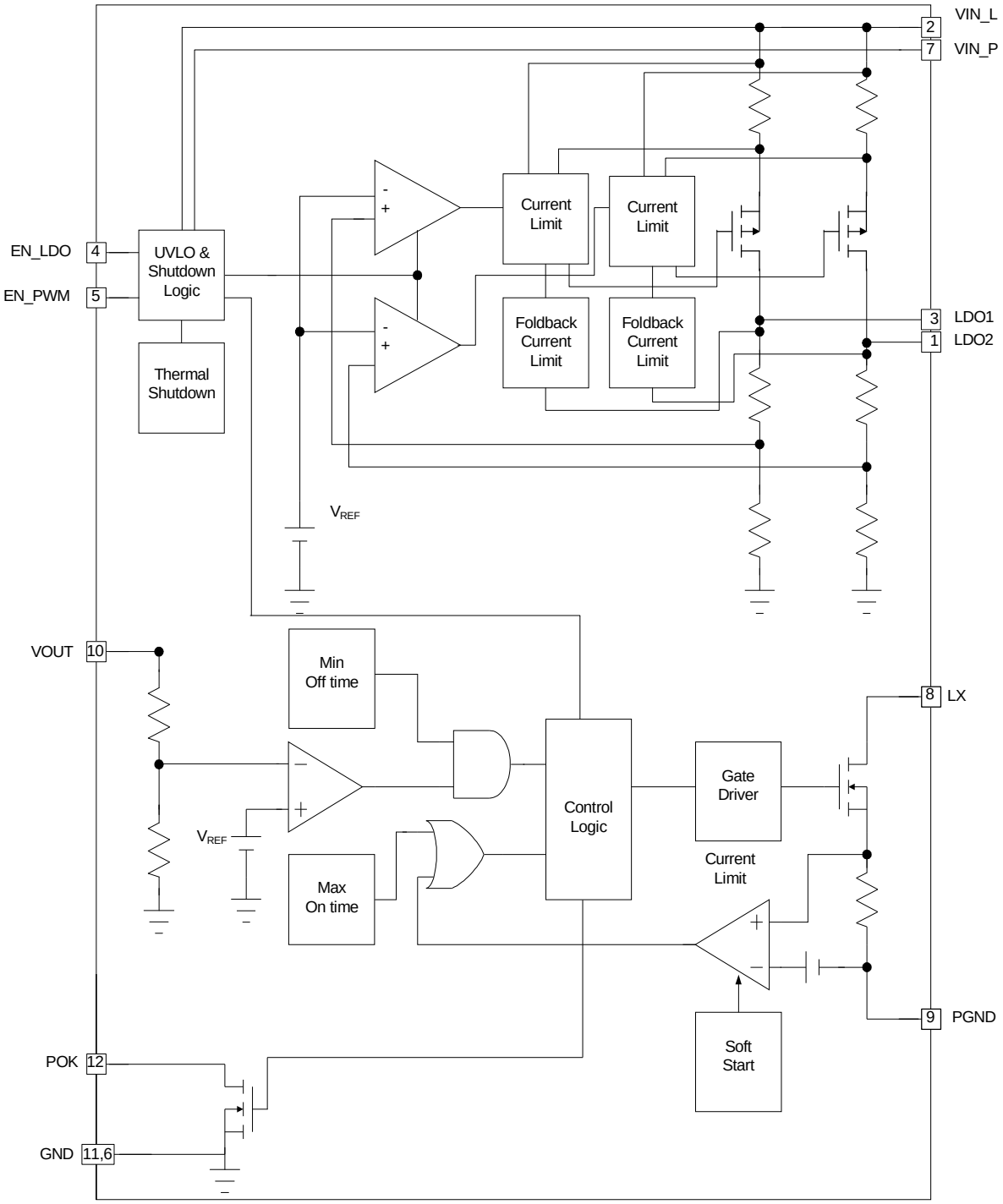
LDO2 Load Transient Response



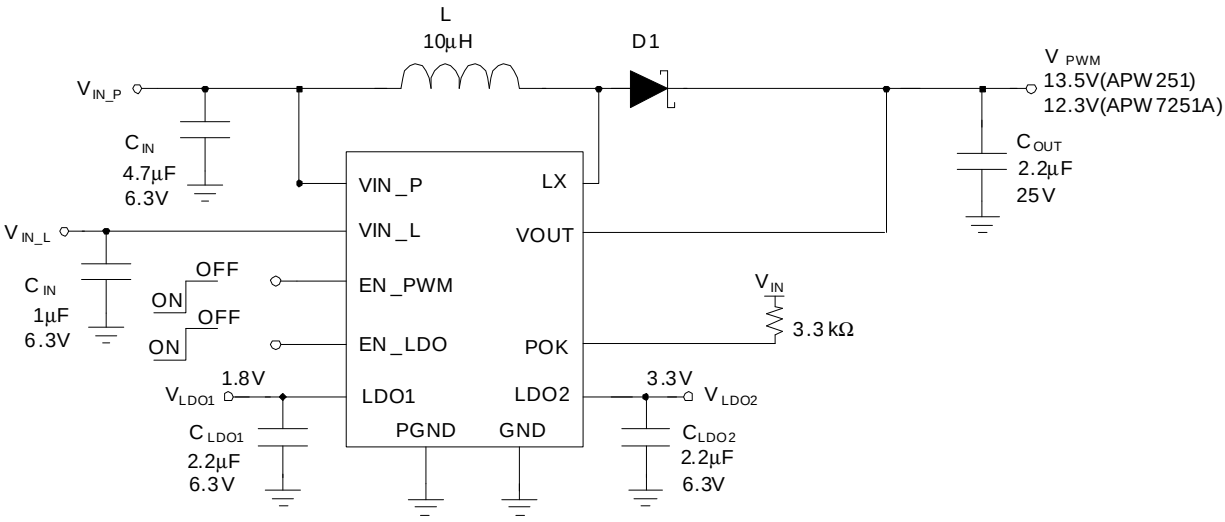
C_{IN}=1µF,C_{LDO2}=2.2µF
I_{LDO2}=1mA to 100mA to 1mA
CH1:V_{LDO2},50mV/Div, DC,Offset=3.3V
CH2:I_{LDO2},50mA/Div, DC
TIME:10µs/Div

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Block Diagram



Typical Application Circuit



Function Description

Under Voltage Lockout

Transients cause system damage or failure when powering on or undergoing instantaneous glitches in the supply voltage. Then, the under voltage lockout circuit turns the main switch off to prevent malfunction at low input voltage.

Soft-Start

The APW7251 limits this inrush current by increasing the current limit at start-up. The soft-start time is programmed by the internal circuit. The soft star time is 2ms for PWM, 60us for LDO.

Shutdown

Driving EN_PWM and EN_LDO to ground places the APW7251 in shutdown. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current of VIN reduces to <1μA

PWM Main Control Loop

The APW7251 operates in a PFM scheme. The operation can be understood by referring to the Block Diagram. The converter keeps monitoring the output voltage through the internal resistor-divider connected with VOUT. The switch turns off if the inductor current reaches the internal peak current limit. The second criterion that turns off the switch is the maximum on-time control. As the switch is off, the external Schottky diode forwards bias, so that the current is delivered to the output. The switch remains off for a minimum off time, and it wouldn't be turned on again until the feedback voltage drops below the reference voltage. This regulation scheme allows a wider selection range for the inductor and output capacitor.

Current-Limit with Current Foldback

The regulator monitors the current via the output PMOS and limits the maximum current. When the output current reaches the current-limit threshold, current-limit with current foldback circuit starts to work to prevent load and regulator from damages during overload or short-circuit conditions. Typical foldback current is about 50mA.

Thermal Shutdown

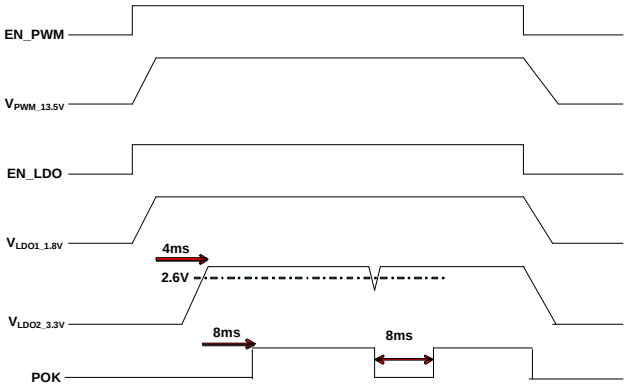
A thermal shutdown circuit limits the junction temperature of APW7251. When the junction temperature exceeds +150°C, a thermal sensor turns off the output PMOS, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 40°C. The thermal shutdown is designed with a 40°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, device power dissipation should be externally limited so that junction temperature will not exceed 125°C.

POK Indicator

The POK is used to indicate the status of the V_{LDO2}. When V_{LDO2} >2.6V, POK rise after 8ms delay time, If V_{LDO2} <2.6V, POK pulls low after 8ms delay time. This pin should not be floating.

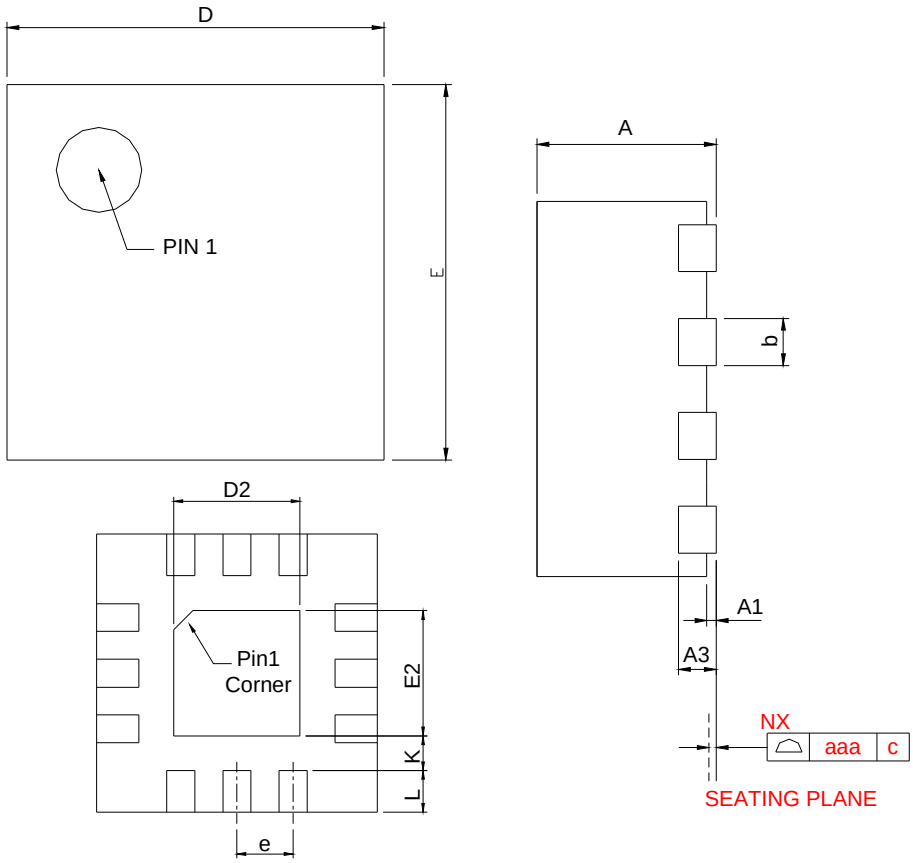
Power Sequence

The power sequence of APW7251 is shown as below diagram.



Package Information

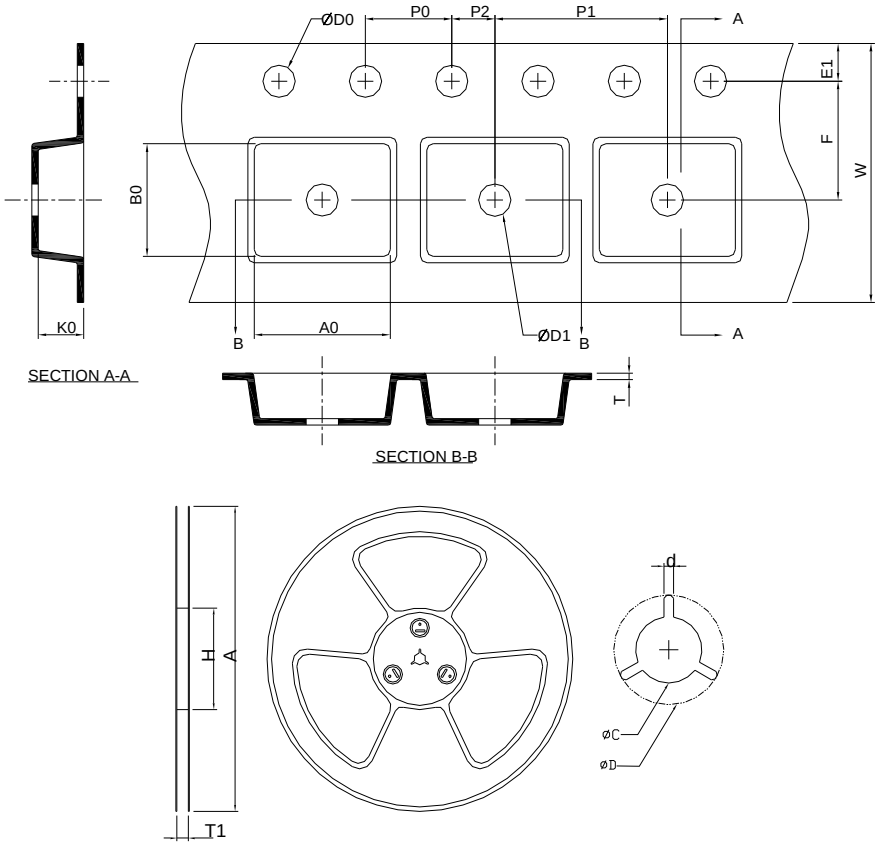
TQFN2x2-12



SYMBOL	TQFN2x2-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	1.90	2.10	0.075	0.083
D2	0.80	1.00	0.031	0.039
E	1.90	2.10	0.075	0.083
E2	0.80	1.00	0.031	0.039
e	0.40 BSC		0.016 BSC	
L	0.25	0.35	0.010	0.014
K	0.20		0.008	
aaa	0.08		0.003	

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Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN2x2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20

(mm)

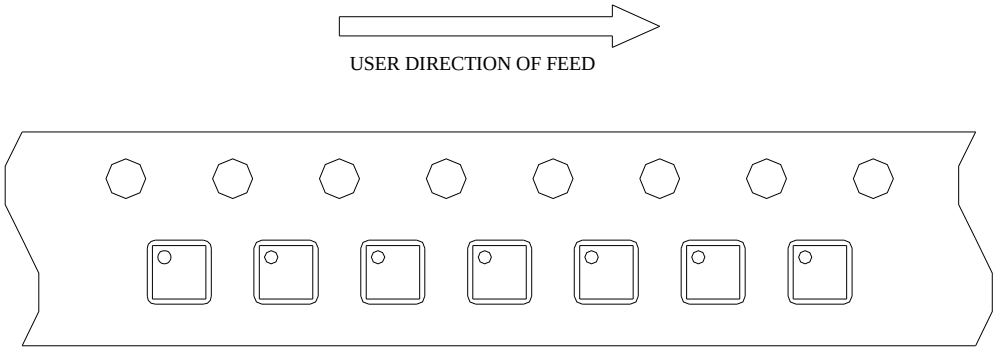
Devices Per Unit

Package Type	Unit	Quantity
TQFN2x2	Tape & Reel	3000

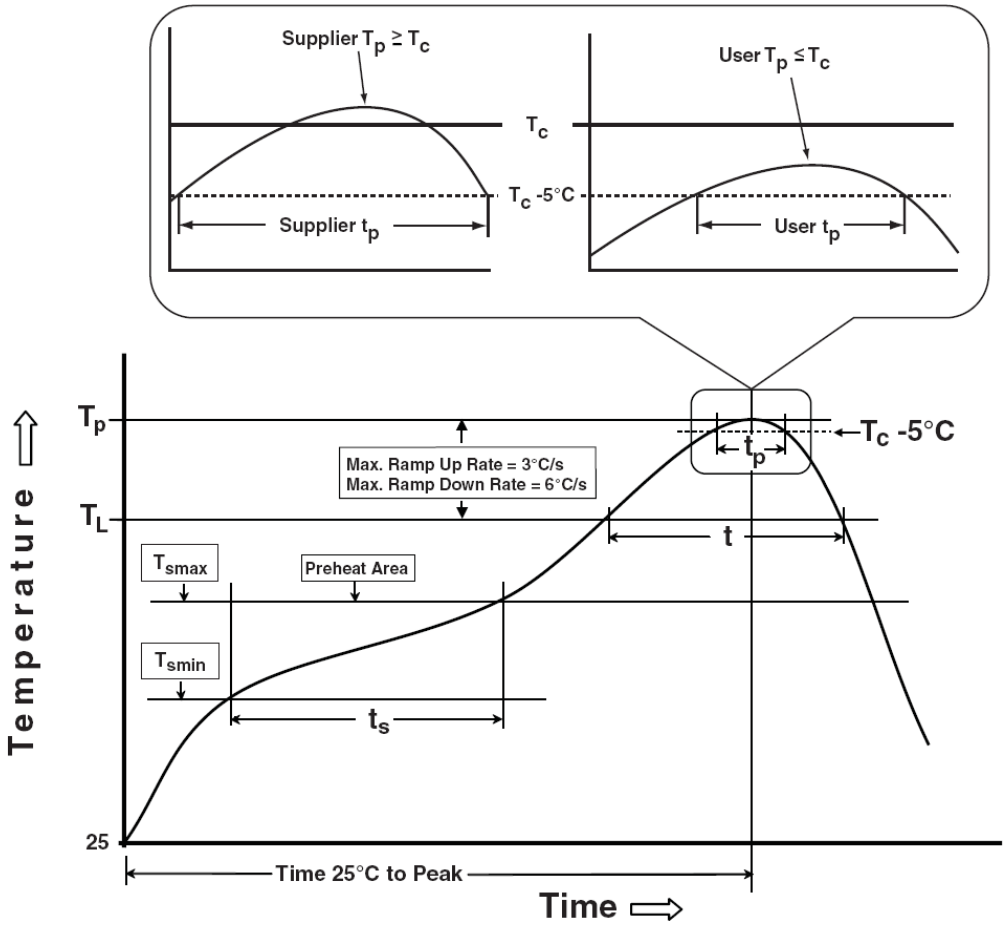
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Taping Direction Information

TQFN2x2



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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