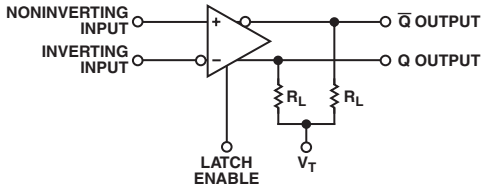
Ultrafast Comparators

AD96685/AD96687

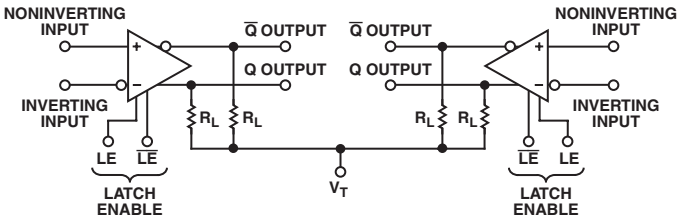
FEATURES
Fast: 2.5 ns Propagation Delay
Low Power: 118 mW per Comparator
Packages: DIP, SOIC, PLCC
Power Supplies: +5 V, –5.2 V
Logic Compatibility: ECL
50 ps Delay Dispersion

APPLICATIONS
High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω-200Ω CONNECTED TO –2.0V, OR 200Ω-2000Ω

GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5 ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50 ps propagation delay dispersion which is a particularly important characteristic of high-speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from –2.5 V to +5 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to –2 V. A level sensitive latch input which permits tracking, track-hold, or sample-hold modes of operation is included.

The AD96685 is available in industrial –25°C to +85°C range in 16-pin SOIC.

The AD96687 is available in industrial range –25°C to +85°C, in 16-pin DIP, SOIC, and 20-lead PLCC.

REV. D

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AD96685/AD96687–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Positive Supply Voltage = 5.0 V; Negative Supply Voltage = –5.2 V, unless otherwise noted.)

Parameter	Temp	Test Level	Industrial Temperature Range –25°C to +85°C						Unit
			AD96685BR			AD96687BQ/BP/BR			
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Input Offset Voltage	25°C	I		1	2		1	2	mV
	Full	VI			3			3	mV
Input Offset Drift	Full	V		20			20		µV/°C
Input Bias Current	25°C	I		7	10		7	10	µA
	Full	VI			13			13	µA
Input Offset Current	25°C	I		0.1	1.0		0.1	1.0	µA
	Full	VI			1.2			1.2	µA
Input Resistance	25°C	V		200			200		kΩ
Input Capacitance	25°C	V		2			2		pF
Input Voltage Ranges[2]	Full	VI	–2.5		+5.0	–2.5		+5.0	V
Common-Mode Rejection Ratio	Full	VI	80	90		80	90		dB
ENABLE INPUT									
Logic "1" Voltage	Full	VI	–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5	V
Logic "1" Current	Full	VI			40			40	µA
Logic "0" Current	Full	VI			5			5	µA
DIGITAL OUTPUTS[3]									
Logic "1" Voltage	Full	VI	–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5	V
SWITCHING PERFORMANCES									
Propagation Delays[4]									
Input to Output HIGH	25°C	IV		2.5	3.5		2.5	3.5	ns
Input to Output LOW	25°C	IV		2.5	3.5		2.5	3.5	ns
Latch Enable to Output HIGH	25°C	IV		2.5	3.5		2.5	3.5	ns
Latch Enable to Output LOW	25°C	IV		2.5	3.5		2.5	3.5	ns
Dispersions[5]	25°C	V		50			50		ps
Latch Enable									
Minimum Pulsewidth	25°C	IV		2.0	3.0		2.0	3.0	ns
Minimum Setup Time	25°C	IV		0.5	1.0		0.5	1.0	ns
Minimum Hold Time	25°C	IV		0.5	1.0		0.5	1.0	ns
POWER SUPPLY[6]									
Positive Supply Current (+5.0 V)	Full	VI		8	9		15	18	mA
Negative Supply Current (–5.2 V)	Full	VI		15	18		31	36	mA
Power Supply Rejection Ratio[7]	Full	VI	60	70		60	70		dB

NOTES
[1]R_S = 100 Ω.
[2]Input Voltage Range can be extended to –3.3 V if $-V_S$ = –6.0 V.
[3]Outputs terminated through 50 Ω to –2.0 V.
[4]Propagation delays measured with 100 mV pulse (10 mV overdrive) to 50% transition point of the output.
[5]Change in propagation delay from 100 mV to 1 V input overdrive.
[6]Supply voltages should remain stable within ±5% for normal operation.
[7]Measured at ±5% of $+V_S$ and $-V_S$.

Specifications subject to change without notice.

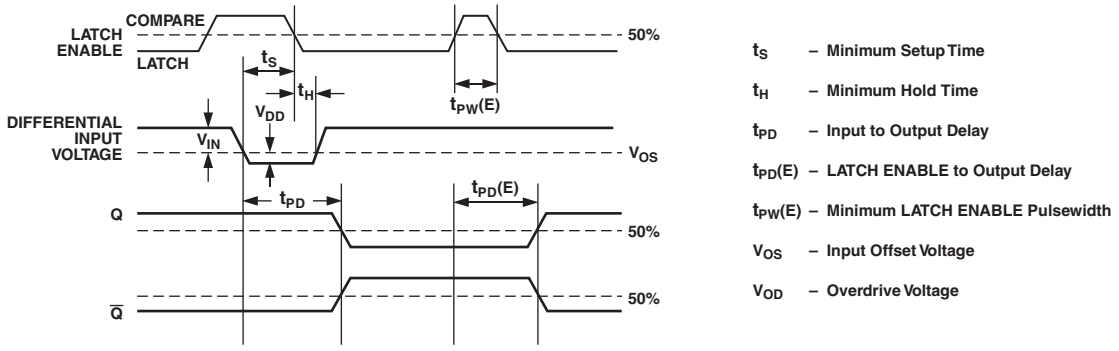


Figure 1. System Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . 6.5 V
Negative Supply Voltage ($-V_S$) . . . . . –6.5 V
Input Voltage Range[2] . . . . . ±5 V
Differential Input Voltage . . . . . 5.5 V
Latch Enable Voltage . . . . . $-V_S$ to 0 V
Output Current . . . . . 30 mA
Operating Temperature Range[3]
AD96685BR/AD96687BQ/BR/BP . . . . . –25°C to +85°C
Storage Temperature Range . . . . . –55°C to +150°C
Junction Temperature . . . . . 175°C
Lead Soldering Temperature (10 sec) . . . . . 300°C

NOTES

[1]Absolute maximum ratings are limiting values, may be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Under no circumstances should the input voltages exceed the supply voltages.

[3]Typical thermal impedances . . .

AD96685 SOIC	q_{JA} = 170°C/W; q_{JC} = 60°C/W
AD96687 Ceramic	q_{JA} = 115°C/W; q_{JC} = 57°C/W
AD96687 SOIC	q_{JA} = 92°C/W; q_{JC} = 47°C/W
AD96687 PLCC	q_{JA} = 81°C/W; q_{JC} = 45°C/W

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at 25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

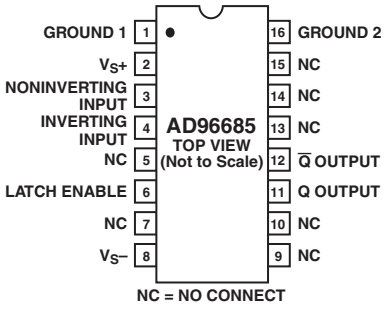
VI – All devices are 100% production tested at 25°C; 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

FUNCTIONAL DESCRIPTION

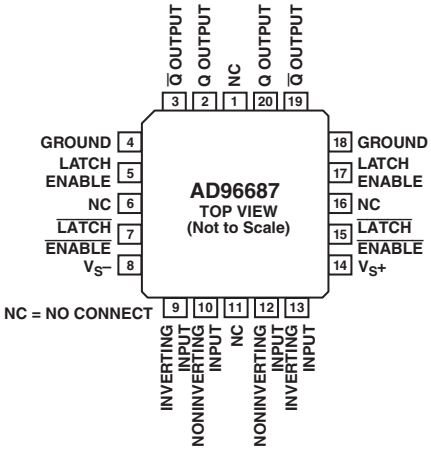
Pin Name	Description
$+V_S$	Positive supply terminal, nominally 5.0 V.
NONINVERTING INPUT	Noninverting analog input of the differential input stage. The NONINVERTING INPUT must be driven in conjunction with the INVERTING INPUT.
INVERTING INPUT	Inverting analog input of the differential input stage. The INVERTING INPUT must be driven in conjunction with the NONINVERTING INPUT.
LATCH ENABLE	In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. $\overline{\text{LATCH ENABLE}}$ must be driven in conjunction with LATCH ENABLE for the AD96687.
$\overline{\text{LATCH ENABLE}}$	In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LATCH ENABLE must be driven in conjunction with $\overline{\text{LATCH ENABLE}}$ for the AD96687.
$-V_S$	Negative supply terminal, nominally –5.2 V.
Q	One of two complementary outputs. Q will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and LATCH ENABLE (AD96687 only) for additional information.
$\overline{Q}$	One of two complementary outputs. $\overline{Q}$ will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE and LATCH ENABLE (AD96687 only) for additional information.
GROUND 1	One of two grounds, but primarily associated with the digital ground. Both grounds should be connected together near the comparator.
GROUND 2	One of two grounds, but primarily associated with the analog ground. Both grounds should be connected together near the comparator.

PIN CONFIGURATIONS

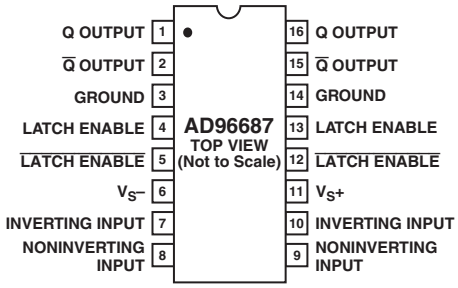
AD96685BR



AD96687BP



AD96687BQ/BR



ORDERING GUIDE

Model	Type	Temperature Range	Description	Package Options
AD96685BR	Single	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A
AD96687BP	Dual	–25°C to +85°C	20-Pin PLCC, Industrial	P-20A
AD96687BQ	Dual	–25°C to +85°C	16-Pin DIP, Industrial	Q-16
AD96687BR	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A
AD96687BR-REEL	Dual	–25°C to +85°C	16-Pin SOIC, Industrial	R-16A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD96685/AD96687 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



APPLICATIONS INFORMATION

The AD96685/AD96687 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD96685/AD96687 design is the use of a low impedance ground plane.

Another area of particular importance is power supply decoupling. Normally, both power supply connections should be separately decoupled to ground through 0.1 μF ceramic and 0.001 μF mica capacitors. The basic design of comparator circuits makes the negative supply somewhat more sensitive to variations. As a result, more attention should be placed on ensuring a "clean" negative supply.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The $\overline{\text{LATCH ENABLE}}$ input of the AD96687 should be tied to –2.0 V or left "floating," to disable the latching function. An alternate use of the LATCH ENABLE input is as a hysteresis control input. By varying the voltage at the LATCH ENABLE input for the AD96685 and the differential voltage between both latch inputs for the AD96687, small variations in the hysteresis can be achieved.

Occasionally, one of the two comparator stages within the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float." The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by ensuring that the two inputs are at least one diode drop apart, while also grounding the LATCH ENABLE input.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD96685/AD96687 are designed to be terminated through 50 Ω resistors to –2.0 V, or any other equivalent ECL termination. If high speed ECL signals must be routed more than a few centimeters, MicroStrip or StripLine techniques may be required to ensure proper transition times and prevent output ringing.

The AD96685/AD96687 have been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1 V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD96685/AD96687 are far less sensitive to input variations than most comparator designs.

Typical Applications

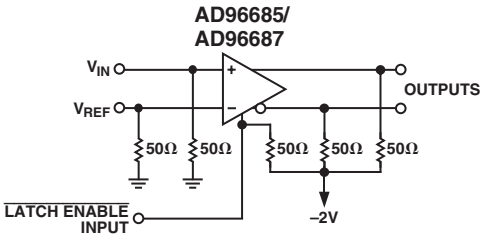


Figure 2. High Speed Sampling Circuit

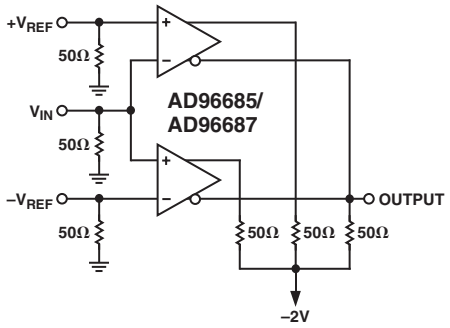
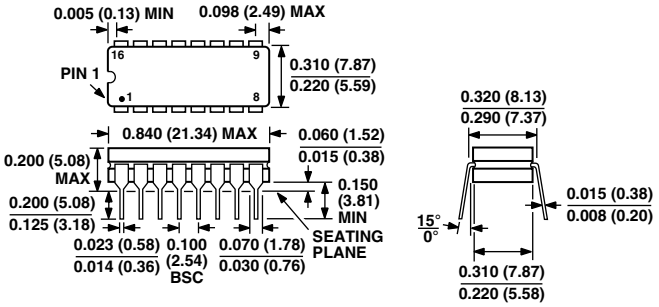


Figure 3. High Speed Window Comparator

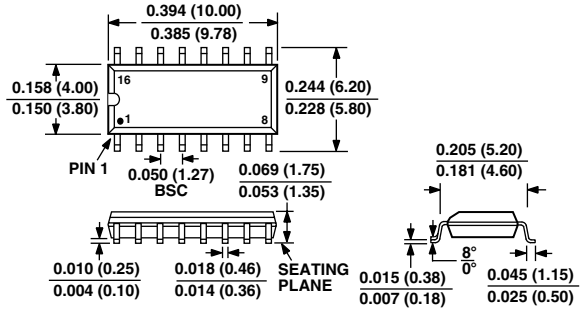
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

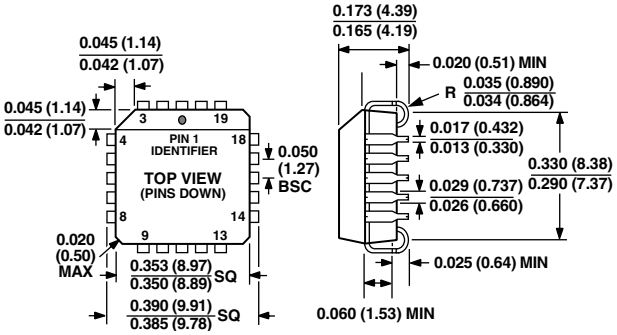
16-Lead Ceramic DIP



16-Lead SOIC



20-Lead PLCC



Revision History

Location	Page

Data Sheet changed from REV. C to REV. D.

Edits to FEATURES 1
Edits to GENERAL DESCRIPTION 1
Edits to ELECTRICAL CHARACTERISTICS 2
Edits to ABSOLUTE MAXIMUM RATINGS 3
Edits to ORDERING GUIDE 4
Deleted DIE LAYOUT AND MECHANICAL INFORMATION 4
Edits to OUTLINE DIMENSIONS 8

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