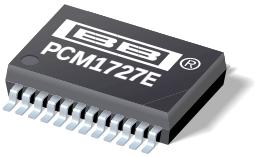
BURR - BROWN®



PCM1727

SoundPLUS™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER WITH PROGRAMMABLE DUAL PLL

FEATURES

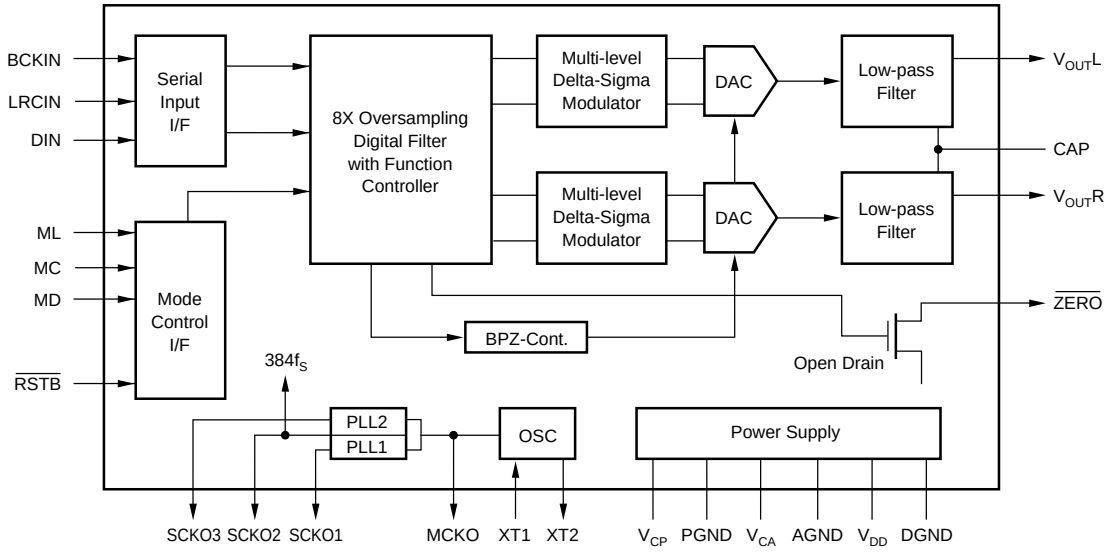
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 92dB
- MULTIPLE SAMPLING FREQUENCIES: f_S = 44.1kHz, 48kHz, 96kHz
- PROGRAMMABLE DUAL PLL CIRCUIT: 27MHz Master Clock Input
- GENERATED SYSTEM CLOCK
  - SCKO1: 33.8688MHz
  - SCK02: $384f_S$
  - SCK03: $768f_S$ (44.1k/48kHz)
    $384f_S$ (96kHz)
- NORMAL OR I^2S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute, Analog Output Mode
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- +5V SINGLE POWER SUPPLY

DESCRIPTION

The PCM1727 is a complete low cost stereo audio digital-to-analog converter (DAC) with a dual phase-locked loop (PLL) circuit included. PLL-1 derives a fixed 33.8688MHz ($768f_S$, f_S = 44.1kHz) system clock (SCKO-1), and PLL-2 derives both the $384f_S$ (f_S = 44.1k/48k/96kHz) system clock (SCKO-2), and the $768f_S$ (f_S = 44.1k/48kHz)/$384f_S$ (f_S = 96kHz) system clock (SCKO-3) from an external 27MHz reference frequency. The DAC contains a 3rd-order ΔΣ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1727 can accept 16-, 20-, or 24-bit input data in either normal or I^2S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis.

The PCM1727 is ideal for applications which combine compressed audio and video data such as DVD, DVD Audio with CD-DA compatibility, karaoke DSP.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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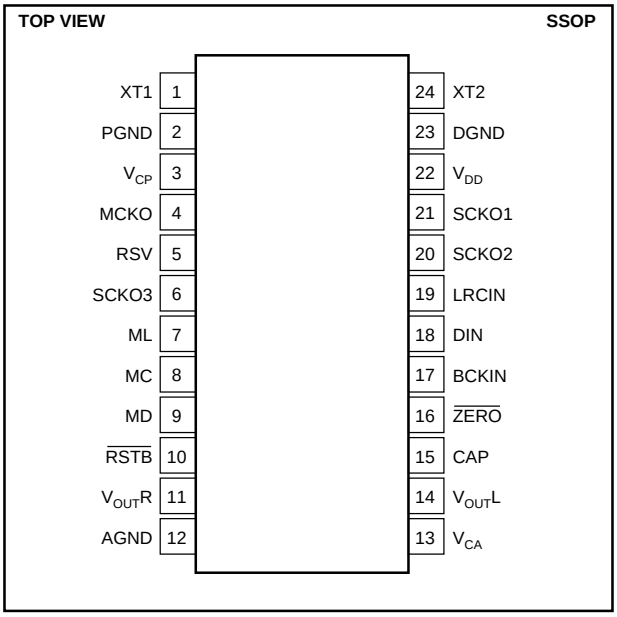
SPECIFICATIONS

All specifications at +25°C, $+V_{CA} = +V_{DD} = +V_{CP} = +5V$, f_S = 44.1kHz, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1727 MIN	PCM1727 TYP	PCM1727 MAX	UNITS
RESOLUTION		16			Bits
DATA FORMAT					
Audio Data Interface Format			Standard/I^2S		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB First, 2's Comp		Selectable
Sampling Frequency (f_S)		44.1		96	kHz
PLL PERFORMANCE					
Master Clock Input Frequency(4)		26.73	27	27.27	MHz
Generated System Clock					
SCKO-1	$768f_S$ (f_S = 44.1k)		33.8688		MHz
SCKO-2	$384f_S$	16.9344		36.8640	MHz
SCKO-3	$768f_S$ (f_S = 44.1k/48k), $384f_S$ (f_S = 96k)	33.8688		36.8640	MHz
Output Logic Level V_{OH}	I_{OH} = 2mA	V_{DD} – 0.4			VDC
(MCKO, SCKO 1 ~ 3) V_{OL}	I_{OL} = 4mA			0.5	VDC
Generated Sysclk Jitter	Standard Dev		±150		ps
Generated Sysclk Transient(1)	f_M = 27MHz			20	ms
Power-Up Time	To Programmed Frequency		15	30	ms
Generated Sysclk Duty Cycle	f_M = 27MHz, C_L = 15pF	40	50	60	%
DIGITAL INPUT LOGIC LEVEL			TTL		
DYNAMIC PERFORMANCE(2)					
THD+N at f_S (0dB)	fs = 44.1kHz		–89	–80	dB
	fs = 96kHz		–87		dB
THD+N at –60dB	fs = 44.1kHz		–31		dB
	fs = 96kHz		–29		dB
Dynamic Range (EIAJ Method)	fs = 44.1kHz	90	92		dB
	fs = 96kHz		90		dB
Signal-to-Noise Ratio(3) (EIAJ Method)	fs = 44.1kHz	90	94		dB
	fs = 96kHz		90		dB
Channel Separation	fs = 44.1kHz	88	93		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±2.0	% of FSR
Bipolar Zero Error	$V_{OUT} = V_{CC}/2$ at BPZ		±30		mV
ANALOG OUTPUT					
Output Voltage	Full Scale (–0dB)		0.62 x V_{CA}		Vp-p
Center Voltage			$V_{CA}/2$		V_{DC}
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445	f_S
Stopband		0.555			f_S
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			$11.125/f_S$		sec
De-emphasis Error		–0.2		+0.55	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	$V_{CC} = V_{DD} = V_{CP}$	4.5	5	5.5	VDC
Supply Current: $I_{CC} + I_{DD} + I_{CP}$	f_S = 44.1kHz		25	27	mA
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (3) SNR is tested at Infinite Zero Detection off. (4) PLL evaluations tested with 1ns maximum jitter on the 27MHz input clock.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM1727E	24-Pin SSOP	338

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Input Current (except power supply)	±10mA
Power Dissipation	300mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	XT1	IN	27MHz Crystal or External Clock Input
2	PGND	—	PLL Ground
3	V_{CP}	—	PLL Power Supply (+5V)
4	MCKO	OUT	Buffered Clock Output of Crystal Oscillator
5	RSV	—	Reserve; This pin should be open.
6	SCKO3	OUT	System Clock Out 3; This output is $768f_S$ or $384f_S$.
7	ML	IN	Latch Enable Input for Serial Interface Mode[2]
8	MC	IN	Bit Clock Input for Serial Interface Mode[2]
9	MD	IN	Serial Data Input for Serial Interface Mode[2]
10	$\overline{RSTB}$	IN	Reset; When this pin is low, the DF and modulator are held in reset.
11	$V_{OUT}R$	OUT	Right Channel, Analog Voltage Output of Audio Signal
12	AGND	—	Analog Ground
13	V_{CA}	—	Analog Power Supply (+5V)
14	$V_{OUT}L$	OUT	Left Channel, Analog Voltage Output of Audio Signal
15	CAP	—	Common Pin of Analog Output Amp
16	$\overline{ZERO}$	OUT	Zero Data Flag; This pin is low when the input data is continuously zero for more than 65,535 cycles of BCKIN[1].
17	BCKIN	IN	Bit Clock Input for Serial Audio Data[3]
18	DIN	IN	Serial Audio Data Input[3]
19	LRCIN	IN	Left and Right Clock (sampling rate–f_S)[3]
20	SCKO2	OUT	System Clock Out 2; This output is $256f_S$ or $384f_S$ system clock.
21	SCKO1	OUT	System Clock Out 1; This output is 33.8688MHz system clock.
22	V_{DD}	—	Digital Power (+5V)
23	DGND	—	Digital Ground
24	XT2	—	27MHz Crystal. Connected to GND at external clock.

Note: (1) Open Drain Output. (2) Schmitt triger input with internal pull-up resistors. (3) Schmitt triger input.

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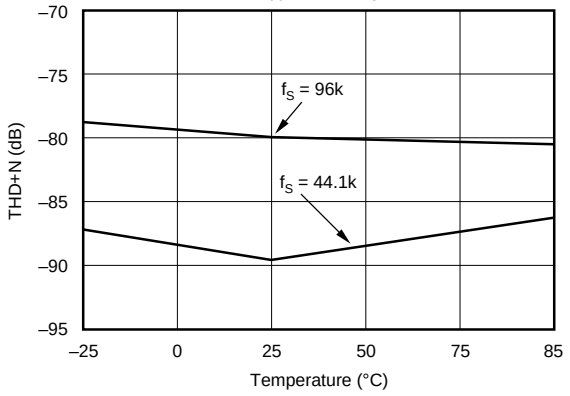
TYPICAL PERFORMANCE CURVES

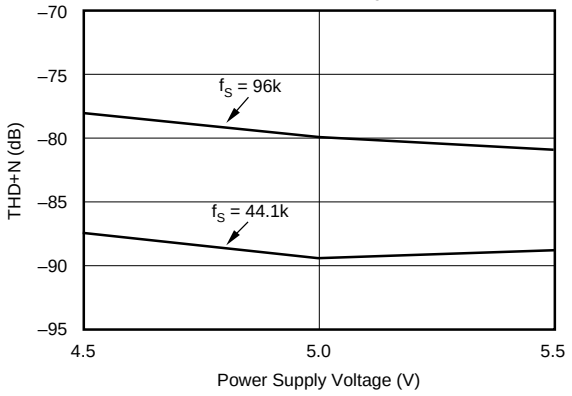
At T_A = +25°C, V_{CC} = V_{DD} = V_{CP} = +5V, f_S = 44.1kHz, 16-bit input data, 384f_S, unless otherwise noted. Measurement bandwidth is 20kHz.

DYNAMIC PERFORMANCE

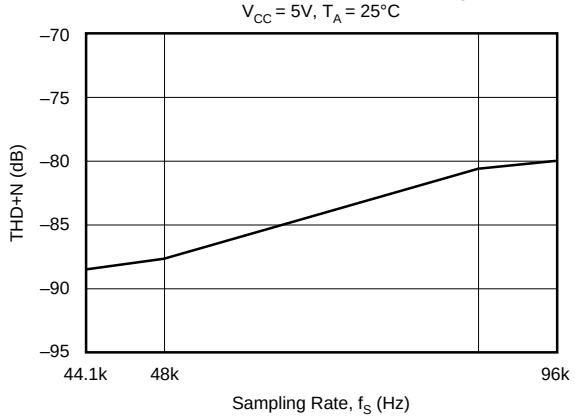
THD+N (0dB) vs TEMPERATURE and
V_{CC} = 5V, 384f_S



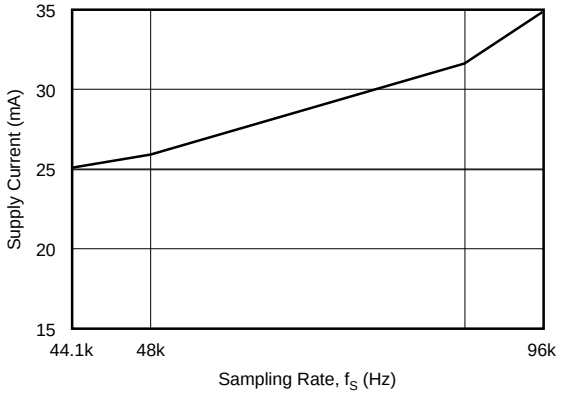
THD+N (0dB) vs POWER SUPPLY VOLTAGE
T_A = 25°C, 384f_S



THD+N (0dB) vs SAMPLING RATE (f_S)
V_{CC} = 5V, T_A = 25°C

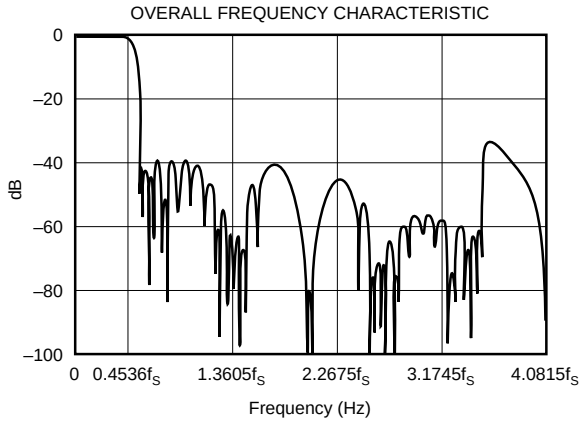


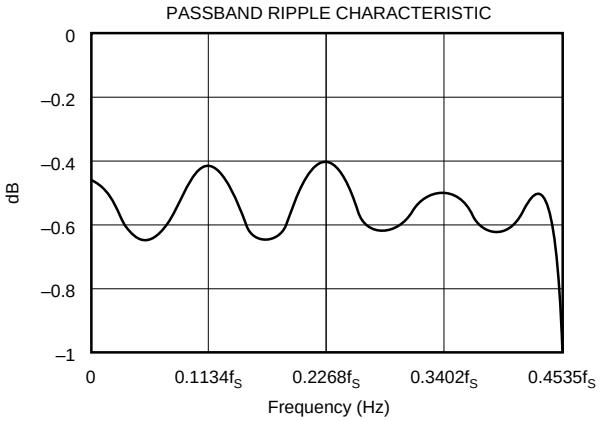
POWER SUPPLY CURRENT vs SAMPLING RATE (f_S)
V_{CC} = 5V, T_A = 25°C

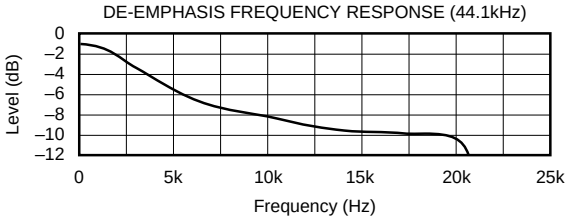


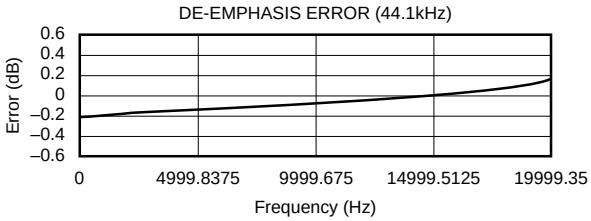
TYPICAL PERFORMANCE CURVES

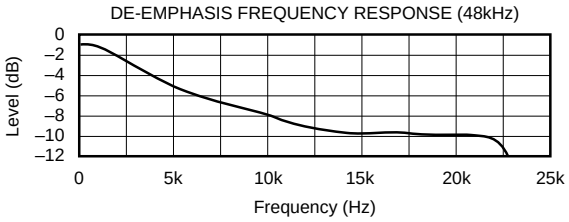
DIGITAL FILTER

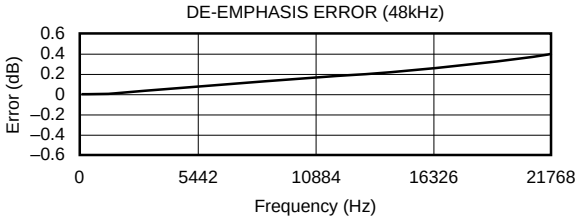












TYPICAL CONNECTION DIAGRAM

Figure 1 illustrates the typical connection diagram for PCM1727 in an DVD Audio application. The 27MHz master video clock (f_M) drives XT1 (pin 1) of PCM1727. A programmable system clock is generated by the PCM1727 PLL, with SCKO2 used to drive the MPEG2 decoder's system clock input. SCKO1 used to drive the CD-DA DSP's system clock input, SCKO3 used to drive Karaoke DSP's system clock input. The standard audio signals (data, bit clock, and word clock) are generated in the decoder from PCM1727's system clock, providing synchronization of audio and video signals.

DUAL PLL CIRCUIT

PCM1727 has a programmable internal DUAL PLL circuit, as shown in Figure 2. The PLL is designed to accept a 27MHz master clock or crystal oscillator and generate all internal system clocks required to operate the digital filter and ΔΣ modulator, at $384f_S$. If an external master clock is used, XT2 should be connected to ground. The PLL will directly track any variations in the master clock's frequency, and jitter on the system clock is specified at 150ps typical. Figure 3 illustrates the timing requirements for the 27MHz master clock. Figure 4 illustrates the system clock connections for an external clock or crystal oscillator.

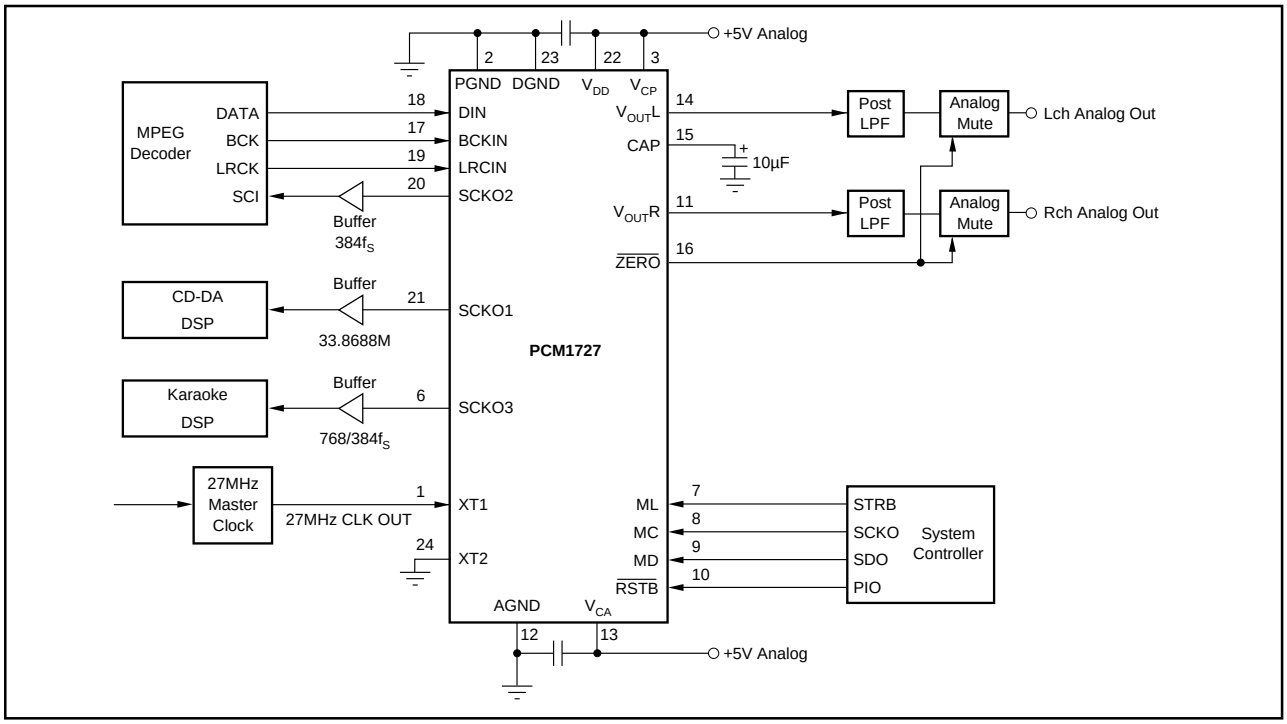


FIGURE 1. Connection Diagram for External Master Clock in a Typical MPEG2 Application.

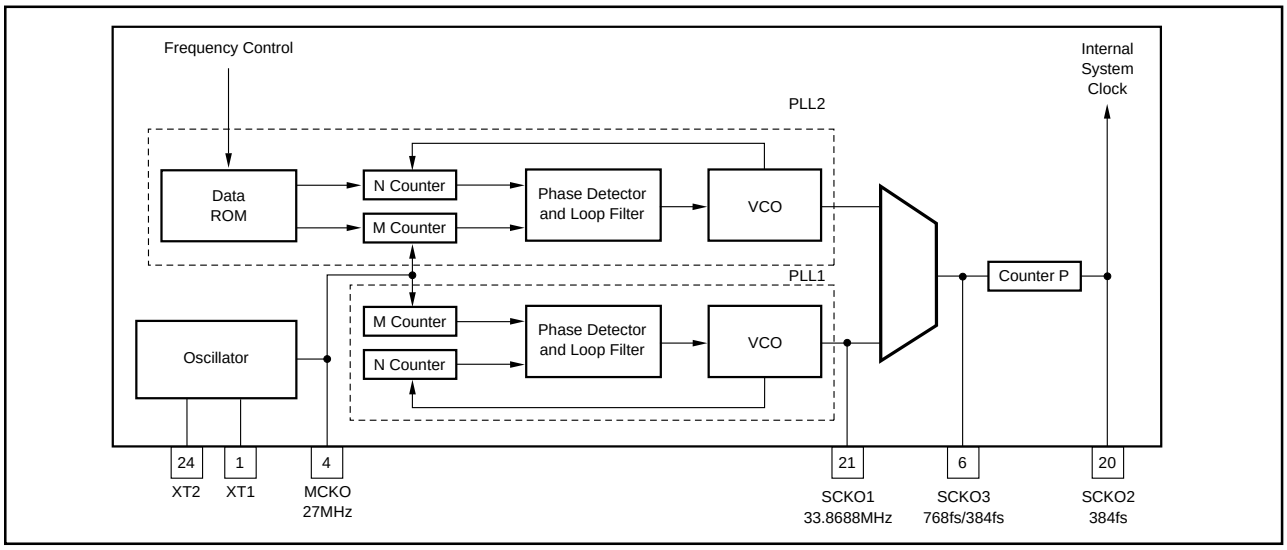


FIGURE 2. PLL Block Diagram.

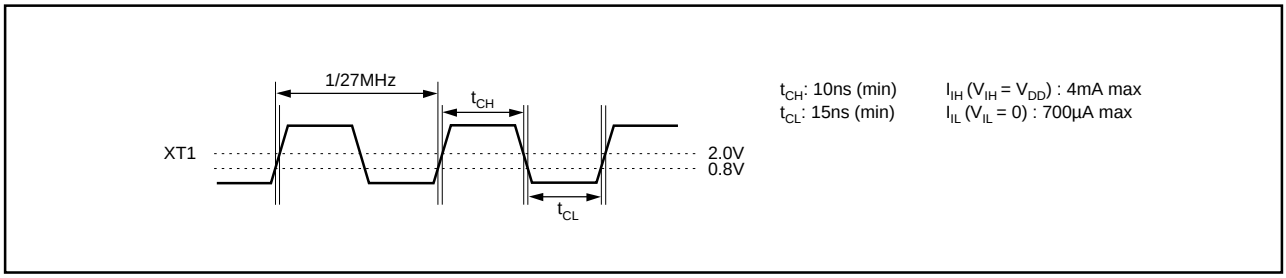


FIGURE 3. XT1 Input Timing.

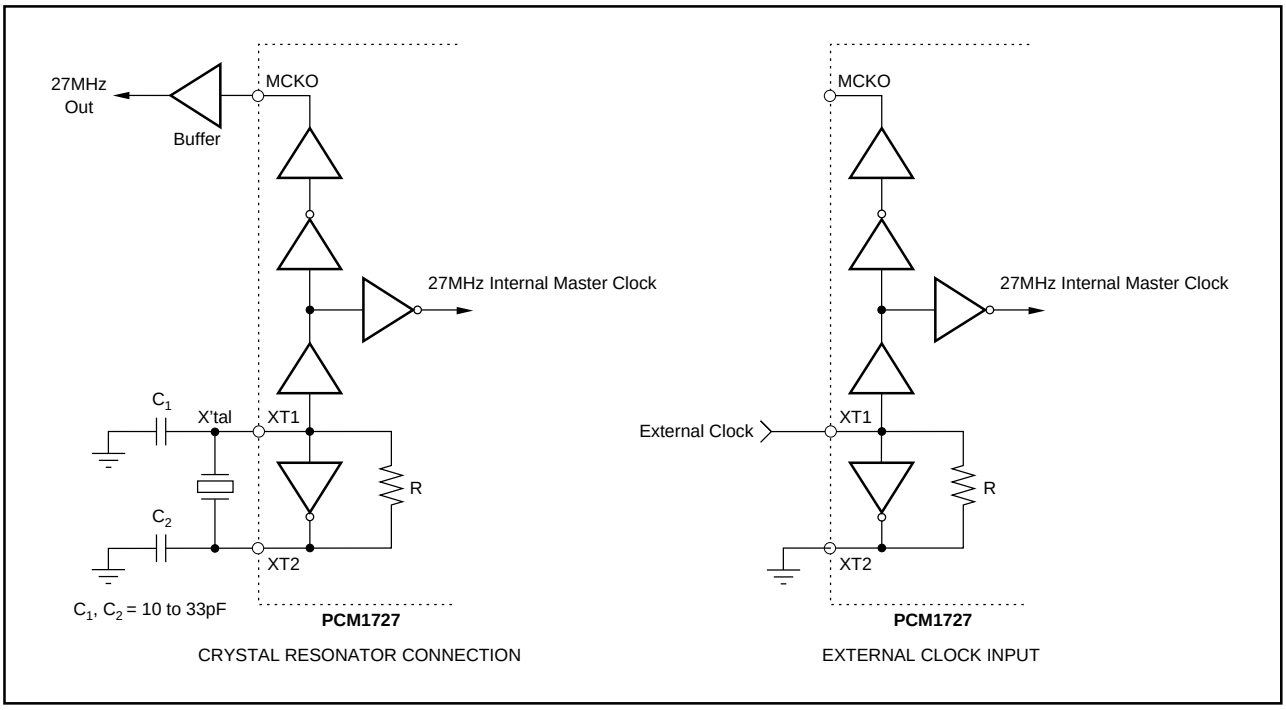


FIGURE 4. System Clock Connection.

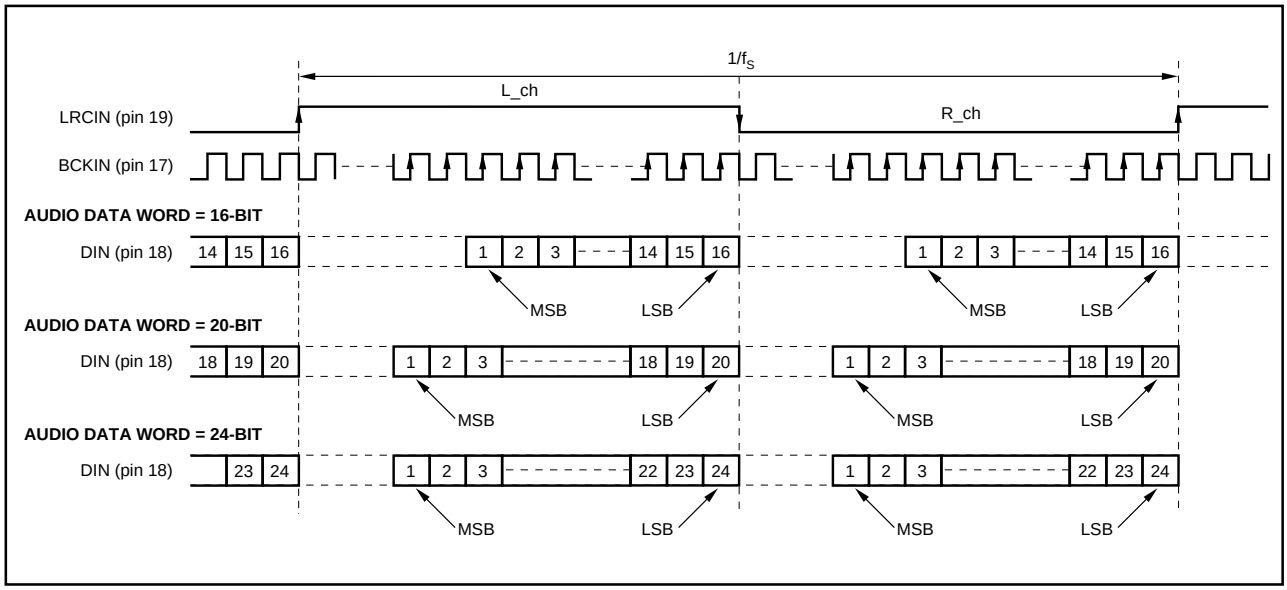


FIGURE 5. “Normal” Data Input Timing.

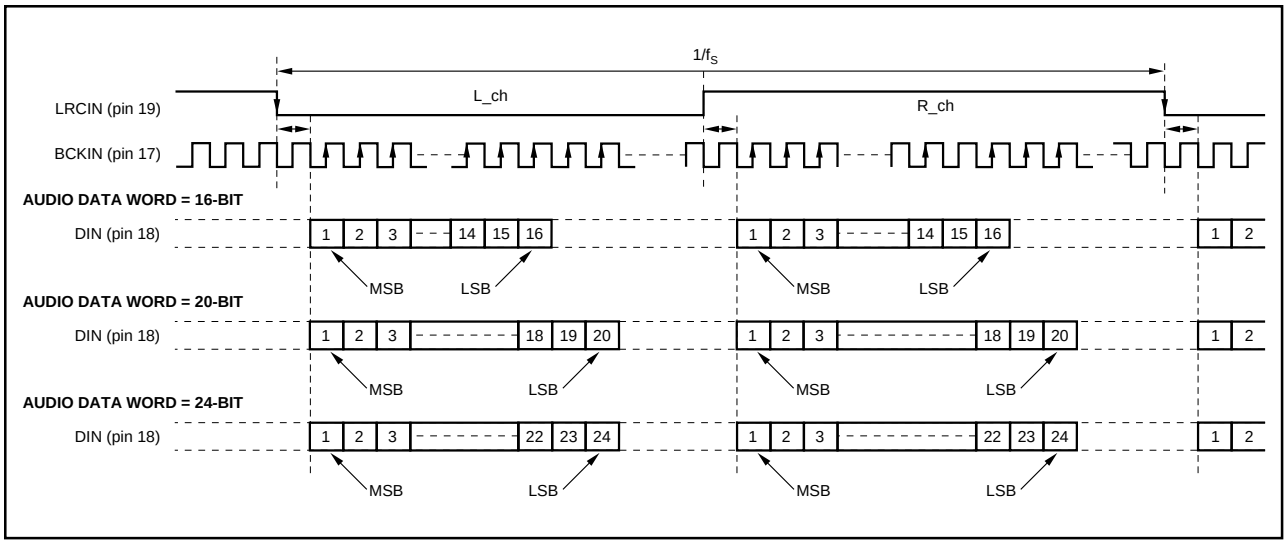
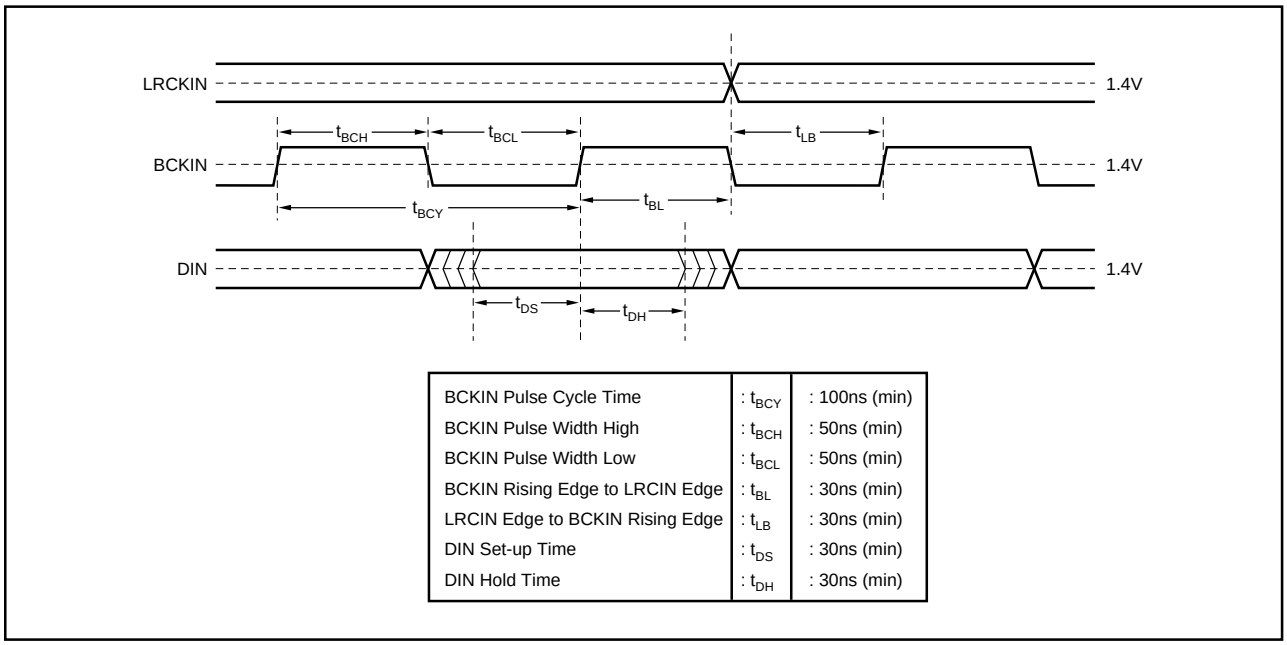


FIGURE 6. "I²S" Data Input Timing.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 7. Audio Data Input Timing.

PCM1727's internal PLL can be programmed for three different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II. The system clock output frequency for PCM1727 is 100% accurate.

Frequency error of generated system clock by programmed PLL is less than ±0.03ppm due to high accuracy PLL construction.

To provide MCKO clock and SCKO1, SCKO2, SCKO3 clocks for external circuits, an external buffer may be used to avoid degrading audio performance (as shown in the connection diagram, in Figure 1).

	Sampling Frequencies-LRCIN (kHz)		
Standard Sampling Freq		44.1	48
Double of Standard Sampling Freq			96

TABLE I. Sampling Frequencies.

Sampling Frequency (LRCIN)		SCKO2 System Clock	SCKO3 System Clock
44.1kHz	Standard	16.9344MHz	33.8688MHz
48kHz	Standard	18.4320MHz	36.8640MHz
96kHz	Double	36.8640MHz	36.8640MHz

TABLE II. Sampling Frequencies vs Internal System Clock (= Output Frequencies of Dual PLL).

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	res	ATC	LRP	I^2S

SPECIAL FUNCTIONS

PCM1727 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 9) is used for the program data, MC (pin 8) is used to clock in the program data, and ML (pin 7) is used to latch in the program data. Table III lists the selectable special functions.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Normal Format I^2S Format	Normal Format
Input Audio Data Bit Selection 16/20/24 Bits	16 Bits
Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High	Lch/Rch = High/Low
De-emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB Lch, Rch Individually Fixed
Infinite Zero Detection Circuit Control	OFF
Operation Enable (OPE)	Enabled
Sampling Rate Selection Standard Sampling Rate—44.1/48kHz Double Sampling Rate—96kHz Sampling Frequency 44.1kHz Group 48kHz Group	Standard Sampling Rate 44.1kHz
Analog Output Mode L, R, Mono, Mute	Stereo

TABLE III. Selectable Functions.

PROGRAM REGISTER BIT MAPPING

PCM1727's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 8 illustrates the serial interface timing.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0) LDL A (1:0) Res	DAC Attenuation Data for Lch Attenuation Data Load Control for Lch Register Address Reserved, should be "L"
Register 1	AR (7:0) LDL A (1:0) Res	DAC Attenuation Data for Rch Attenuation Data Load Control for Rch Register Address Reserved, should be "L"
Register 2	MUT DEM OPE IW (1:0) PL (3:0) A (1:0) res	Left and Right DACs Soft Mute Control De-emphasis Control Left and Right DACs Operation Control Input Audio Data Bit Select Output Mode Select Register Address Reserved, should be "L"
Register 3	I^2S LRP ATC DSR (1:0) SF (1:0) IZD A (1:0) Res	Audio Data Format Select Polarity of LRCIN (pin 19) Select Attenuator Control Double Sampling Rate Select Sampling Rate Select Infinite Zero Detection Circuit Control Register Address Reserved, should be "L"

TABLE IV. Internal Register Mapping.

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

$$ATT = [20 \log10 (ATT_DATA/255)] \text{ dB}$$

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

Attenuation Level (ATT) can be controlled as following Resistor set AL (R) (7:0).

AL (R) (7:0)	ATT LEVEL
00h	–∞dB (Mute)
01h	–48.16dB
.	.
.	.
.	.
FEh	–0.07dB
FFh	0dB

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a “HIGH” level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no “click” is audible). Bit 1 is used to control de-emphasis. A “LOW” level on bit 1 disables de-emphasis, while a “HIGH” level enables de-emphasis.

Bit 2, (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled

TABLE V. Operation Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is “LOW”, the DAC will convert all non-zero input data. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be forced to zero only if IZD is “HIGH”. When OPE is “HIGH”, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

TABLE VI. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = “HIGH”	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = “LOW”	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

TABLE VII. Reset (RSTB) Function.

NOTE: (1) ΔΣ is disconnected from output amplifier. (2) ΔΣ is connected to output amplifier.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1727 can be set up for input word resolutions of 16, 20, or 24 bits:

Bit 4 (IW1)	Bit 3 (IW0)	Input Resolution
0	0	16-bit Data Word
0	1	20-bit Data Word
1	0	24-bit Data Word
1	1	Reserved

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1727 can be programmed for 16 different states, as shown in Table VIII.

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE VIII. Programmable Output Format.

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	YES	ATC	LRP	I^2S

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency and infinite zero detection.

Bits 0 (I^2S) and 1 (LRP) are used to control the input data format. A “LOW” on bit 0 sets the format to “Normal” (MSB-first, right-justified Japanese format) and a “HIGH” sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is “LOW”, left channel data is assumed

when LRCIN is in a “HIGH” phase and right channel data is assumed when LRCIN is in a “LOW” phase. When bit 1 is “HIGH”, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is “HIGH”, the attenuation data loaded in program Register 0 is used for both left and right channels. When bit 2 is “LOW”, the attenuation data for each register is applied separately to left and right channels.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

DSR1	DSR0	Multiple	
0	0	Normal	44.1/48kHz
0	1	Double	96kHz
1	0	Reserved	Reserved
1	1	Reserved	Reserved

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency:

SF1	SF0	Sampling Frequency	
0	0	44.1kHz group	44.1kHz
0	1	48kHz group	48/96kHz
1	0	Reserved	Reserved
1	1	Reserved	Reserved

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is “LOW”, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is “HIGH”, the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1727 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

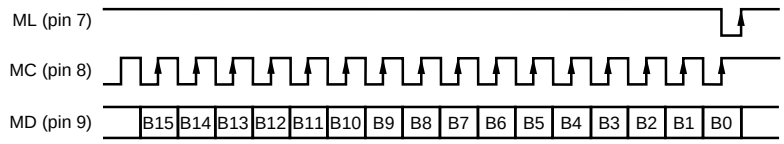
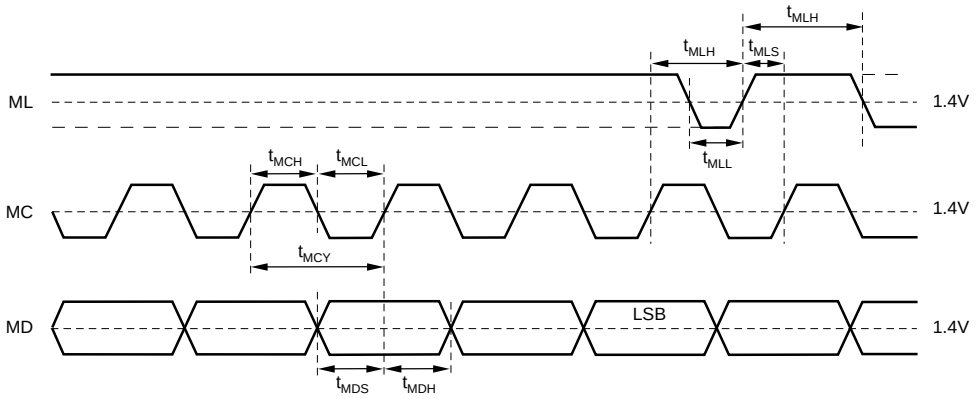


FIGURE 8. Three-Wire Serial Interface.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC Pulse Width LOW	t_{MCL}	40ns (min)
MC Pulse Width HIGH	t_{MCH}	40ns (min)
MD Setup Time	t_{MDS}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
ML Low Level Time	t_{MLL}	40ns + 1SYSCLK (min)
ML High Level Time	t_{MLH}	40ns + 1SYSCLK (min)
ML Setup Time	t_{MLS}	40ns (min)
ML Hold Time	t_{MLH}	40ns (min)
SYSCLK: $1/384f_S$		

FIGURE 9. Program Register Input Timing.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1727:

$$T_D = 11.125 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, DVD audio, Video CD, DAT, Minidisc, etc., generally are not affected by delay time.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1727 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 10. The higher frequency rolloff of the filter is shown in Figure 11. If the user's application has the PCM1727 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 12. For some applications, a passive RC filter or 2nd-order filter may be adequate.

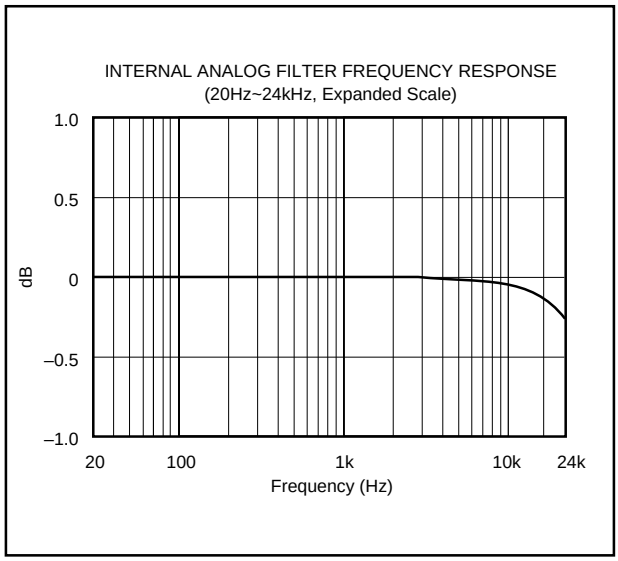


FIGURE 10. Low Pass Filter Frequency Response.

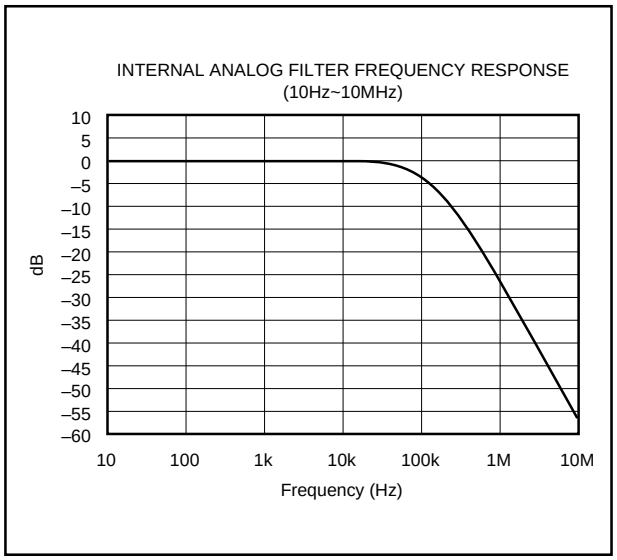


FIGURE 11. Low Pass Filter Wideband Frequency Response.

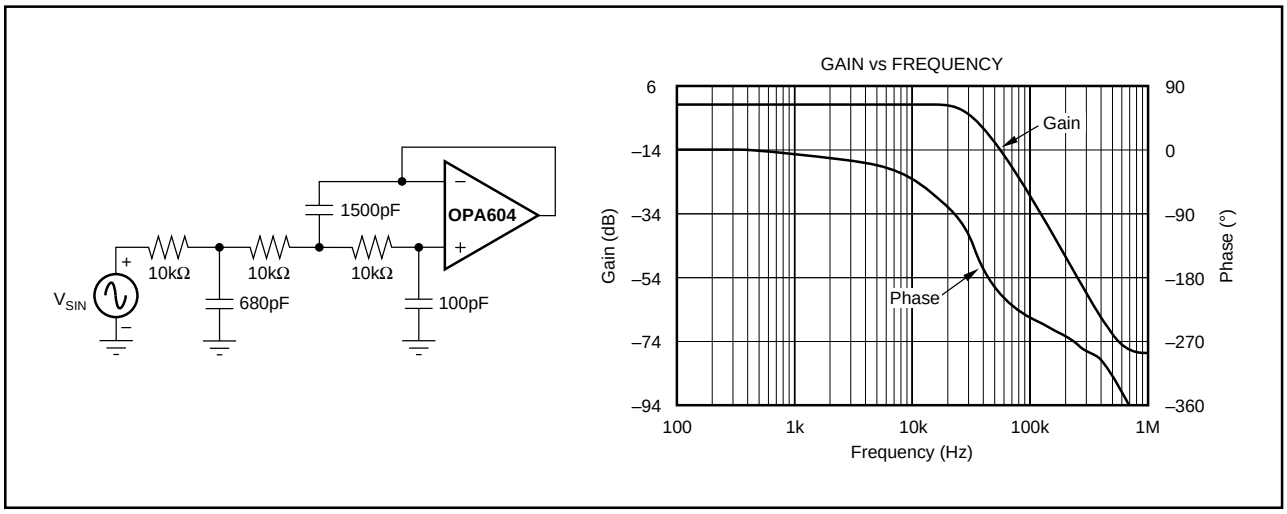


FIGURE 12. 3rd-Order LPF.

Reset

PCM1727 has both internal power-on reset circuit and the $\overline{RSTB}$ pin (pin 10) which accepts an external forced reset by $\overline{RSTB}$ = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 13 illustrates the timing of the internal power on reset.

PCM1727 accepts an external forced reset when $\overline{RSTB}$ = L. When $\overline{RSTB}$ = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RSTB}$ = H.) Figure 14 illustrates the timing of the $\overline{RSTB}$ reset pin.

For system applications, the power-up time of the internal PLL circuit to provide a stable system clock output, is approximately 1024 system clocks plus a 15ms transient time.

POWER SUPPLY CONNECTIONS

PCM1727 has three power supply connections: digital (V_{DD}), analog (V_{CA}), and PLL (V_{CP}). Each connection also has a separate ground return pin. It is acceptable to use a common +5V power supply for all three power pins. If separate supplies are used without a common connection, the delta between the supplies during ramp-up time must be less than 0.3V. An application circuit to avoid a power-on latch-up condition is shown in Figure 15.

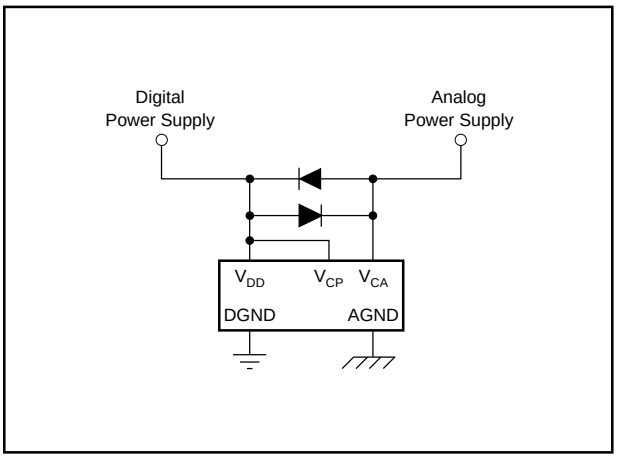


FIGURE 15. Latch-up Prevention Circuit.

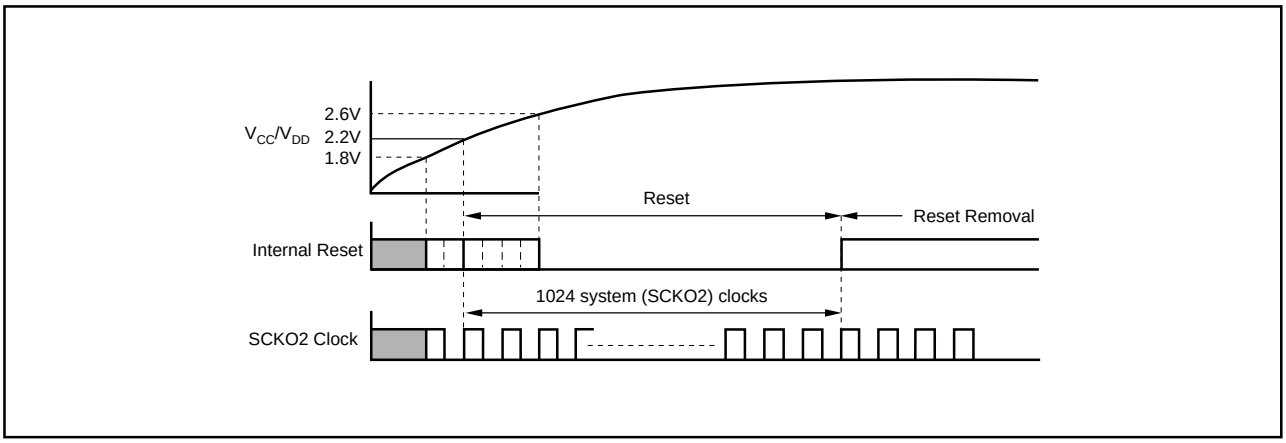


FIGURE 13. Internal Power-On Reset Timing.

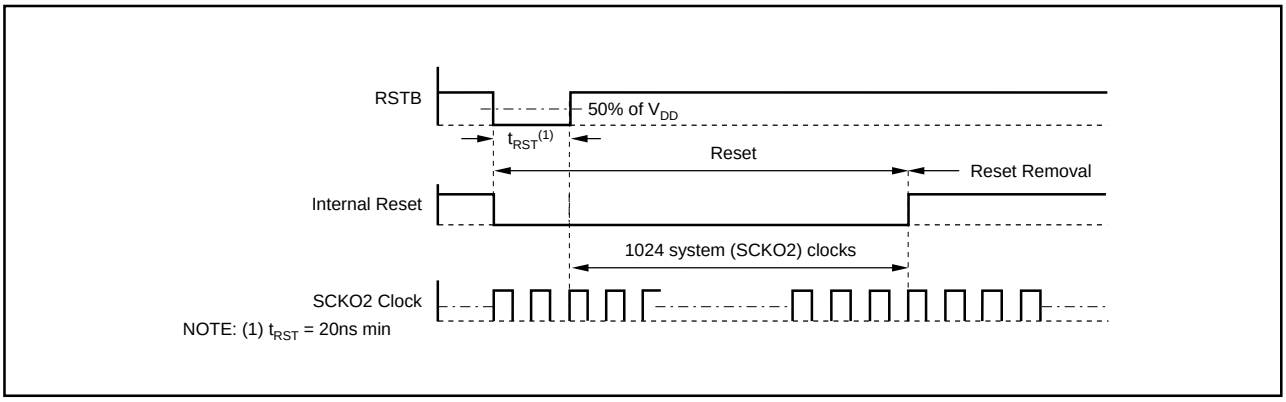


FIGURE 14. RSTB-Pin Reset Timing.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 18 for optimal values of bypass capacitors. Its is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum capacitor.

THEORY OF OPERATION

The delta-sigma section of PCM1727 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 16. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $48f_S$ for a $384f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 17.

Multi Level Delta Sigma

AC-3 APPLICATION CIRCUIT

A typical application for PCM1727 is AC-3 5.1 channel audio decoding and playback. This circuit uses PCM1727 to develop the audio system clock from the 27MHz video clock, with the SCKO2 pin used to drive the AC-3 decoder and two PCM1720 units, the non-PLL version of PCM1723 and PCM1727.

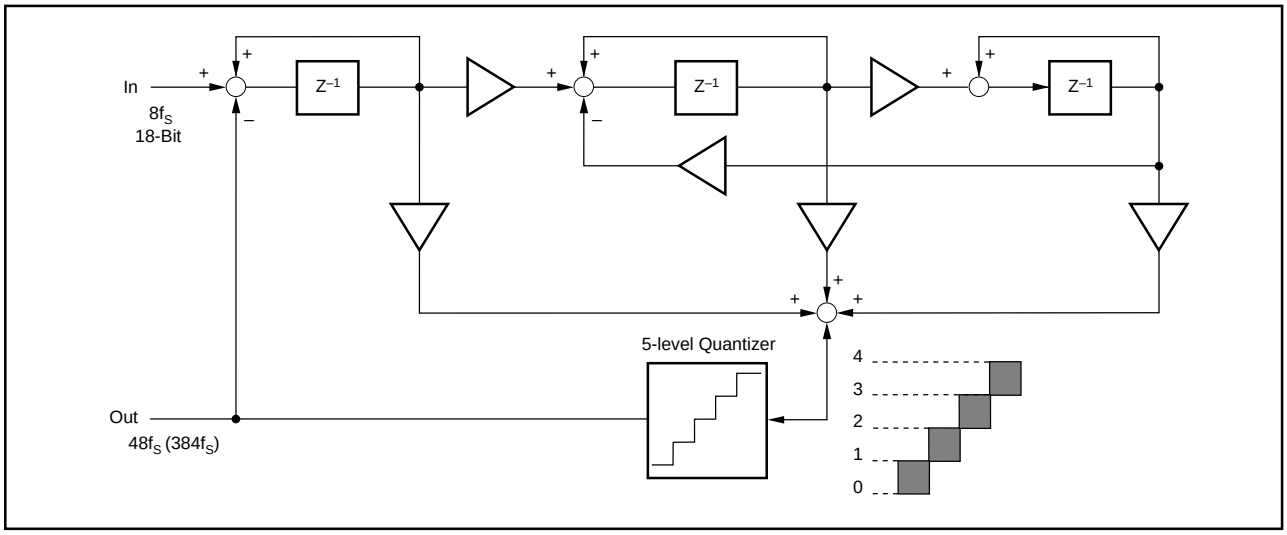


FIGURE 16. 5-Level ΔΣ Modulator Block Diagram.

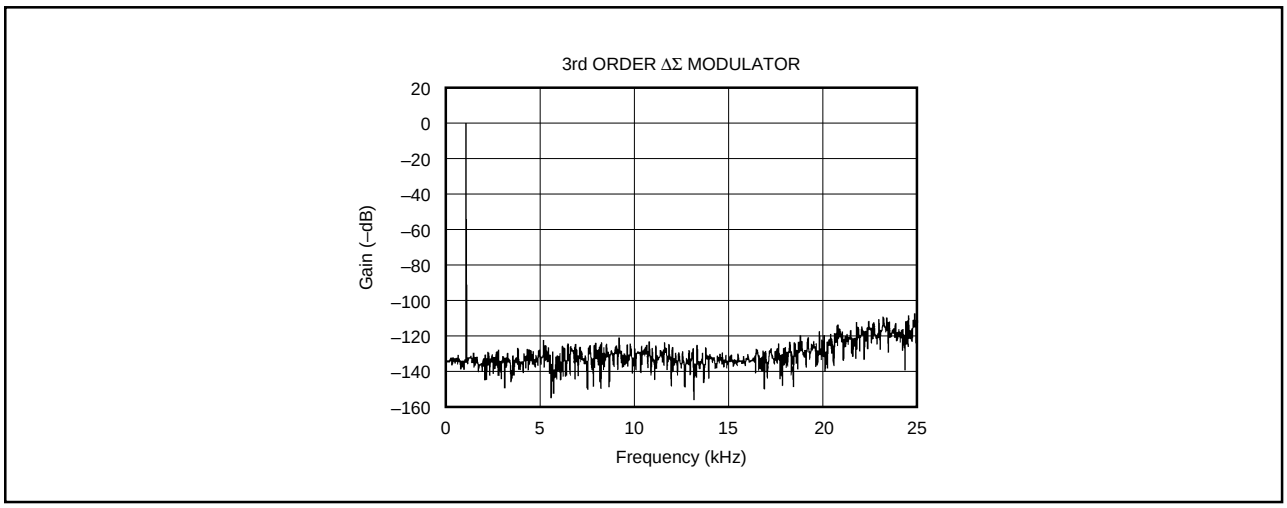


FIGURE 17. Quantization Noise Spectrum.

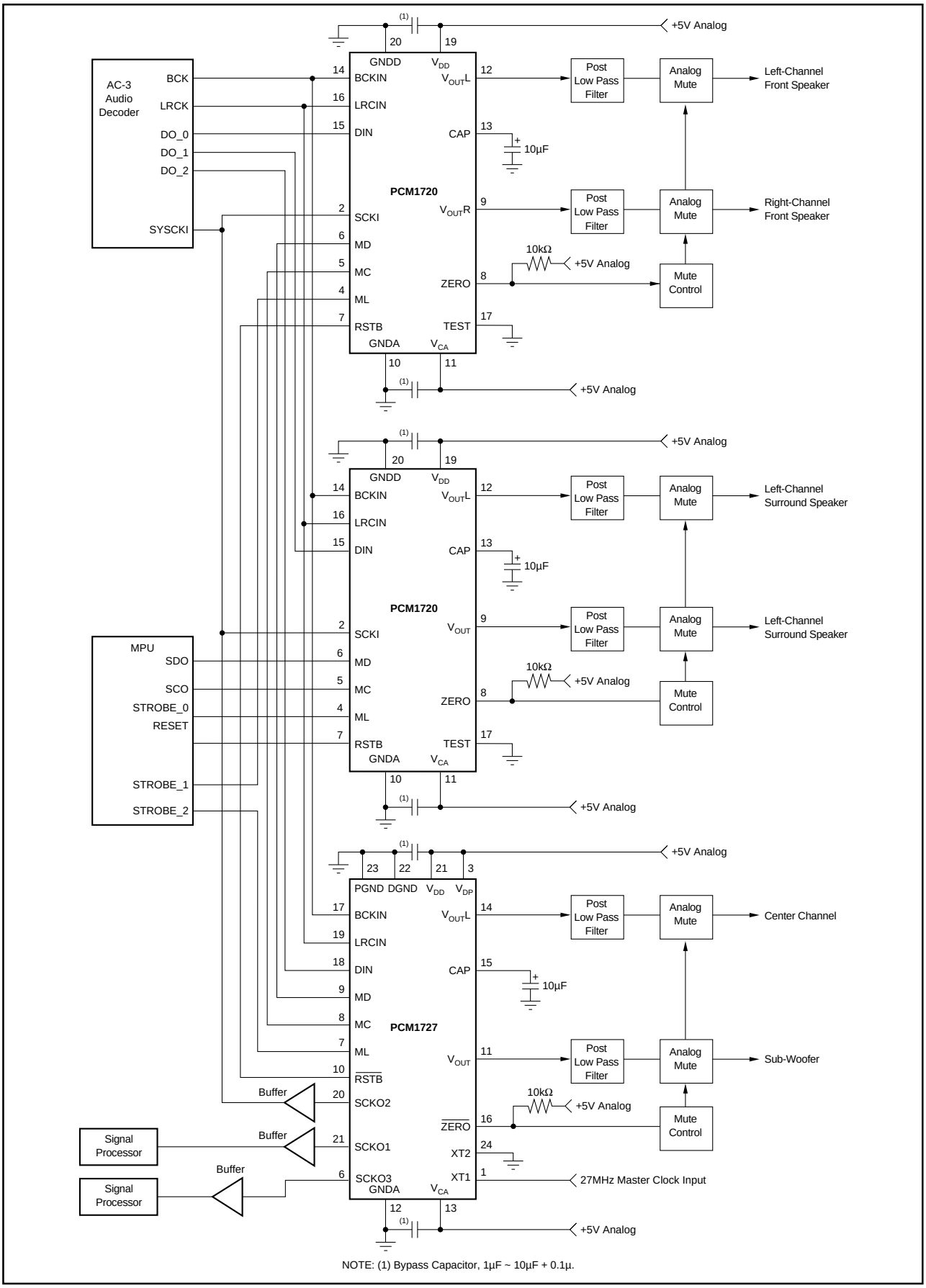


FIGURE 18. Connection Diagram for a 6-Channel AC-3 Application.