FTS64K
Block User Guide
V01.01

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Section 1 Introduction

1.1 Overview

This document describes the FTS64K module which is a 64k byte Flash (Non-Volatile) Memory. The Flash array is organized as 1 block of 64k bytes organized as 1024 rows of 64 bytes. The Flash block's erase sector size is 8 rows (512 bytes).

The Flash memory may be read as either bytes, aligned words or misaligned words. Read access time is one bus cycle for byte and aligned word, and two bus cycles for misaligned words.

Program and erase functions are controlled by a command driven interface. Both sector erase and mass erase of the entire 64k byte Flash block are supported. An erased bit reads '1' and a programmed bit reads '0'. The high voltage required to program and erase is generated internally by on-chip charge pumps.

It is not possible to read from the Flash block while it is being erased or programmed.

The Flash is ideal for program and data storage for single-supply applications allowing for field reprogramming without requiring external programming voltage sources.

WARNING

A word must be erased before being programmed. Cumulative programming of bits within a word is not allowed.

1.1.1 Glossary

Command Sequence

A three-step MCU instruction sequence to program, erase or erase-verify a Flash block.

1.2 Features

- 64k bytes of Flash memory.
- Automated program and erase algorithm.
- Interrupts on Flash command completion and command buffer empty.
- Fast sector erase and word program operation.
- 2-stage command pipeline
- Flexible protection scheme for protection against accidental program or erase.
- Single power supply program and erase.
- Security feature.

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1.3 Modes of Operation

- Program and erase operation (please refer to **4.1** for details)

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1.4 Block Diagram

Figure 1-1 shows a block diagram of the FTS64K module.

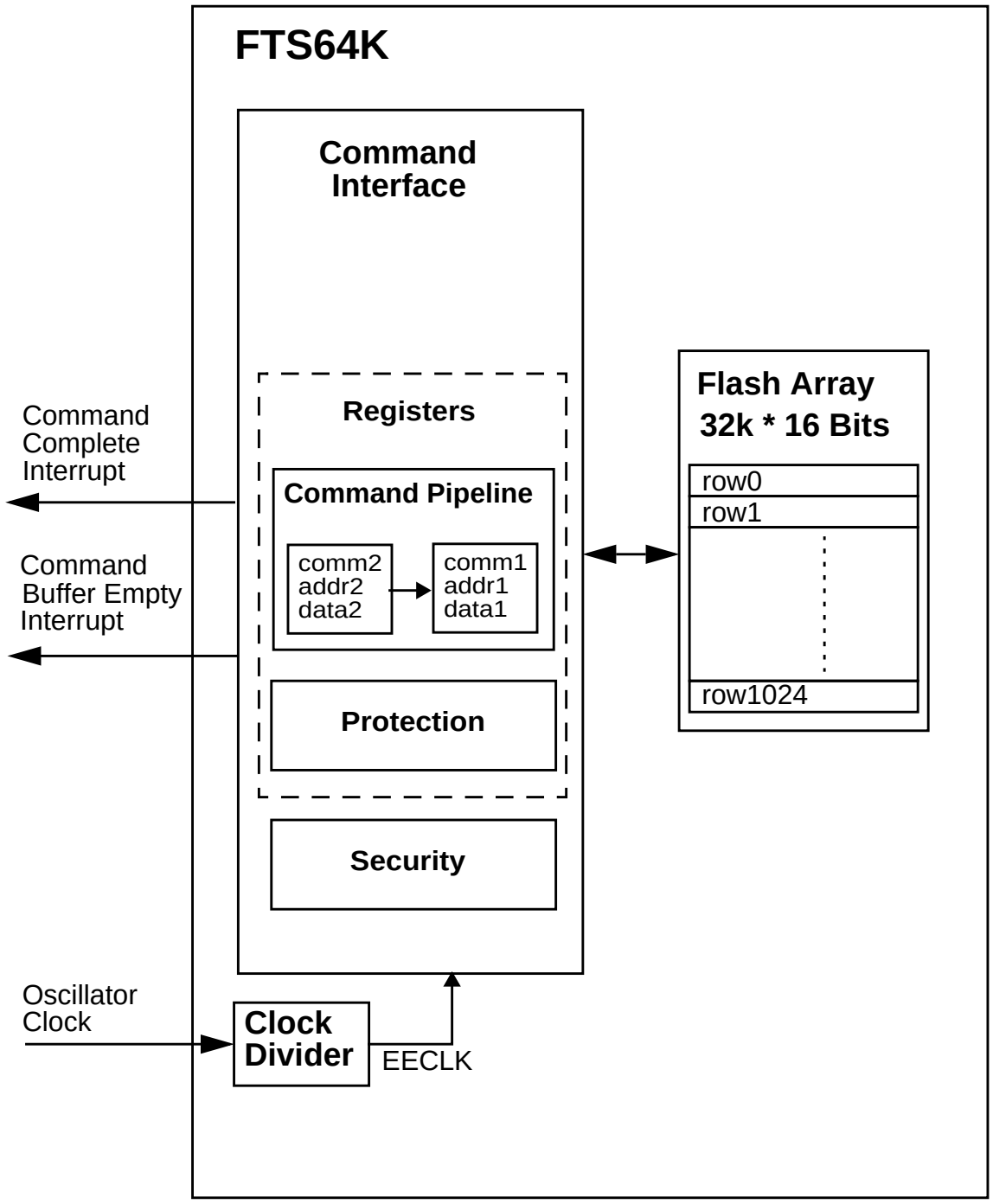


Figure 1-1 FTS64K Module Block Diagram

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Section 2 External Signal Description

2.1 Overview

The FTS64K module contains no signals that connect off-chip.

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Section 3 Memory Map and Registers

3.1 Overview

This section describes the FTS64K memory maps and registers.

3.2 Modules Memory Map

Figure 3-1 shows the FTS64K memory map. The STAR12 architecture places the Flash memory address between $4000 and $FFFF, which corresponds to three 16k byte pages.The content of the PPAGE register is used to map the logical middle page ranging from address $8000 to $BFFF to any physical 16K bytes page in the physical memory[1]. Shown within the blocks are a protection/options field and user defined Flash protected sectors.

The FPOPEN bit in the FPROT register (see **3.3.5**) can globally protect the entirety of the memory block. However, two protected areas, one starting from the Flash page starting address (called lower) towards higher addresses and the other one growing downward from the Flash page end address (called higher) can be activated. The latter is mainly targeted to hold the boot loader code since it covers the vector space. All the other areas may be used to keep critical parameters.

The pagination process using the PPAGE register is handled the Star12 CPU.

The Flash module register space covers the addresses BASE + $100 to BASE + $10F.

NOTES:
1. By placing $3F or $3E in the PPAGE register, the bottom respectively top “fixed” 16Kbytes pages can be seen twice in the MCU memory map.

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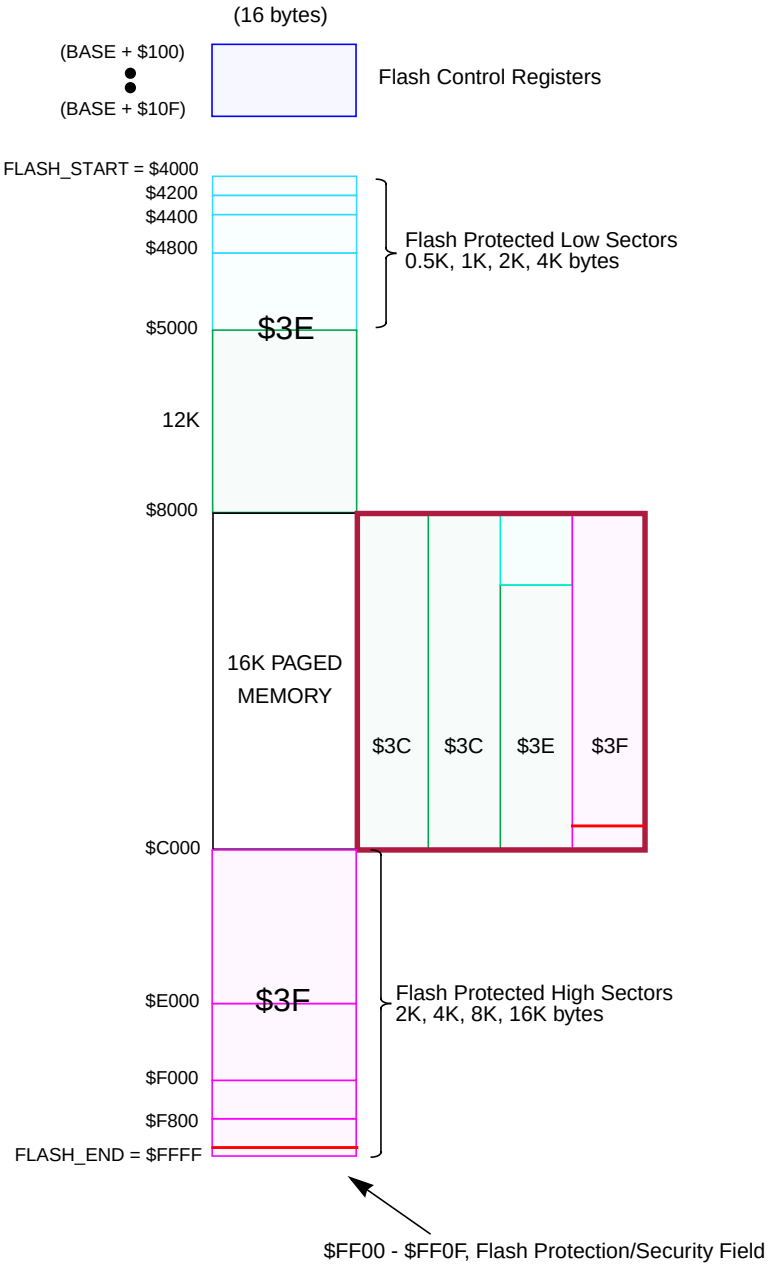
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Security information that allows the MCU to prevent intrusive access to the NVM module is stored in the Flash block's Flash Protection/Options field. A description of the 16 bytes used in this field is given in **Table 3-1**.

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Figure 3-1 FTS64K Flash Memory Map



Note: $3C-$3F correspond to the PPAGE register content

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Table 3-1 Flash Protection/Options Field

Address	Size (bytes)	Description
$FF00 - $FF07	8	Backdoor Comparison Keys
$FF08 - $FF0C	5	Reserved
$FF0D	1	Flash Protection byte Refer to Section **3.3.5**
$FF0E	1	Reserved
$FF0F	1	Flash Options/Security byte Refer to Section **3.3.2**

Table 3-2 Memory Maps Summary

MCU Address Range	PPAGE	Protectable Low Range	Protectable High Range	Block Relative Address[1]
$4000-$7FFF	Unpaged ($3E)	$4000-$41FF $4000-$43FF $4000-$47FF $4000-$4FFF	N.A.	$8000-$BFFF
$8000-$BFFF	$3C	N.A.	N.A.	$0000-$3FFF
	$3D	N.A.	N.A.	$4000-$7FFF
	$3E	$8000-$81FF $8000-$83FF $8000-$87FF $8000-$8FFF	N.A.	$8000-$BFFF
	$3F	N.A.	$B800-$BFFF $B000-$BFFF $A000-$BFFF $8000-$BFFF	$C000-$FFFF
$C000-$FFFF	Unpaged ($3F)	N.A.	$F800-$FFFF $F000-$FFFF $E000-$FFFF $C000-$FFFF	$C000-$FFFF

NOTES:
1. Inside Flash block.

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The Flash module has hardware interlocks which protect data from accidental corruption. One protected sector is located at the higher address end, just below $FFFF. Another protected sector is located at the lower address end, just after the beginning of the Flash code implementation at address $4000. Both the high and low address protected sectors in the Flash can be sized from 512 bytes to 4K bytes. The middle Flash page can also exhibit protectable areas as indicated in the memory map summary **Table 3-2**.

The NVM module also contains a set of 16 control and status registers located in address space BASE + $100 to BASE + $10F. A summary of these registers is given in **Table 3-3**.

Table 3-3 FTS64K Memory Map

Address Offset	Use	Access
$_00	Flash Clock Divider Register (FCLKDIV)	R/W
$_03	Flash Security Register (FSEC)	R
$_02	RESERVED1[1]	R
$_03	Flash Configuration Register (FCNFG)	R/W
$_04	Flash Protection Register (FPROT)	R/W
$_05	Flash Status Register (FSTAT)	R/W
$_06	Flash Command Register (FCMD)	R/W
$_07	RESERVED2[2]	R
$_08	RESERVED3[3]	R
$_09	RESERVED4[4]	R
$_0A	RESERVED5[5]	R
$_0B	RESERVED6[6]	R

NOTES:
1. RESERVED2 intended for factory test purposes only.
2. RESERVED3 intended for factory test purposes only.
3. RESERVED4 intended for factory test purposes only.
4. RESERVED5 intended for factory test purposes only.
5. RESERVED6 intended for factory test purposes only.
6. RESERVED7 intended for factory test purposes only.

NOTE: *Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.*

3.3 Register Descriptions

3.3.1 FCLKDIV — Flash Clock Divider Register

The FCLKDIV register is used to control timed events in program and erase algorithms.

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Register address BASE + $100

	7	6	5	4	3	2	1	0
R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
W								
RESET:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-2 Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6-0 are write once and bit 7 is not writable.

FDIVLD — Clock Divider Loaded.

1 = Register has been written to since the last reset.

0 = Register has not been written.

PRDIV8 — Enable Prescaler by 8.

1 = Enables a prescaler by 8, to divide the Flash module input oscillator clock before feeding into the CLKDIV divider.

0 = The input oscillator clock is directly fed into the FCLKDIV divider.

FDIV[5:0] — Clock Divider Bits.

The combination of PRDIV8 and FDIV[5:0] effectively divides the Flash module input oscillator clock down to a frequency of 150kHz - 200kHz. The maximum divide ratio is 512. Please refer to section **4.1.1** for more information.

3.3.2 FSEC — Flash Security Register

This FSEC register holds all bits associated with the device security.

Register address BASE + $101

	7	6	5	4	3	2	1	0
R	KEYEN	NV6	NV5	NV4	NV3	NV2	SEC1	SEC0
W								
Reset:	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 3-3 Flash Security Register (FSEC)

All bits in the FSEC register are readable but not writable.

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The FSEC register is loaded from the Flash Protection/Options field byte at $FF0F during the reset sequence, indicated by “F” in **Figure 3-3**.

KEYEN — Enable backdoor key to security.
1 = backdoor to Flash is enabled.
0 = backdoor to Flash is disabled.

NV[6:2] — Non Volatile Flag Bits.

These 5 bits are available to the user as non-volatile flags.

SEC[1:0] — Memory Security Bits.

The SEC[1:0] bits define the security state of the device as shown in **Table 3-4**. If the Flash is unsecured using the Backdoor Key Access, the SEC bits are forced to 10.

Table 3-4 Security States

SEC[1:0]	Description
00	secured
01	secured
10	unsecured
11	secured

The security function in the Flash module is described in section **4.5**.

3.3.3 RESERVED1

This register is reserved and is not accessible to the user.

Register address BASE + $102

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-4 RESERVED 1

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3.3.4 FCNFG — Flash Configuration Register

The FCNFG register enables the Flash interrupts and gates the security backdoor writes.

Register address BASE + $103

	7	6	5	4	3	2	1	0
R	CBEIE	CCIE	KEYACC	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5 Flash Configuration Register (FCNFG)

CBEIE, CCIE and KEYACC are readable and writable. Bits 4-0 read zero and are not writable.

CBEIE — Command Buffer Empty Interrupt Enable.

The CBEIE bit enables the interrupts in case of an empty command buffer in the Flash.
1 = An interrupt will be requested whenever the CBEIF flag, **Figure 3-7**, is set.
0 = Command Buffer Empty interrupts disabled.

CCIE — Command Complete Interrupt Enable.

The CCIE bit enables the interrupts in case of all commands being completed in the Flash.
1 = An interrupt will be requested whenever the CCIF, **Figure 3-7**, flag is set.
0 = Command Complete interrupts disabled.

KEYACC — Enable Security Key Writing.
1 = Writes to Flash array are interpreted as keys to open the backdoor. Reads of the Flash array return invalid data.
0 = Flash writes are interpreted as the start of a program or erase sequence.

3.3.5 FPROT — Flash Protection Register

The FPROT register defines which Flash sectors are protected against program or erase.

Register address BASE + $104

	7	6	5	4	3	2	1	0
R	FPOPEN	NV6	FPHDIS	FPHS1	FPHS0	FPLDIS	FPLS1	FPLS0
W								
Reset:	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 3-6 Flash Protection Register (FPROT)

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The FPROT register is readable in user and special modes. Bit NV6 is not writable. FPOPEN, FPHDIS and FPLDIS bits in the FPROT register can only be written to the protected state (i.e. 0). FPLS[1:0] can be written anytime until bit FPLDIS is cleared. FPHS[1:0] bits can be written anytime until bit FPHDIS is cleared. If the FPOPEN bit is cleared, then the state of the FPHDIS, FPHS[1:0], FPLDIS and FPLS[1:0] bits is irrelevant. The FPROT register is loaded from Flash address $FF0D during reset.

To change the Flash protection that will be loaded on reset, the upper sector of Flash must be unprotected, then the Flash Protect/Security byte located as described in **Table 3-1** must be written to.

A protected Flash sector is disabled by the bits FPHDIS and FPLDIS while the size of the protected sector is defined by FPHS[1:0] and FPLS[1:0] in the FPROT register.

Trying to alter any of the protected areas will result in a protect violation error and bit PVIOL will be set in the Flash Status Register FSTAT. A mass erase of the whole Flash block is only possible when protection is fully disabled by setting FPLDIS and FPHDIS bits.

FPOPEN — Opens the Flash for program or erase.

1 = The Flash sectors not protected are enabled for program or erase.

0 = The whole Flash array is protected. In this case the FPHDIS, FPHS[1:0], FPLDIS and FPLS[1:0] bits within the protection register are don't care.

FPHDIS — Flash Protection Higher address range Disable.

The FPHDIS bit determines whether there is a protected area in the higher space of the Flash address map.

1 = Protection disabled.

0 = Protection enabled.

FPHS[1:0] — Flash Protection Higher Address Size.

The FPHS[1:0] bits determine the size of the protected sector. Refer to **Table 3-5**.

Table 3-5 Flash Higher Address Range Protection

FPHS	Protected Address Range	Protected Size
00	see **Table 3-2**	2K bytes
01		4K
10		8K
11		16K

FPLDIS — Flash Protection Lower address range Disable.

The FPLDIS bit determines whether there is a protected sector in the lower space of the Flash address map.

1 = Protection disabled.

0 = Protection enabled.

FPLS[1:0] — Flash Protection Lower Address Size.

The FPLS[1:0] bits determine the size of the protected sector. Refer to **Table 3-6**.

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Table 3-6 Flash Lower Address Range Protection

FPLS	Protected Address Range	Protected Size
00	see **Table 3-2**	512 Bytes
01		1K
10		2K
11		4K

NV6 — Non Volatile Flag Bit.

This bit is available as non-volatile flag.

3.3.6 FSTAT — Flash Status Register

The FSTAT register defines the Flash state machine command status and Flash array access, protection and blank verify status.

Register address BASE + $105

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
W								
Reset:	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7 Flash Status Register (FSTAT)

Register bits CBEIF, PVIOL and ACCERR are readable and writable, bits CCIF and BLANK are readable and not writable, bits 3, 1 and 0 read zero and are not writable.

CBEIF — Command Buffer Empty Interrupt Flag.

The CBEIF flag indicates that the address, data and command buffers are empty so that a new command sequence can be started. The CBEIF flag is cleared by writing a “1” to CBEIF. Writing a “0” to the CBEIF flag has no effect on CBEIF but sets ACCERR, which can be used to abort a command sequence. This bit, CBEIF, is used together with the enable bit CBEIE, to generate the interrupt request (see also **Figure 6-1**).

1 = Buffers are ready to accept a new command.
0 = Buffers are full.

CCIF — Command Complete Interrupt Flag.

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The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is clear and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect. This bit, CCIF, is used together with the enable bit CCIE, to generate the interrupt request (see also **Figure 6-1**).

1 = All commands are completed.
0 = Command in progress.

PVIOL — Protection Violation.

The PVIOL flag indicates an attempt was made to program or erase an address in a protected Flash memory area. The PVIOL flag is cleared by writing a “1” to PVIOL. Writing a “0” to the PVIOL flag has no effect on PVIOL. While PVIOL is set it is not possible to launch another command.

1 = A protection violation has occurred.
0 = No failure.

ACCERR — Flash Access Error.

The ACCERR flag indicates an illegal access to the selected Flash array. This can be either a violation of the command sequence, issuing an illegal command (illegal combination of the CMDBx bits in the FCMD register) or the execution of a CPU STOP instruction while a command is executing (CCIF=0). The ACCERR flag is cleared by writing a “1” to ACCERR. Writing a “0” to the ACCERR flag has no effect on ACCERR. While ACCERR is set it is not possible to launch another command.

1 = Access error has occurred.
0 = No failure.

BLANK — Array has been verified as erased.

The BLANK flag indicates that an Erase Verify command has checked the Flash block and found it to be blank. The BLANK flag is cleared by hardware when CBEIF is cleared as part of a new valid command sequence. Writing to the BLANK flag has no effect on BLANK.

1 = Flash block verifies as erased.
0 = If an Erase Verify command has been requested, and the CCIF flag is set, then a zero in BLANK indicates the Flash is not erased.

3.3.7 FCMD — Flash Command Register

The FCMD register defines the Flash commands.

Register address BASE + $106

	7	6	5	4	3	2	1	0
R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-8 Flash Command Buffer and Register (FCMD)

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Bits 7, 4, 3 and 1 read zero and are not writable. Bits CMDB6, CMDB5, CMDB2 and CMDB0 are readable and writable during a command sequence.

CMDB — Valid NVM User mode commands are shown in **Table 3-7**. Any commands other than those mentioned in **Table 3-7** sets the ACCERR bit in the FSTAT register (**3.3.6**).

Table 3-7 FCMD NVM User Mode Commands

Command	Meaning
$05	Erase Verify
$20	Byte Program
$40	Sector Erase
$41	Mass Erase

3.3.8 RESERVED2

This register is reserved for factory testing and is not accessible to the user.

Register address BASE + $107

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-9 RESERVED2

All bits read zero and are not writable.

3.3.9 RESERVED3

This register is reserved for factory testing and is not accessible to the user.

Register address BASE + $108

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-10 RESERVED3

All bits read zero and are not writable.

3.3.10 RESERVED4

This register is reserved for factory testing and is not accessible to the user.

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Register address BASE + $109

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-11 RESERVED4

All bits read zero and are not writable.

3.3.11 RESERVED5

This register is reserved for factory testing and is not accessible to the user.

Register address BASE + $11A

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-12 RESERVED5

All bits read zero and are not writable.

3.3.12 RESERVED6

This register is reserved for factory testing and is not accessible to the user.

Register address BASE + $11B

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

Figure 3-13 RESERVED6

All bits read zero and are not writable.

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Section 4 Functional Description

4.1 Program and Erase Operation

Write and read operations are both used for the program and erase algorithms described in this section. These algorithms are controlled by a state machine whose timebase FCLK is derived from the oscillator clock via a programmable divider. The command register as well as the associated address and data registers operate as a buffer and a register (2-stage FIFO), so that a new command along with the necessary data and address can be stored to the buffer while the previous command is still in progress. This pipelined operation allows a time optimization when programming more than one word on a specific row, as the high voltage generation can be kept ON in between two programming commands. The pipelined operation also allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the Flash status register. Interrupts for the Flash will be generated if enabled.

The next four subsections describe:

- How to write the FCLKDIV register.
- The write sequences used to program, erase and erase-verify the Flash.
- Valid Flash commands.
- Errors resulting from illegal Flash operations.

4.1.1 Writing the FCLKDIV Register

Prior to issuing any program or erase command, it is first necessary to write the FCLKDIV register to divide the oscillator down to within the 150kHz to 200kHz range. The program and erase timings are also a function of the bus clock, such that the FCLKDIV determination must take this information into account. If we define:

- FCLK as the clock of the Flash timing control block
- Tbus as the period of the bus clock
- INT(x) as taking the integer part of x (e.g. INT(4.323)=4),

then FCLKDIV register bits PRDIV8 and FDIV[5:0] are to be set as described in **Figure 4-1**.

For example, if the oscillator clock frequency is 950kHz and the bus clock is 10MHz, FCLKDIV bits FDIV[5:0] should be set to 4 (000100) and bit PRDIV8 set to 0. The resulting FCLK is then 190kHz. As a result, the Flash algorithm timings are increased over optimum target by:

$$(200 - 190)/200 \times 100 = 5\%$$

NOTE

Command execution time will increase proportionally with the period of FCLK.

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WARNING

Because of the impact of clock synchronization on the accuracy of the functional timings, programming or erasing the Flash cannot be performed if the bus clock runs at less than 1 MHz. Programming or erasing the Flash with an input clock < 150kHz should be avoided. Setting FCLKDIV to a value such that FCLK < 150kHz can destroy the Flash due to overstress. Setting FCLKDIV to a value such that (1/FCLK+Tbus) < 5μs can result in incomplete programming or erasure of the memory array cells.

If the FCLKDIV register is written, the bit FDIVLD is set automatically. If this bit is zero, the register has not been written since the last reset. Program and erase commands will not be executed if this register has not been written to.

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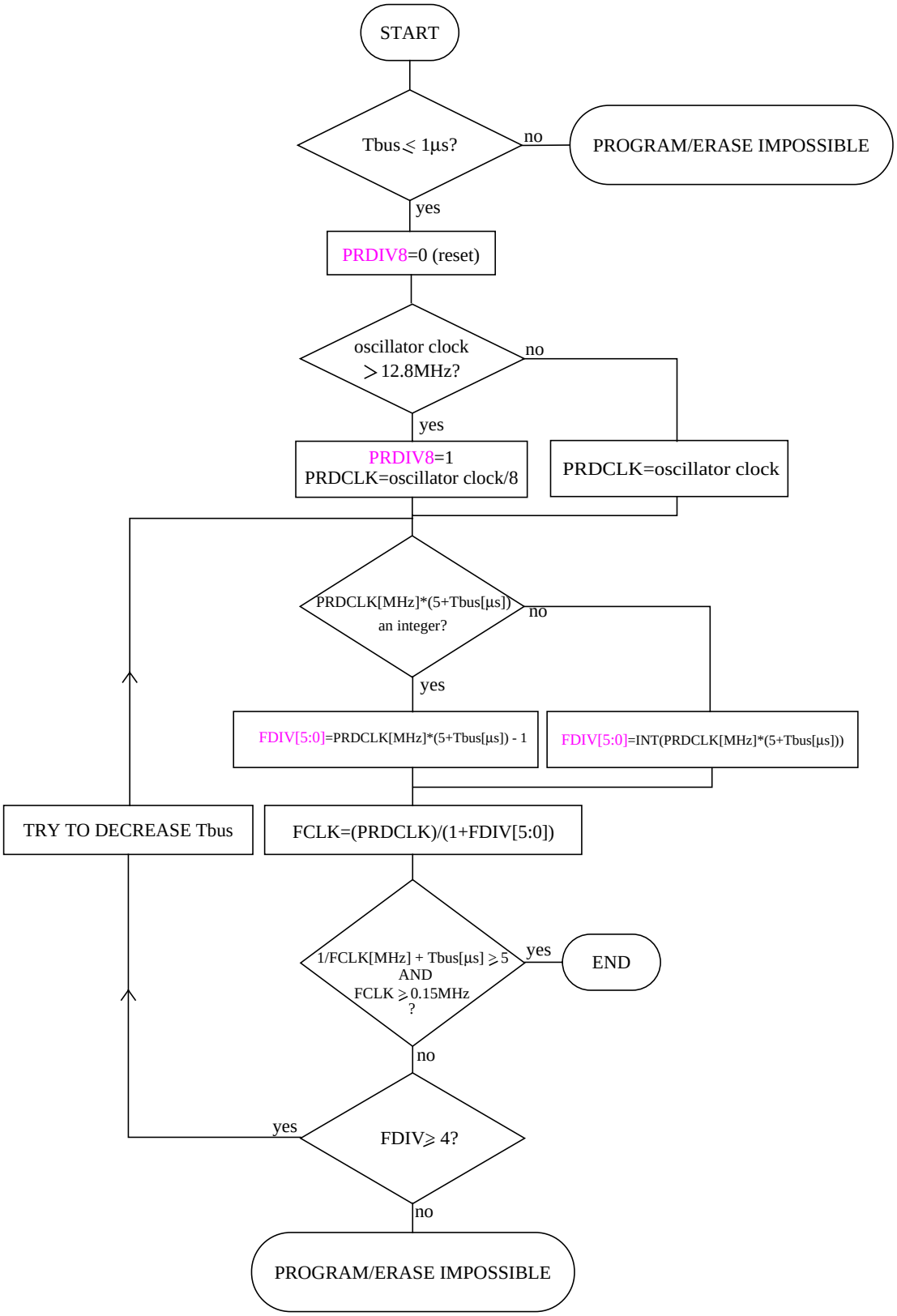


Figure 4-1 PRDIV8 and FDIV bits Determination Procedure

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4.1.2 Program and Erase Sequences in User Mode

A Command State Machine is used to supervise the write sequencing for program and erase. The erase-verify command follows the same flow. Before starting a command sequence, it is necessary to verify that there is no pending access error or protection violation (the ACCERR and PVIOL flags should be cleared in the FSTAT register) It is then required to set the PPAGE register. The procedure is as follows:

1. Verify that all ACCERR and PVIOL flags in the FSTAT register are cleared.
2. Write to the core PPAGE register ($x030) to select one of the pages to be programmed if programming in the $8000-$BFFF address range. There is no need to set PPAGE when programming in the $4000-$7FFF or $C000-$FFFF address ranges.

After this possible initialization step the CBEIF flag should be tested to ensure that the address, data and command buffers are empty. If so, the program/erase command write sequence can be started. The following 3-step command write sequence must be strictly adhered to and no intermediate writes to the Flash module are permitted between the 3 steps. It is possible to read any Flash register during a command sequence. The command sequence is as follows:

1. Write the aligned data word to be programmed to the valid Flash address space. The address and data will be stored in internal buffers. For program, all address bits are valid. For erase, the value of the data bytes is don't care. For mass erase, the address can be anywhere in the available address space of the block to be erased. For sector erase the address bits[8:0] are ignored.
2. Write the program or erase command to the command buffer. These commands are listed in **Table 4-1**.
3. Clear the CBEIF flag by writing a "1" to it to launch the command. When the CBEIF flag is cleared, the CCIF flag is cleared by hardware indicating that the command was successfully launched. The CBEIF flag will be set again indicating the address, data and command buffers are ready for a new command sequence to begin.

The completion of the command is indicated by the CCIF flag setting. The CCIF flag only sets when all active and pending commands have been completed.

NOTE

The Command State Machine will flag errors in program or erase write sequences by means of the ACCERR (access error) and PVIOL (protection violation) flags in the FSTAT register. An erroneous command write sequence will abort and set the appropriate flag. If set, the user must clear the ACCERR or PVIOL flags before commencing another command write sequence. By writing a 0 to the CBEIF flag the command sequence can be aborted after the word write to the Flash address space or after writing a command to the FCMD register and before the command is launched. Writing a "0" to the CBEIF flag in this way will set the ACCERR flag.

A summary of the program algorithm is shown in **Figure 4-2**. For the erase algorithm, the user writes either a mass or sector erase command to the FCMD register.

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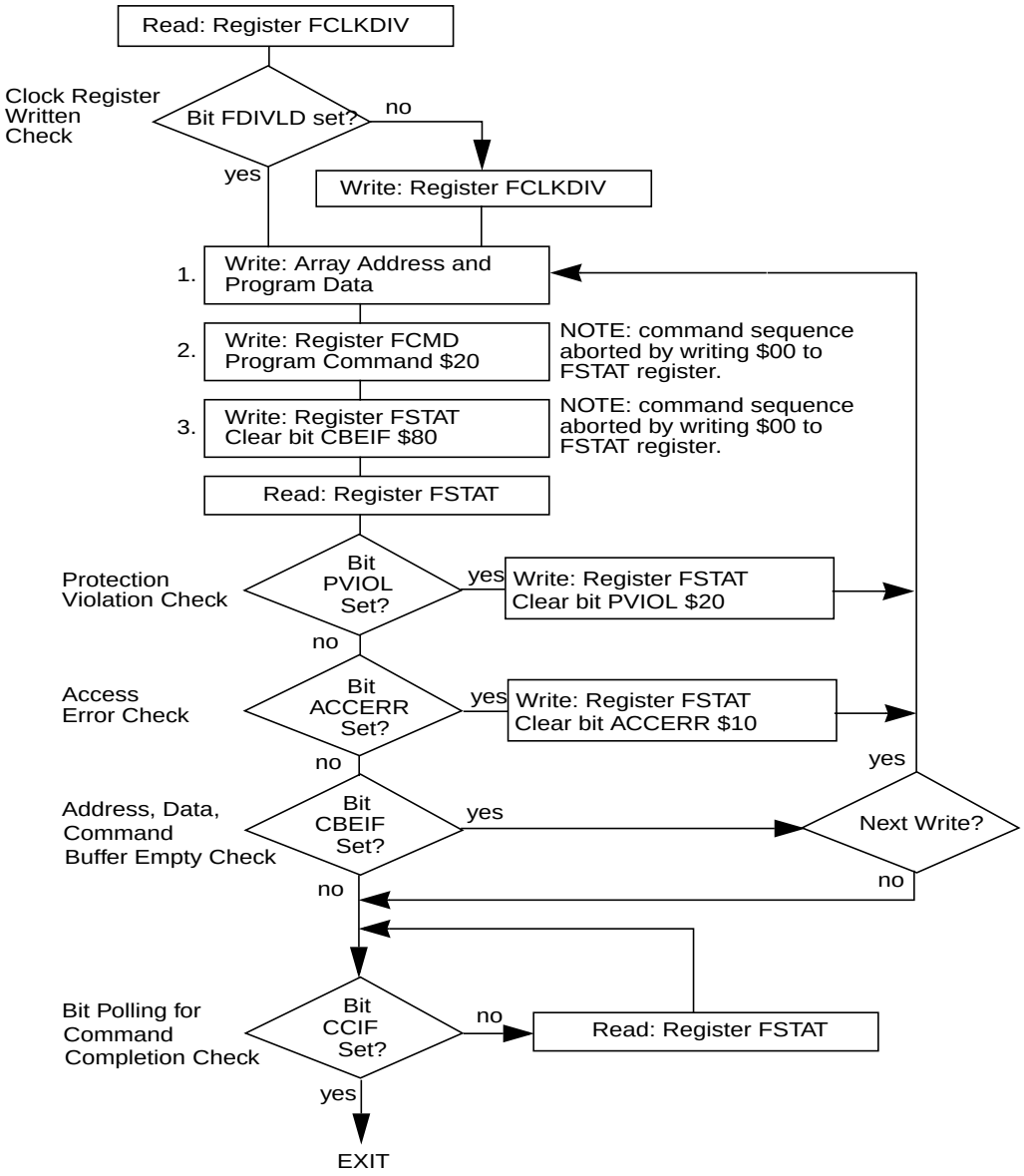


Figure 4-2 Example Program Algorithm

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4.1.3 Valid Flash Commands

Table 4-1 summarizes the valid Flash User commands. Also shown are the effects of the commands on the Flash

Table 4-1 Valid Flash Commands

FCMD	Meaning	Flash
$05	Erase Verify	Verify all memory bytes of the Flash block are erased. If the array is erased the BLANK bit will set in the FSTAT register, upon command completion.
$20	Program	Program a word (two bytes).
$40	Sector Erase	Erase 256 words of Flash.
$41	Mass Erase	Erase all the Flash array. A mass erase of the full block is only possible when FPLDIS, FPHDIS and FPOPEN are set.

WARNING

It is not permitted to program a Flash word without first erasing the sector in which that word resides.

4.1.4 Illegal Flash Operations

The ACCERR flag will be set during the command write sequence if any of the following illegal operations are performed causing the command write sequence to immediately abort:

1. Writing to the Flash address space before initializing FCLKDIV.
2. Writing to the Flash address space in the range $8000-$BFFF when PPAGE register does not select a 16K bytes page in the Flash block.
3. Writing a misaligned word or a byte to the valid Flash address space.
4. Writing to the Flash address space while CBEIF is not set.
5. Writing a second word to the Flash address space before executing a program or erase command on the previously written word.
6. Writing to any Flash register other than FCMD after writing a word to the Flash address space.
7. Writing a second command to the FCMD register before executing the previously written command.

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8. Writing an invalid user command to the FCMD register in user mode.
9. Writing to any Flash register other than FSTAT (to clear CBEIF) after writing to the command register, FCMD.
10. The part enters STOP mode and a program or erase command is in progress. The command is aborted and any pending command is killed.
11. When security is enabled, a command other than Mass-Erase originating from a non-secure memory or from the Background Debug Mode is written to FCMD.
12. A “0” is written to the CBEIF bit in the FSTAT register.

The ACCERR flag will not be set if any Flash register is read during the command sequence.

If the Flash array is read during execution of an algorithm (i.e. CCIF bit in the FSTAT register is low) the read will return non valid data and the ACCERR flag will not be set

If an ACCERR flag is set in the FSTAT register the Command State Machine is locked. It is not possible to launch another command until the ACCERR flag is cleared.

The PVIOL flag will be set during the command write sequence after the word write to the Flash address space if any of the following illegal operations are performed, causing the command sequence to immediately abort:

1. Writing a Flash address to program in a protected area of the Flash.
2. Writing a Flash address to erase in a protected area of the Flash.
3. Writing the mass erase command to FCMD while any protection is enabled. See Protection register description in **3.3.5**.

If a PVIOL flag is set in the FSTAT register the Command State Machine is locked. It is not possible to launch another command until the PVIOL flag is cleared.

4.2 Wait Mode

When the MCU enters WAIT mode and if any command is active (CCIF=0), that command and any pending command will be completed.

The FTS64K module can recover the part from WAIT if the interrupts are enabled (see **Section 6**).

4.3 Stop Mode

If a command is active (CCIF = 0) when the MCU enters the STOP mode, the command will be aborted, and the data being programmed or erased is lost. The high voltage circuitry to the flash will be switched off when entering STOP mode. CCIF and ACCERR flags will be set. Upon exit from STOP the CBEIF flag is set and any pending command will not be executed. The ACCERR flag must be cleared before returning to normal operation.

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WARNING

As active commands are immediately aborted when the MCU enters STOP mode, it is strongly recommended that the user does not use the STOP command during program and erase execution.

4.4 Background Debug Mode

In Background Debug Mode (BDM), the FPROT registers are writable. If the chip is unsecured then all Flash commands listed in **Table 4-1** can be executed. In special single chip mode if the chip is secured then the only possible command to execute is Mass Erase.

4.5 Flash Security

The Flash module provides the necessary security information to the rest of the chip. After each reset, the Flash module determines the security state of the microcontroller as defined in section **3.3.2**.

The contents of the Flash Protection/Options byte at $FF0F in the Flash Protection/Options Field must be changed directly by programming $FF0F when the device is unsecured and the higher address sector is unprotected. If the Flash Protection/Options byte is left in the secure state, any reset will cause the microcontroller to return to the secure operating mode

4.5.1 Unsecuring the Flash via the Backdoor Key Access

The microcontroller may only be unsecured by using the Backdoor Key Access feature. This requires knowledge of the contents of the backdoor keys, four 16-bit words programmed in the Flash at addresses $FF00 - $FF07. With the KEYEN and KEYACC bits set, a write to a backdoor key address triggers a comparison between the written data and the backdoor key data stored in the Flash. If all four words of data are written to the correct addresses in the correct order and the data matches the backdoor keys stored in the Flash the microcontroller will be unsecured. The data must be written to the backdoor keys sequentially staring with $FF00-1 and ending with $FF06-7.When the KEYACC bit is set reads of the Flash array will return invalid data.

The user code stored in the Flash must have a method of receiving the backdoor key from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN bit is set in the FCNFG register, the flash can be unsecured by the following Back Door Access Sequence:

1. Set the KEYACC bit in the Flash Configuration Register FCNFG.
2. Write the correct four 16-bit words backdoor keys to Flash addresses $FF00 - $FF07 sequentially starting with $FF00.
3. Clear the KEYACC bit.
4. If all four 16-bit words match the Flash content, the MCU is unsecured and bits SEC[1:0] in the FSEC register are forced to the unsecure state, ‘10’.

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5. If any of the four 16-bit words does not match the Flash content the MCU remains secured.

After the Backdoor Access Sequence has been correctly matched, the microcontroller will be unsecured. The Flash security byte can be programmed to the unsecure state, if desired.

In the unsecured state the user has full control of the contents of the four word Backdoor Key by programming it in bytes $FF00 - $FF07 of the Flash Protection/Options Field.

The security of the Flash module as defined in the Flash Security/Options byte ($FF0F) is not changed by unsecuring the flash module using the back door access scheme. The Back Door Comparison Key stored in words $FF00 - $FF07 is unaffected by the Back Door Access sequence. After the next reset sequence, the security state of the Flash module is determined by the Flash Security/Options byte ($FF0F)}. The back door access method of unsecuring the microcontroller has no effect on the program and erase protections defined in the Flash Protection Register FPROT.

It is not possible to unsecure the microcontroller in Special Single Chip mode by the Backdoor Access Key sequence via the Background Debug Mode.

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Section 5 Resets

5.1 General

If a reset occurs while any command is in progress that command will be immediately aborted. The state of the word being programmed or the sector / block being erased is not guaranteed.

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Section 6 Interrupts

6.1 General

The FTS64K module can generate an interrupt when all Flash commands are completed or the address, data and command buffers are empty.

Table 6-1 Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash Address, Data and Command Buffers empty	CBEIF (FSTAT from any Flash block)	CBEIE	I Bit
All Commands are completed on Flash	CCIF (FSTAT from any Flash block)	CCIE	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level

6.2 Description of Interrupt Operation

Figure 6-1 shows the logic used for generating interrupts.

This system uses the CBEIF and CCIF flags in combination with the enable bits CBIE and CCIE to discriminate for the interrupt generation.

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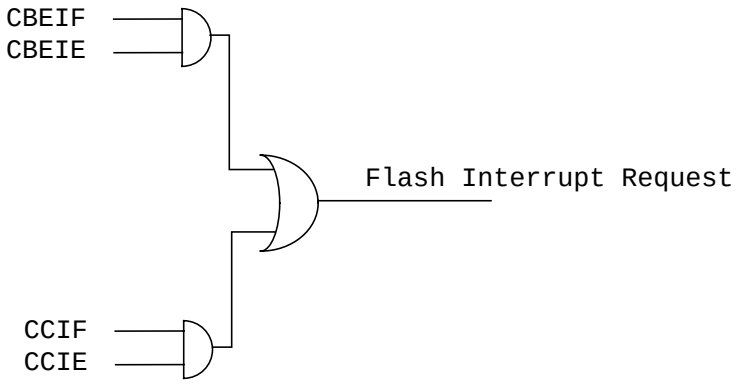


Figure 6-1 FTS64K Flash Interrupt Implementation

For a detailed description of the register bits refer to the Flash Configuration register and Flash Status register sections (respectively **3.3.4** and **3.3.6**).

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