ML9298

12-Hour System Clock IC for 1/2 Duty Fluorescent Display Tubes

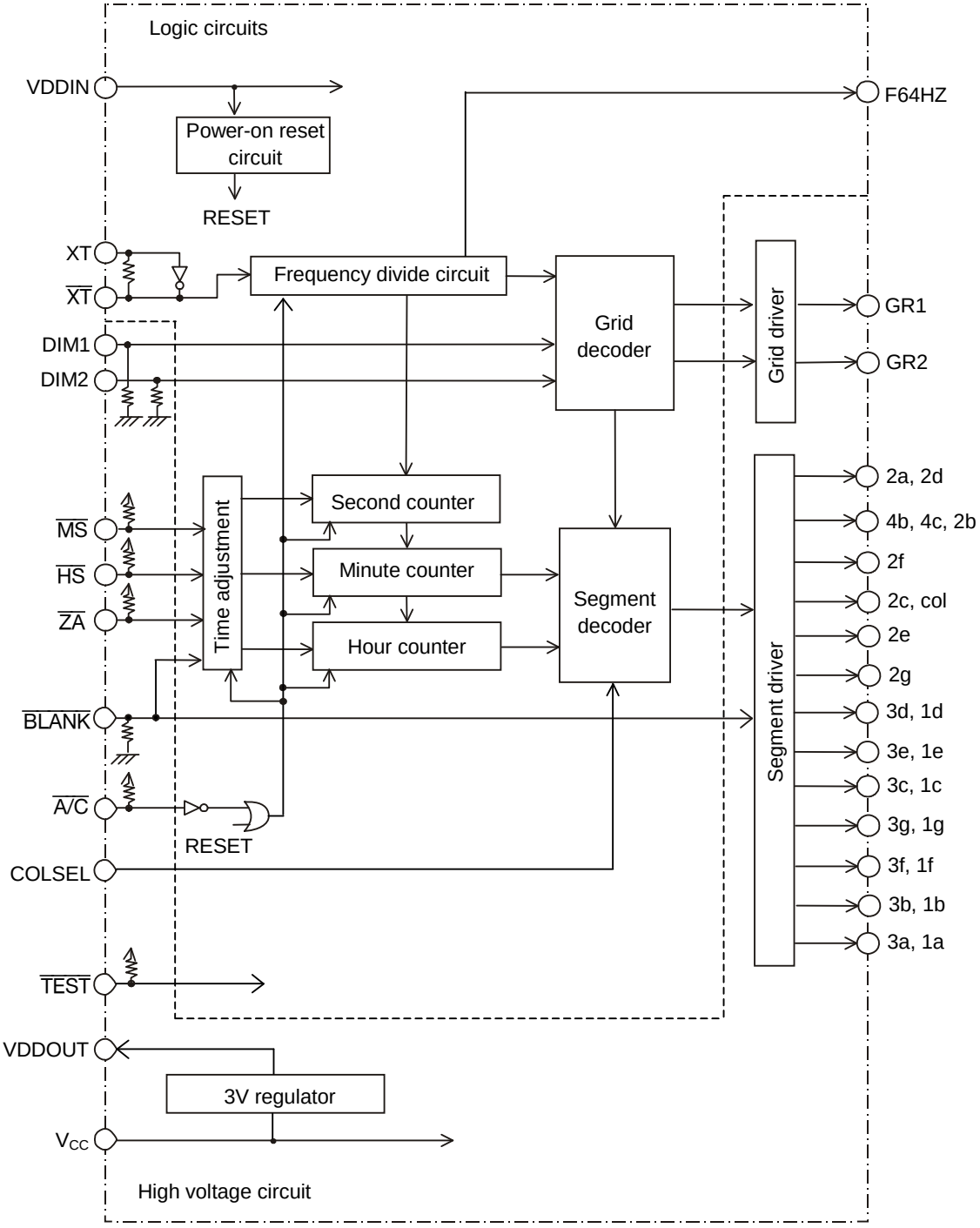
GENERAL DESCRIPTION

The ML9298 is a 12-hour system clock IC that drives 1/2 duty fluorescent display tubes. It has a wide range of power supply using an oscillation source of 4.194304 MHz. The ML9298 has a time adjustment function in hour, minute and 30-minute units, and the function has two adjustment modes, 1 Push 1 ADJ and 2Hz fast forward. Additionally, it has a brightness adjustment function for the fluorescent display tube, providing four levels of brightness settings.

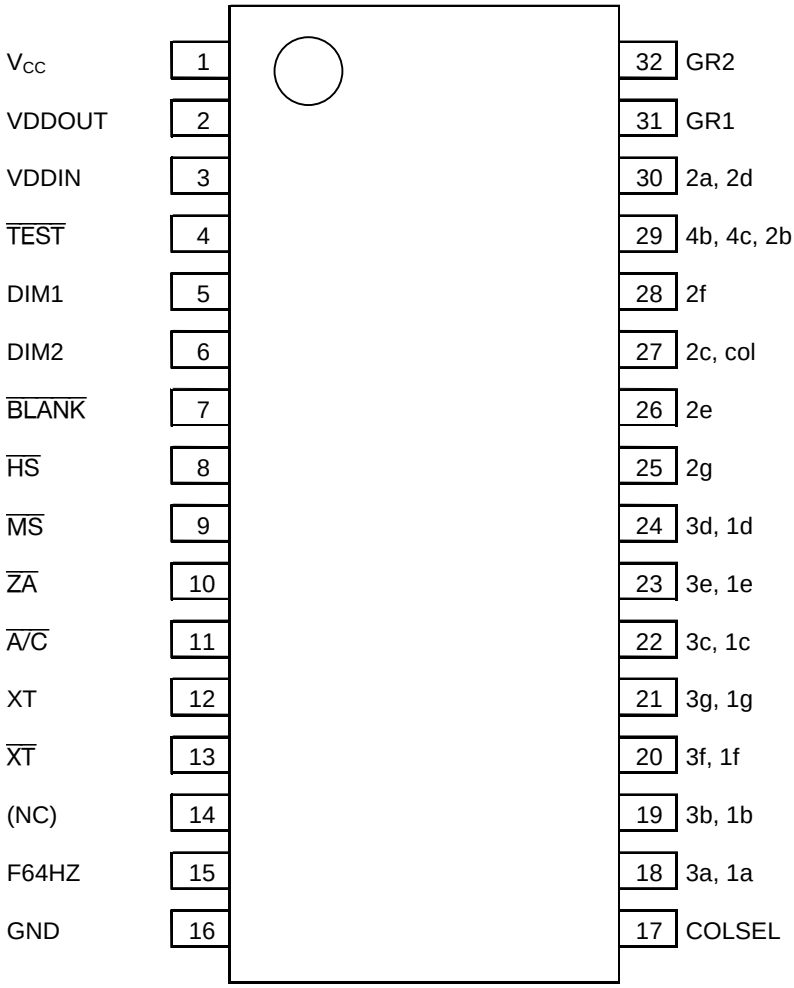
FEATURES

- 12-hour system
- Wide power supply range from 4 to 18V (built-in voltage regulator circuit)
- Designed for 1/2 duty fluorescent display tubes
- 4.194304MHz (crystal oscillation)
- Four levels of brightness settings
- Package: 32-pin plastic SSOP (SSOP32-P-430-1.00-K) (ML9298MB)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTION

Pin	I/O	Pull-up/ Pull-down	Description
DIM1	I	Pull-down	Brightness switching pin.
DIM2	I	Pull-down	
$\overline{A/C}$	I	Pull-up	Input pin with a pull-up resistor to reset the circuits inside this LSI at a “L” level. Set the reset pulse width to 2 ms or more.
$\overline{ZA}$	I	Pull-up	Zero adjust pin.
$\overline{HS}$	I	Pull-up	Hour digit adjustment pin.
$\overline{MS}$	I	Pull-up	Minute digit adjustment pin.
$\overline{BLANK}$	I	Pull-down	Blank input pin. Display disappears at a “L” level.
COLSEL	I	—	This is the input pin for selecting flashing or lighting of the colon output. "L" level : Flashing, "H" level : Lighting
XT	I	—	Crystal oscillation pin to connect a crystal and capacitors Cx and Cy externally.
$\overline{XT}$	O		
$\overline{TEST}$	I	Pull-up	IC testing pin. Leave this pin open or fix it to a “H” level.
F64Hz	O	—	64Hz signal output pin for oscillation frequency adjustment.
GR1	O	—	Output pins for the 1/2 duty fluorescent display tube grids.
GR2			
1a, 3a to 2b, 4b, 4c	O	—	Output pins for the 1/2 duty fluorescent display tube anodes.
V_{CC}	—	—	Power supply pin for high voltage.
GND	—	—	Ground pin.
VDDOUT	O	—	built-in regulator output pin for logic circuits. Connect the pin to the VDDIN pin.
VDDIN	I	—	Power supply pin for logic circuits. Connect the pin to the VDDOUT pin.
NC	—	—	NC pin. Leave the pin open.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage (High voltage)	V_{CC}	Ta = 25°C	–0.3 to 20	V
Power supply voltage (Logic)	VDDIN	Ta = 25°C	–0.3 to 6.5	V
Input voltage (High voltage)	V_{HI}	Ta = 25°C	–0.3 to V_{CC} +0.3	V
Input voltage (Logic)	V_{LI}	Ta = 25°C	–0.3 to VDDIN+0.3	V
Output voltage (High voltage)	V_{HO}	Ta = 25°C	–0.3 to V_{CC} +0.3	V
Output voltage (Logic)	V_{LO}	Ta = 25°C	–0.3 to VDDIN+0.3	V
Output current (High voltage)	I_{HO}	Ta = 25°C	–30 to 3	mA
Output current (Logic)	I_{LO}	Ta = 25°C	–5 to 5	mA
Power dissipation	P_D	Ta ≤ 85°C	350	mW
Storage temperature	T_{STG}	—	–55 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage (High voltage)	V_{CC}	—	4.0	12.0	18.0	V
Power supply voltage (Logic)	VDDIN	—	2.8	3.2	3.6	V
Operating temperature	Ta	—	–40	25	85	°C
Crystal frequency	f(X'tal)	—		4.194304		MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Vcc = 4.0 to 18.0 V, VDDIN = 2.8 to 3.6 V, Ta = –40 to 85°C)

Parameter	Applicable pin	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" input voltage	*1)	V_{IH}	V_{CC} = 4 to 18 V	V_{CC}×0.8	—	—	V
"L" input voltage	*1)	V_{IL}	V_{CC} = 4 to 18 V	—	—	V_{CC}×0.2	V
Input current	DIM1, DIM2, $\overline{BLANK}$, COLSEL	I_{IH1}	V_{CC} = 12 V VIN = V_{CC}	20	65	200	μA
		I_{IL1}	V_{CC} = 12 V VIN = 0 V	–2	—	2	μA
	$\overline{ZA}$, $\overline{HS}$, $\overline{MS}$, $\overline{A/C}$, $\overline{TEST}$	I_{IH2}	V_{CC} = 12 V VIN = V_{CC}	–2	—	2	μA
		I_{IL2}	V_{CC} = 12 V VIN = 0 V	–200	–65	–20	μA
	COLSEL	I_{IH3}	V_{CC} = 12 V VIN = V_{CC}	–2	—	2	μA
		I_{IL3}	V_{CC} = 12 V VIN = 0 V	–2	—	2	μA
Output voltage	*2)	V_{OH1}	V_{CC} = 12 V IOH1 = –1 mA	V_{CC}–2.0	—	—	V
		V_{OL1}	V_{CC} = 12 V IOL1 = 0.55 mA	—	—	2	V
	*3)	V_{OH2}	V_{CC} = 12 V IOH2 = –2 mA	V_{CC}–2.0	—	—	V
		V_{OL2}	V_{CC} = 12 V IOL2= 0.55 mA	—	—	2	V
	GRID1, GRID2	V_{OH3}	V_{CC} = 12 V IOH3 = –15 mA	V_{CC}–2.0	—	—	V
		V_{OL3}	V_{CC} = 12 V IOL3 = 0.55 mA	—	—	2	V
	F64HZ	V_{OH4}	VDDIN = 3.0V IOH4 = –0.1mA	VDDIN–0.5	—	—	V
		V_{OL4}	VDDIN = 3.0V IOL4 = 0.1mA	—	—	0.5	V
Dynamic supply current	V_{CC}	I_{CC}	*4)	—	400	600	μA

*1) Applicable to the following pins:
DIM1, DIM2, $\overline{BLANK}$, $\overline{TEST}$, $\overline{ZA}$, $\overline{HS}$, $\overline{MA}$, $\overline{A/C}$, and COLSEL

*2) Applicable to the following SEGMENT output pins:
1a and 3a, 1b and 3b, 1c and 3c, 1d and 3d, 1e and 3e, 1f and 3f, 1g and 3g, 2g, 2e, and 2f

*3) Applicable to the following SEGMENT output pins:
2a, 2d, 2b and 4b, 4c and 2c, and col

*4) f = 4.194304 MHz, Cg = Cd = 33pF, V_{CC} = 12V, open input, and non-loaded output

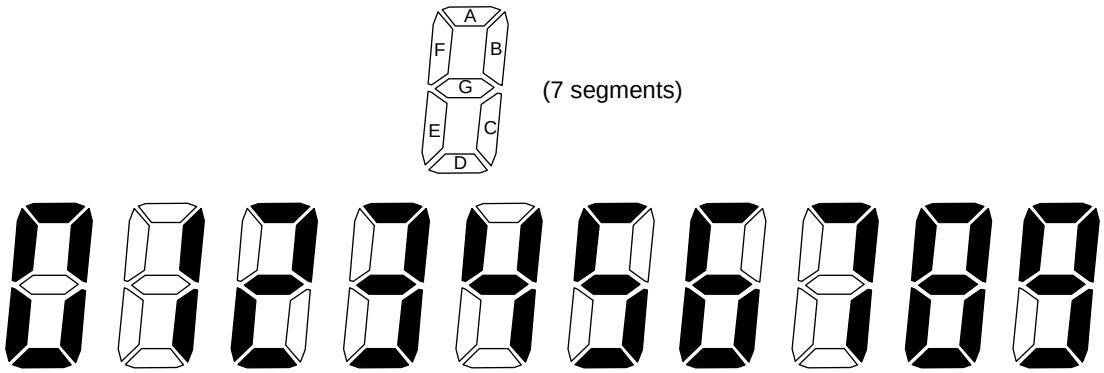
FUNCTIONAL DESCRIPTION

Time Base

Built-in 4.194304MHz crystal oscillation circuit (AMP, feedback resistor)

* Keep crystal and external capacitors as close to this LSI as possible to minimize connection wiring.
* The values of external components, such as crystal and capacitors, should be determined including capacitance of user's circuit boards. It is recommended to contact a crystal manufacturer.

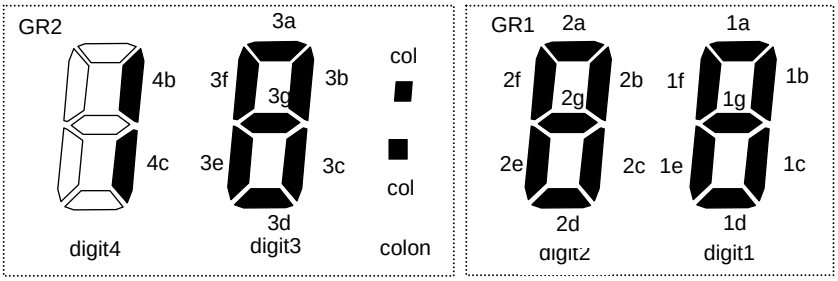
7-Segment Display Format



Display Device

Dynamic drive 4-digit fluorescent display tube (with colon)

Relationship Between Anode/Grid Output and Display



Brightness Switching Function

4-level brightness settings (frequency = 256 Hz, gap between GR1 and GR2 at 1/2 duty = 32 μs)

Switch pin name		Operating mode
DIM1	DIM2	
L	L	f = 256 Hz, 1/2 duty (50% display)
H	L	f = 256 Hz, 1/4 duty (25% display)
L	H	f = 256 Hz, 1/8 duty (12.5% display)
H	H	f = 256 Hz, 1/16 duty (6.25% display)

Display Mode

4-digit hour and minute display in 12-hour system
Hour display ····· 1 to 12
Minute display ····· 00 to 59
No time display when the most significant digit is 0 (Most Significant Digit Zero Suppress function)

Time Adjustment

Hour/Minute Fast-forwarding Function

Hour and minute can be fast-forwarded separately. The $\overline{HS}$ (Hours Set) pin fast-forwards the hour digits, and the $\overline{MS}$ (Minutes Set) pin fast-forwards the minute digits individually at 2Hz. One push counts one hour or one minute. When continuously pushed, hour or minute is incremented at 2Hz.

The $\overline{HS}$ and $\overline{MS}$ pins are held at a "H" level by a pull-up resistor in the open state, being in the no active state. These pins are placed in the active state by driving them at a "L" level externally.

The fast-forwarding of the hour and minute digits can be performed simultaneously.

When fast-forwarding the hour digits, the lower counter continues a regular operation, but the carry-over from the minute to the hour is not performed.

When fast-forwarding the minute digits, carry over to the hour digits is not performed.

Zero Adjustment Function (±30 minute reset to zero)

The $\overline{ZA}$ (Zero Adjust) pin is held at a "H" level by a pull-up resistor in the open state, being in the no active state. This pin is placed in the active state by driving it at a "L" level externally so that hours, minutes and seconds can be adjusted to zeros.

If the minute digits is less than 30 minutes, the minute and second digits are reset to 00'00".

Also, if the minute digits exceed 30 minutes, the minute and second digits are reset to 00'00", and the hour digits are carried over.

Moreover, the counter below seconds is reset up to 8 Hz.

<Examples of Zero Adjustments>

(X−1) hours 30 minutes 00 seconds
X hours 00 minutes 00 seconds
(X) hours 29 minutes 59 seconds
→ X hours 00 minutes 00 seconds

(X) hours 30 minutes 00 seconds
X hours 59 minutes 59 seconds
(X+1) hours 29 minutes 59 seconds
→ (X+1) hours 00 minutes 00 seconds

Blanking of Display

Blanking occurs in display by driving the $\overline{BLANK}$ pin at a "L" level externally.

Inputs from $\overline{HS}$, $\overline{MS}$, and $\overline{ZA}$ pins are disabled during blanking.

F64Hz Pin

This is the output pin for oscillation frequency adjustment, and constantly outputs a 64Hz signal.

External Reset

This device can be reset by placing the $\overline{A/C}$ pin at a "H" level.

After reset, the display starts at "1: 00".

Built-in Regulator Circuit

The built-in regulator circuit reduces the power supply voltage (V_{CC}) for the high voltage to the power supply voltage for logic , which is output to the VDDOUT pin.

Power is supplied to logic circuitry by connecting the VDDOUT pin to the VDDIN pin.

Power-on Reset

The power-on reset circuit built in this device eliminates the need for providing an external reset circuit.

* Do the followings to operate the power-on reset circuit properly:
  - Make a slope of a rise time of V_{CC} to a voltage equal to or larger than 8V/ms.
  - Connect a smoothing capacitor of 1000 pF±20% or more between the VDDOUT pin and GND.

$\overline{\text{TEST}}$ pin
This is the pin for testing this device.
This pin should be left open or fixed at a “H” level when not used.

Removal of Chatters
Three $\overline{\text{MS}}$, $\overline{\text{HS}}$ and $\overline{\text{ZA}}$ input pins are connected to the chatter removing circuits internally, and therefore chatters within 15.625 msec for each pin can be removed inside the device.

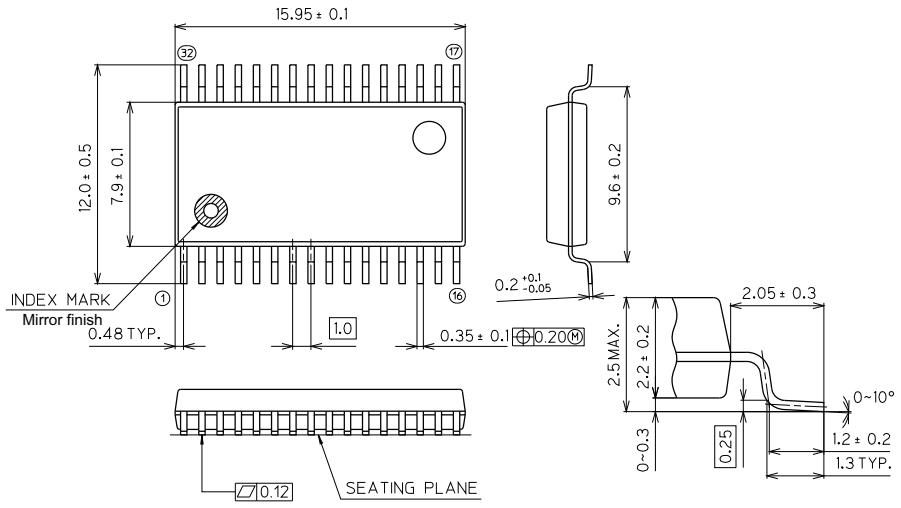
Colon Flashing/Lighting Select Function
Flashing or lighting of a colon can be selected by this COLSEL pin.

COLSEL	Operating mode
L	Flashing at 1 Hz
H	Lighting

PACKAGE DIMENSIONS

(Unit: mm)

SSOP32-P-430-1.00-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.60 TYP.
Rev. No./Last Revised	3/Dec. 5, 1996

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9298-01	Dec. 1, 2004	–	–	Preliminary edition 1
FEDL9298-01	July. 11, 2005	–	–	Final edition 1

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