BK2461

Datasheet

FLIP51 MCU+RF

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Revision History

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Table of Contents

1 Introduction 9
2 Feature 9
3 Block Diagram 10
4 PIN information 11
4.1 BK2461_QFN24 11
4.2 BK2461_SOP16 13
5 FLIP51 Micro-Controller 14
5.1 Instruction Set 14
5.2 MCU diagram 15
6 FLIP8051 address space 17
6.1 Overview 17
6.2 Program Memory (CODE space) 17
6.3 External Data Memory (XDATA space) 17
6.4 Internal Data Memory (IDATA space) 18
6.4.1 Internal Data memory organization 18
6.4.2 Internal ram: lower 128 byes 19
6.4.3 Internal Ram: Upper 128 Bytes 19
6.4.4 The Stack and the stack pointer 19
6.4.5 Special Function Registers 20
6.4.6 SFR table for MCU part 24
7 Power management 26
7.1 Power Control Register 26
7.2 Work State 27
7.2.1 IDLE MODE 27
7.2.2 SLEEP MODE 27
7.2.3 DEEP SLEEP MODE 27
7.2.4 Wake Up 28
8 Clock system 28
8.1 System clock topology 28
8.2 Peripherals clock management 29
9 Reset system 30
10 Interrupt system 31
10.1 7.1 Introduction 31
10.1.1 Interrupt source 31
10.1.2 Int0_n and int1_n 32
10.1.3 Intnmi interrupt 33
10.1.4 Additional interrupts 33
10.1.5 Timer Interrupts 34
10.1.6 Serial Port Interrupt 34
10.1.7 TRAP interrupt 34
10.2 Interrupt enable 34
10.3 Interrupt priority 35
10.4 Interrupt blocking conditions 37

CONFIDENTIAL

11 Peripheral module 38
11.1 OVERVIEW 38
11.2 UART 38
11.2.1 Serial port overview 38
11.2.2 Operation mode 38
11.2.3 Programming the Baud Rate 40
11.2.4 Serial port registers 41
11.1 ADC 43
11.1.1 introduction 43
11.1.2 Register explain 43
11.1.3 Sample rate: 44
11.1.4 ADC usage 44
11.2 PWM 45
11.2.1 OVERVIEW 45
11.2.2 FUNCTIONAL DESCRIPTION 45
11.2.3 Frequency of PWM 46
11.3 I2C master 47
11.3.1 Overview 47
11.3.2 List of I2CM register 47
11.3.3 I2C frame data format 51
11.3.4 Acknowledge 52
11.3.5 Clock synchronization and wait state 53
11.3.6 Master mode: Transmission 54
11.3.7 Master mode: Reception 58
11.3.8 Stop and Repeated Start 58
11.3.9 Reception FSM 60
11.3.10 Data Handling 60
11.3.11 Software Reset 61
11.4 Ext_timer 62
11.5 WDT 63
12 BK2461 RF transceiver 64
12.1 General Description 64
12.2 Abbreviations 66
12.3 State Control 67
12.3.1 State Control Diagram 67
12.3.2 Power Down Mode 68
12.3.3 Standby-I Mode 68
12.3.4 Standby-II Mode 68
12.3.5 TX Mode 68
12.3.6 RX Mode 69
12.4 Packet Processing 70
12.4.1 Packet Format 70
12.4.2 Packet Handling 72
12.5 Data and Control Interface 73
12.5.1 TX/RX FIFO 73
12.5.2 Interrupt 74

CONFIDENTIAL

12.6 RF Command 75
12.7 Register Map 77
12.7.1 Digital Register 77
12.7.2 Analog Register 84
12.7.3 TX power control setting 85
13 Typical Application Schematic 88
14 Package Information 89
15 Solder Reflow Profile 93
16 Order Information 94
17 Solder Reflow Profile 94
18 Contact Information 95

CONFIDENTIAL

List of Figures

FIGURE 1BK2461 BLOCK DIAGRAM 10
FIGURE 2 BK2461-QFN 11
FIGURE 3 BK2461-SOP 13
FIGURE 4 FLIP51 ARCHITECTURE 15
FIGURE 5 **FLIP51 SPACE** 17
FIGURE 6 ***INTERNAL DATA MEMORY*** 19
FIGURE 7 ***INTERNAL RAM LOWER 128 BYTES*** 19
FIGURE 8 WAKE UP PROCESS 28
FIGURE 9 CLOCK TOPOLOGY 29
FIGURE 10 ***SERIAL TRANSMIT MODE 1*** 39
FIGURE 11 ***SERIAL RECEIVE MODE 1*** 39
FIGURE 12 ***SERIAL TRANSMIT MODE 2*** 40
FIGURE 13 ***SERIAL RECEIVE MODE 2*** 40
FIGURE 14 ***ADC*** 43
FIGURE 15 ***PWM PARAMETER*** 46
FIGURE 16 *COMPLETE DATA TRANSFER* 51
FIGURE 17 ***"NOT ACKNOWLEDGE" BY SLAVE*** 52
FIGURE 18 ***"NOT ACKNOWLEDGE" BY MASTER (END OF TRANSMISSION)*** 53
FIGURE 19 ***CLOCK SYNCHRONIZATION AS HANDSHAKE*** 53
FIGURE 20 ***CLOCK SYNCHRONIZATION*** 54
FIGURE 21 ***TYPICAL TRANSMISSION*** 54
FIGURE 22 ***REPEATED START OR STOP CONDITION AFTER LAST BYTE*** 55
FIGURE 23 ***TRANSMISSION FSM*** 57
FIGURE 24 ***TYPICAL RECEPTION*** 58
FIGURE 25 ***REPEATED START OR STOP CONDITION AFTER LAST BYTE*** 59
FIGURE 26 ***RECEPTION FSM*** 60
FIGURE 27 BK2461 RF BLOCK DIAGRAM 65
FIGURE 28 PTX (PRIM_RX=0) STATE CONTROL DIAGRAM 67
FIGURE 29 PRX (PRIM_RX=1) STATE CONTROL DIAGRAM 68
FIGURE 30 PACKET FORMAT 70
FIGURE 31 CLASSIFICATION REFLOW PROFILE 93

CONFIDENTIAL

List of tables

TABLE 1 PIN DEFINITION 12
TABLE 2 PIN DEFINITION 14
TABLE 3 *SPECIAL FUNCTION REGISTERS MEMORY MAP* 24
TABLE 4 *CORE SFRS* 24
TABLE 5 *ADDITIONAL INTERRUPT SFRS* 24
TABLE 6 *I/O PORTS SFRS* 25
TABLE 7 *SERIAL PORT SFRS* 25
TABLE 8 *TIMERS SFRS* 26
TABLE 9 *BIRD SFRS* 26
TABLE 10 POWER MANAGEMENT REGISTER 26
TABLE 11 CLOCK ENABLE REGISTER 29
TABLE 12 *INTERRUPT SOURCES* 32
TABLE 13 *TIMER/COUNTER CONTROL REGISTER (TCON LOW)* 33
TABLE 14 *ADDITIONAL INTERRUPT REGISTERS* 33
TABLE 15 *ADDITIONAL INTERRUPT FLAG REGISTER (AIF)* 34
TABLE 16 *INTERRUPT ENABLE 0 REGISTER (IE0)* 35
TABLE 17 *ADDITIONAL INTERRUPT ENABLE REGISTER (AIE)* 35
TABLE 18 *INTERRUPT PRIORITY LEVELS AND VECTOR ADDRESSES* 36
TABLE 19 *INTERRUPT PRIORITY WITHIN A SAME PRIORITY LEVEL (0 OR 1)* 37
TABLE 20 *INTERRUPT PRIORITY REGISTER (IP)* 37
TABLE 21 *ADDITIONAL INTERRUPT PRIORITY REGISTER (AIP)* 37
TABLE 22 *SERIAL PORT REGISTERS* 41
TABLE 23 *SERIAL PORT CONTROL REGISTER (SCON)* 42
TABLE 26 ADC REGISTER 43
TABLE 27 ADC REGISTER 44
TABLE 28 ADC 的 SFR 44
TABLE 29 ADC REGISTER 44
TABLE 30 ADC REGISTER 44
TABLE 31 ADC ANALOG REGISTER 45
TABLE 24 *PWM REGISTER ADDRESS* 45
TABLE 25 *I2CM REGISTER* 47
TABLE 26 *I2CM CONTROL REGISTER (MCON)* 48
TABLE 27 *I2CM RECEIVE REGISTER (MRXBUF)* 48
TABLE 28 *I2CM TRANSMIT BUFFER (MTXBUF)* 48
TABLE 29 *I2CM MPRESC REGISTER* 48
TABLE 30 *I2CM STATUS REGISTER 0 (MSTAT0)* 49
TABLE 31 *I2CM STATUS REGISTER 1 (MSTAT1)* 49
TABLE 32 *I2CM INTERRUPT ENABLE REGISTER 0 (MIEN0)* 50
TABLE 33 *I2CM INTERRUPT ENABLE REGISTER 1 (MIEN1)* 50
TABLE 34 *I2CM CALL ADDRESS REGISTER (MCADDR)* 51
TABLE 35 *RESERVED ADDRESSES FOR I2CANSACTIONS* 52
TABLE 36 RTC REGISTER 62
TABLE 20 WATCH DOG REGISTER 63
TABLE 21 THE PRESCALE OF WATCH DOG CLOCK 63
TABLE 37 RF COMMAND 76
TABLE 38 DIGITAL REGISTER 84
TABLE 39 REGISTER BANK 1 85
TABLE 40 TX POWER SETTING 85
TABLE 41 SOLDER REFLOW PROFILE 93

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1 Introduction

The BK2461 is a RF SOC chip, which embedded the newest FLIP51 processor.

2 Feature

- 1.9 V to 3.6 V power supply
- FLIP51 MCU compatible with 8051
- A 4-stage pipeline architecture that enables to execute most of the instructions in a single clock cycle.
- 8k bytes OTP for program
- 256 Bytes IRAM and 512k Bytes SRAM
- Embedded three Timer/Counter
- Support UART I2C interface
- low power consumption, embedded with 32k RC oscillator
- Total 9/18 GPIO available
- The most 5 PWM available
- The embedded BIRD (Built-In Real-time Debugger) system for online debug
- 8+1 channel ADC embedded
- Integrated 2.4G RF transceiver
- The max output power can be 12DBm
- low power consumption, embedded with 32k RC oscillator

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3 Block Diagram

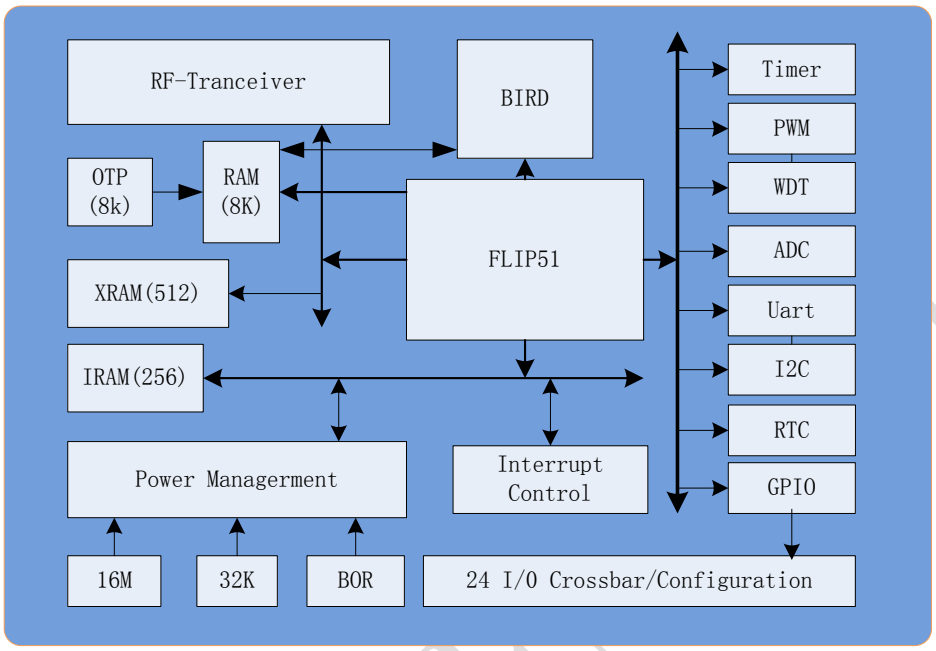


Figure 1BK2461 Block Diagram

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4 PIN information

4.1 BK2461_QFN24

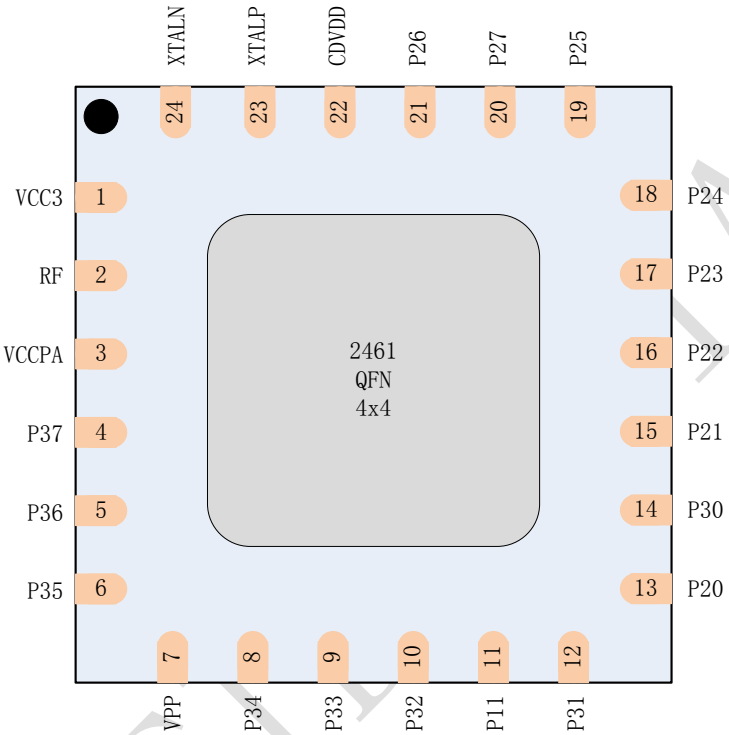


Figure 2 BK2461-QFN

Num.	Name	Pin Function	Description
1	VCC3	Power supply	3v supply
2	RF	Antenna input/output	
3	VCCPA	Analog output	PA power output, connected with decoupling CAP
4	P3.7	Digital I/O	General I/O，ADC input
5	P3.6	Digital I/O	General I/O，ADC input
6	P3.5	Digital I/O	General I/O，ADC input
7	VPP	Power supply	Mode select and 6.5V power supply for OTP burning, or P12 output(PWM)
8	P3.4	Digital I/O	General I/O，ADC input
9	P3.3	Digital I/O	General I/O，ADC input

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10	P3.2	Digital I/O	General I/O，ADC input
11	P1.1	Digital I/O	General I/O， external interrupt
12	P3.1	Digital I/O	General I/O，ADC input
13	P2.0	Digital I/O	General I/O，or input for UART
14	P3.0	Digital I/O	General I/O，ADC input
15	P2.1	Digital I/O	General I/O，or output for UART
16	P2.2	Digital I/O	General I/O，or I2C SCL
17	P2.3	Digital I/O	General I/O，or I2C SDA
18	P2.4	Digital I/O	General I/O，or PWM, or JTAG
19	P2.5	Digital I/O	General I/O，or PWM, or JTAG
20	P2.7	Digital I/O	General I/O，or PWM, or JTAG
21	P2.6	Digital I/O	General I/O，or PWM, or JTAG
22	CDVDD	Analog output	power output, connected with decoupling CAP
23	XTALP	Analog output	Oscillator output
24	XTALN	Analog input	Oscillator input

Table 1 PIN definition

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4.2 BK2461_SOP16

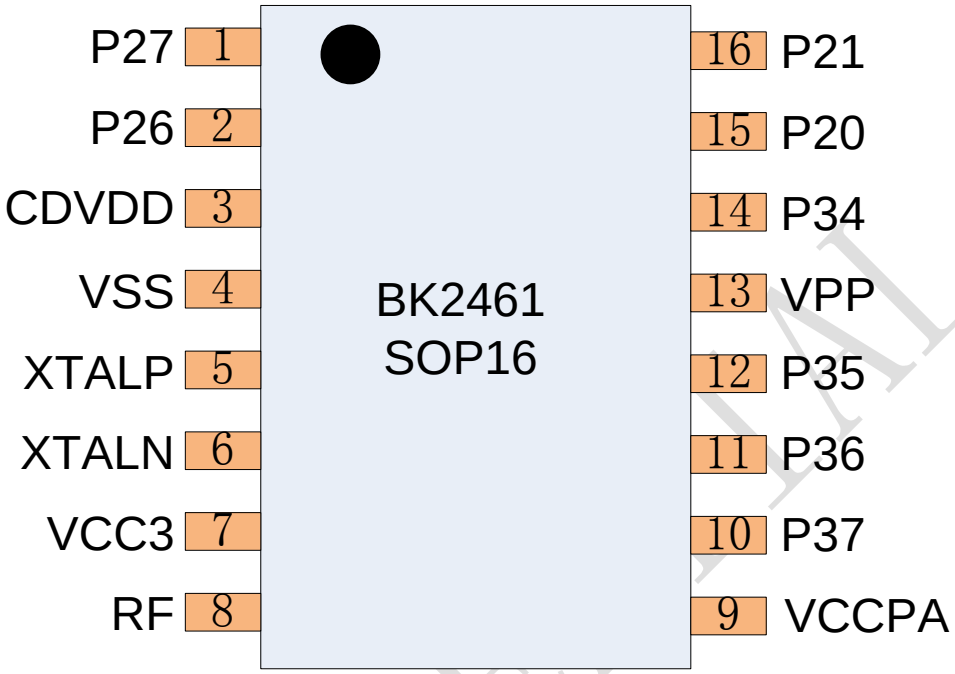


Figure 3 BK2461-SOP

NO.	Name	Pin Function	Description
1	P2.7	Digital I/O	General I/O，or PWM
2	P2.6	Digital I/O	General I/O，or PWM
3	CDVDD	Analog output	power output, connected with decoupling CAP
4	**VSS**	ground	
5	XTALP	Analog output	Oscillator output
6	XTALN	Analog input	Oscillator input
7	VCC3	Power supply	3v supply
8	RF	Antenna input/output	
9	VCCPA	Analog output	PA power output, connected with decoupling CAP
10	P3.7	Digital I/O	General I/O，ADC input ,OTP download
11	P3.6	Digital I/O	General I/O，ADC input ,OTP download
12	P3.5	Digital I/O	General I/O，ADC input ,OTP download
13	VPP	Power supply	Mode select and 6.5V power supply for OTP burning, or P12 output
14	P3.4	Digital I/O	General I/O，ADC input ,OTP download

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15	P2.0	Digital I/O	General I/O，or input for UART
16	P2.1	Digital I/O	General I/O，or output for UART

Table 2 PIN definition

5 FLIP51 Micro-Controller

5.1 Instruction Set

The FLIP8051 is an improved option of the 80c51 microcontroller. It is 100% binary code upward compatible with the legacy 80c51.

Its pipeline architecture provides an increase of processing speed an average nine times, when running at the same clock frequency as a standard 80c51 real component.

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5.2 MCU diagram

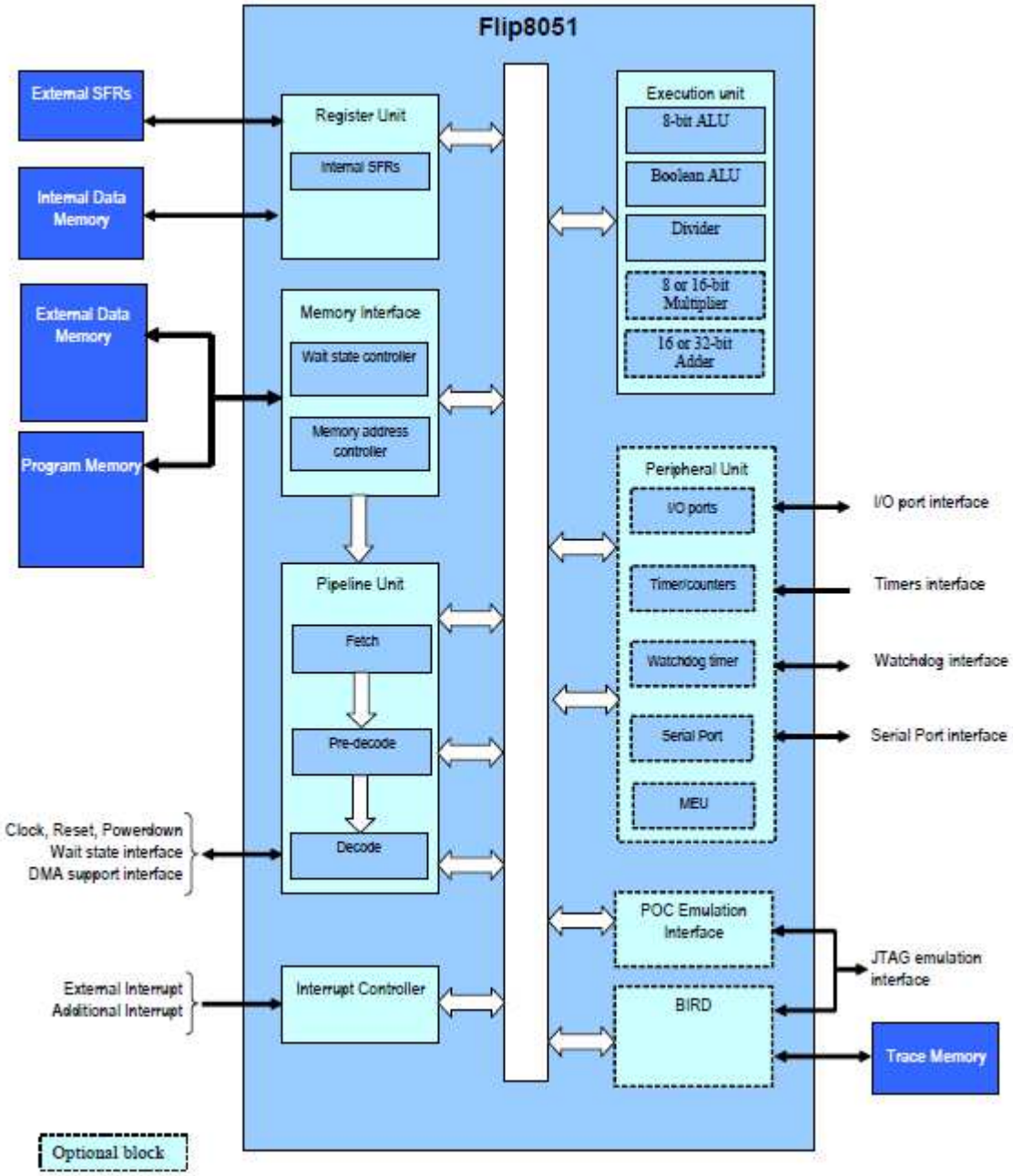


Figure 4 FlIP51 architecture

6 Development and download

The BK2461 have some different development and download methods. The working mode is decided by the VPP voltage when power up. The next table describes the different working mode.

VPP voltage	mode	description	Note
6.5+-0.5	OTP burning mode	GPIO mapping to OTP download mode.	P3.4=spi_mosi P3.5=spi_miso P3.6=spi_clk P3.7=spi_cs
3+-0.5	DEBUG mode	GPIO mapping to BIRD interface used to debug on chip. At this mode, the program can be loaded to the chip from JTAG interface.	P2.4=TDO P2.5=TDI P2.6=TMS P2.7=TCK
1.2+-0.5	FLASH download mode	At this mode, BK2461 load program from the outside FLASH firstly, then run the loaded program	P3.4=boot_si P3.5= boot_s0 P3.6= boot_sck P3.7= boot_csn
0+-0.5	Normal mode (product mode)	At this mode, BK2461 run the program from the OTP directly.	

Table 3 *work mode selection*

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7 FLIP8051 address space

7.1 Overview

The memory organization of the Flip8051 is similar to that of standard 80C51. There are three separate memory spaces: CODE space (program memory), the XDATA space (external data memory) and the IDATA space (internal data memory).

These memory spaces shared the same address space but are accessed with different instruction types.

There are organized as follow for BK2461:

- CODE space: up to 8K Bytes of addressing range
- XDATA space: up to 512 Bytes of addressing range
- IDATA space: up to 256 Bytes.

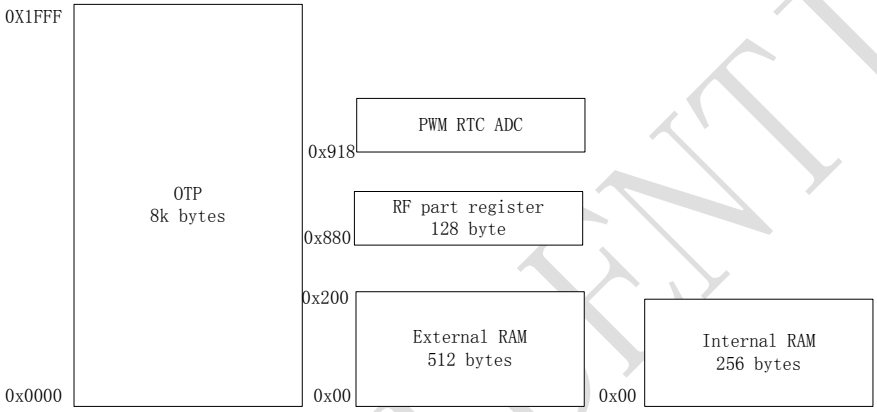


Figure 5 **FLIP51 SPACE**

7.2 Program Memory (CODE space)

The Flip8051 has a 64K Bytes **CODE** space (8K for BK2461). Program memory is normally assumed to be read only and can be accessed only by MOVC instruction (or of course by the instruction fetch)

Two addressing modes are available for MOVC instructions:

- 16-bit data pointer (@A+DPTR).

The MOVC instructions use these indirect modes to access the current 64 K page of the code memory.

- 16-bit program counter (@A+PC).

The MOVC instruction uses this indirect mode to access the 64 K page of the code memory.

7.3 External Data Memory (XDATA space)

The **External Data memory** shares address bus with program memory. This data space can be up to 64K Bytes (512 for BK2461).

The external data memory can be accessed only by the standard MOVX instructions (plus some new instructions of the WHIRL instruction set)

Two addressing modes are available for MOVX instructions:

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 Byte register (@Ri, i = 0,1).

Registers R0 and R1 indirectly address external data memory locations 00h-FFh. When MOVX instructions use this indirect mode, the MSB of the 16-bit address is filled with the content of MPAGE SFR (0A1h). Then, it allows MOVX @Ri instruction to access to 64K Bytes of external data memory. Usually, in 80C51 application, the Port 2 is used to this address extension. In order to keep software compatibility with existing 80C51 program, the register MPAGE is also updated by any value written at P2 register.

 16-bit data pointer (@DPTR).

The MOVX instructions use these indirect modes to access the page of the external data RAM pointed by the extended data pointer (DPX).

7.4 Internal Data Memory (IDATA space)

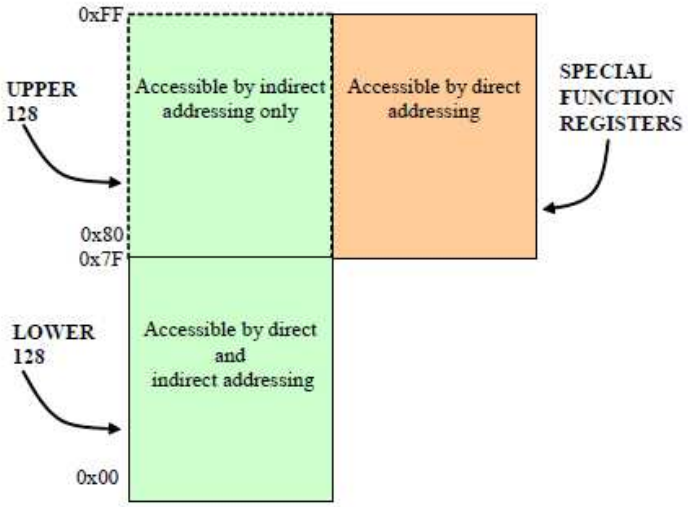
The **Internal data memory** is composed by 256 bytes of internal RAM and by a number of SFRs.

The main difference between these IDATA and XDATA spaces is the kind of instructions that enable to access to these memories. Most of the “data transfer” instructions are dedicated to access internal data memory (IDATA) since there are only four instructions (MOVX) dedicated to access external data memory. Moreover, only indirect addressing mode is available for XDATA whilst IDATA can be addressed by register, direct, register-indirect or immediate addressing mode. This provides a higher flexibility to access data. In addition, the Flip8051 memory interface with IDATA space is optimized and then access time to this space is faster than the access time of XDATA for both read/write operations.

7.4.1 Internal Data memory organization

The internal data memory is divided into 3 spaces, which are referred to as the **Lower 128**, **Upper 128** and **SFR space**. Either direct or indirect addressing may be used to access the **lower 128** bytes of internal data memory. The **upper 128** bytes of internal data memory are accessible by indirect addressing only while direct addressing to region above 0x7F will access **SFR space**.

In the Flip8051, the SFRs are implemented internally to the model using Flip-Flops.



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Figure 6 ***Internal Data memory***

7.4.2 Internal ram: lower 128 byes

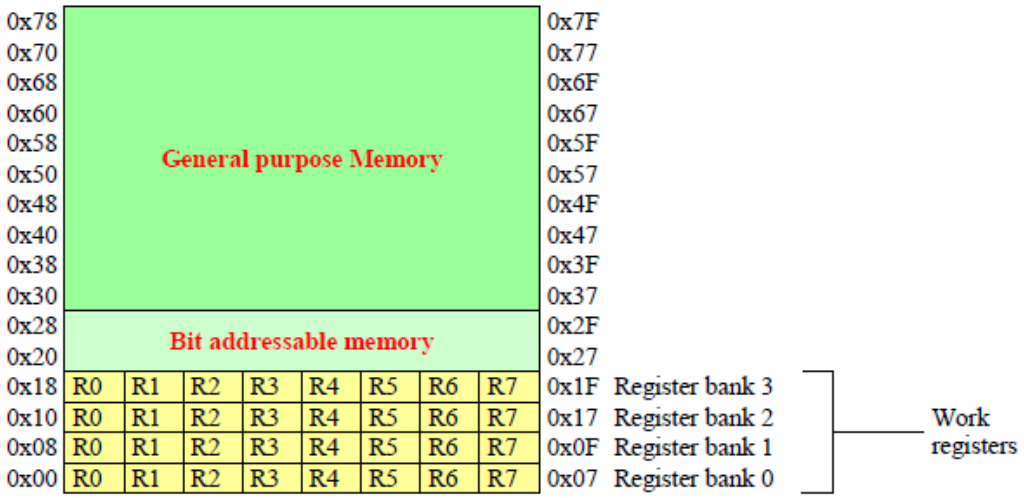


Figure 7 ***Internal Ram lower 128 bytes***

The lower 128 bytes of Internal Data Memory is organized in three distinct areas:
0x00-0x1F: The Register Banks are at the lowest 32 bytes of the internal data memory. Only one Register Bank is used at a time when an instruction uses R0 to R7. 2 bits in Processor Status Word (PSW), called RS1 and RS0, control the selection of the Register Bank. Bank 0 is selected upon reset. Indirect addressing mode used R0 and R1 as index registers
0x20-0x2F: This memory space contains a general-purpose memory, which is bit addressable as well as byte addressable. The bit address ranged from 0 to 0x7F. When bit addressing is used in an instruction, the bit access in this region will occur. In this memory range, when bit addressing is used, bit address 0x00 is the bit 0 of address 0x20 while bit 7 of of the byte 0x20 has bit address 0x07. Bit address 0x7F is the bit 7 of address 0x2F. A bit access is different than a byte access by the type of instruction used.
0x30-0x7F: A general-purpose byte-addressable memory is located above address 0x30. It can be accessed both by direct or indirect addressing mode.

7.4.3 Internal Ram: Upper 128 Bytes

The usage of the addresses between 0x80 and 0xFF is up to the user. This memory can be used for any purpose providing that indirect addressing mode is used when accessing this memory space, otherwise the Special Function Register memory will be accessed.

7.4.4 The Stack and the stack pointer

The stack refers to an area of internal RAM that is used in conjunction with certain instructions (PUSH, POP) to store and retrieve data quickly. The Stack pointer register (SP, 0x81) is used to hold an internal RAM address that is called the “top of the stack”. The data held in the SP register is the address in internal RAM where the last byte of data was stored by a stack operation. The reset value of Stack pointer register is 0x07 and can be changed to any internal RAM address by the programmer. Usually, the stack is located high in the RAM to avoid conflict with the work register, bit and byte area in internal RAM.

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7.4.5 Special Function Registers

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). All the special function registers of the original 80C51 are present in the Flip8051. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, P1, SCON, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only.

The special function registers (SFRs) reside in their associated peripherals or in the core. The following tables shows the SFR address space with the SFR mnemonics and reset values. Unoccupied locations in the SFR space are unimplemented, i.e. no register exists. If an instruction attempts to write to an unimplemented SFR location, the instruction executes, but nothing is actually written. If an unimplemented SFR location is read, it returns an unspecified value.

SFR Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	addr
									0x80
SP	-	-	-	-	-	-	-	-	0x81
DPL	-	-	-	-	-	-	-	-	0x82
DPH	-	-	-	-	-	-	-	-	0x83
CKCON	CKDIV1	CKDIV0	smod0	x	x	x	x	x	0x84
CLK_EN CFG	adc_en	timer_en	uart_en	pwm_en	spi_en	i2c_en	aes_mud_ en	wdt_en	0x85
PCON2	SMOD	EUSB	CMD_RS T	Latch_en	deep_sleep	OSC32k	RC32k	IDLE	0x86
									0x87
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	0x88
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	0x89
TL0	-	-	-	-	-	-	-	-	0x8A
TL1	-	-	-	-	-	-	-	-	0x8B
TH0	-	-	-	-	-	-	-	-	0x8C
TH1	-	-	-	-	-	-	-	-	0x8D
CCMCON	-	-	-	-	-	-	-	-	0x8E
CCMVAL	-	-	-	-	-	-	-	-	0x8F
P1	-	-	-	-	-	-	-	-	0x90
									0x91
DPSEL	x	x	x	x	x	x	x	DPSEL0	0x92
P1IN_EN	-	-	-	-	-	-	-	-	0x93
P2IN_EN	-	-	-	-	-	-	-	-	0x94
P3IN_EN	-	-	-	-	-	-	-	-	0x95
									0x96

MMS	-	-	-	-	-	-	-	-	0x97
SCON0	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	0x98
SBUF0	-	-	-	-	-	-	-	-	0x99
									0x9A
PAGE_A（NA）	x	x	x	x	x	x	x	x	0x9B
PAGE_B（NA）	x	x	x	x	x	x	x	x	0x9C
PAGE_C（NA）	x	x	x	x	x	x	x	x	0x9D
P1OUT_N	-	-	-	-	-	-	-	-	0x9E
P2OUT_N	-	-	-	-	-	-	-	-	0x9F
P2	-	-	-	-	-	-	-	-	0xA0
MPAGE	-	-	-	-	-	-	-	-	0xA1
									0xA2
									0xA3
									0xA4
P3OUT_N	-	-	-	-	-	-	-	-	0xA5
WDT	x	x	x	state	x	ps2	ps1	ps0	0xA6
									0xA7
IE	EA	x	ET2	ES	ET1	EX1	ET0	EX0	0xA8
									0xA9
P1_PU	-	-	-	-	-	-	-	-	0xAA
P2_PU	-	-	-	-	-	-	-	-	0xAB
P3_PU	-	-	-	-	-	-	-	-	0xAC
									0xAD
									0xAE
P1_PD	-	-	-	-	-	-	-	-	0xAF
P3	-	-	-	-	-	-	-	-	0xB0
									0xB1
									0xB2
									0xB3
P2_PD	-	-	-	-	-	-	-	-	0xB4
P3_PD	-	-	-	-	-	-	-	-	0xB5
									0xB6
									0xB7
IP	-	-	-	-	-	-	-	-	0xB8
									0XB9
									0xBA

									0xBB
									0xBC
									0xBD
									0xBE
									0xBF
AIF	-	-	-	-	-	-	-	-	0xC0
									0xC1
									0xC2
									0xC3
									0xC4
									0xC5
									0xC6
									0xC7
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	0xC8
									0xC9
RCAP2L	-	-	-	-	-	-	-	-	0xCA
RCAP2H	-	-	-	-	-	-	-	-	0xCB
TL2	-	-	-	-	-	-	-	-	0xCC
TH2	-	-	-	-	-	-	-	-	0xCD
									0xCE
									0xCF
PSW	-	-	-	-	-	-	-	-	0xD0
									0xD1
I2CM DATA_IE	x	x	ETBE	x	ETBF	ERBE	x	ERBF	0xD2
									0xD3
I2CM CALLADDR0	RWN	CADDR[6]	CADDR[5]	CADDR[4]	CADDR[3]	CADDR[2]	CADDR[1]	CADDR[0]	0xD4
									0xD5
									0xD6
									0xD7
									0xD8
P1_OPDR	-	-	-	-	-	-	-	-	0xD9
P2_OPDR	-	-	-	-	-	-	-	-	0xDa
P3_OPDR	-	-	-	-	-	-	-	-	0xDb
									0xDc
									0xDd
									0xDe

									0xDf
ACC	-	-	-	-	-	-	-	-	0xE0
I2CM CTRL	x	x	WAIT	x	STOP	SRST	STA	BUSY	0xE1
I2CM RXDATA	-	-	-	-	-	-	-	-	0xE2
I2CM TXDATA	-	-	-	-	-	-	-	-	0xE3
I2CM PRESC	-	-	-	-	-	-	-	-	0xE4
I2CM TXRX_STS		x	x	DNA	SANA	UNF	OVF	NEND	0XE5
I2CM DATA_STS	x	x	TBE	x	TBF	RBE	x	RBF	0XE6
I2CM TXRX_IE	x	x	x	EDNA	ESANA	EUNF	EOVF	ENEND	0xE7
AIE	-	-	-	-	-	-	-	-	0xE8
PALT0	x	x	T2_EX_EN	T2_IN_EN	T1_IN_EN	T0_IN_EN	EX1_IN_EN	EX0_IN_EN	0xE9
EXSLEEP	x	x	x	x	x	x	exsleep2	ex_sleep1	0xEA
									0xEB
P1_WUEN	-	-	-	-	-	-	-	-	0xEC
P2_WUEN	-	-	-	-	-	-	-	-	0xED
P3_WUEN	-	-	-	-	-	-	-	-	0xEE
									0xEF
B									0xF0
									0xF1
									0xF2
									0xF3
									0xF4
									0xF5
									0xF6
PALT1 (W only)	PWM4_IO_EN	PWM3_IO_EN	PWM2_IO_EN	PWM1_IO_EN	PWM0_IO_EN	UART0_IO	SPI_IO	I2C_IO	0xF7
AIP	-	-	-	-	-	-	-	-	0xF8
									0xF9
P1_WUMOD	-	-	-	-	-	-	-	-	0xFA
P2_WUMOD	-	-	-	-	-	-	-	-	0xFB
P3_WUMOD	-	-	-	-	-	-	-	-	0xFC
									0xFD
									0xFE

									0xFF

Table 4 ***Special Function Registers Memory Map***

7.4.6 SFR table for MCU part

Register	Address	Description	Reset value
ACC	0xE0	Accumulator	00h
B	0xF0	B Register	00h
DPH	0x83	Data Pointer high byte	00h
DPL	0x82	Data Pointer low byte	00h
DPSEL	0x92	Data Pointer selection	00h
IE	0xA8	Interrupt Enable Control	00h
IP	0xB8	Interrupt Priority Control	00h
MPAGE	0xA1	Memory page register	00h
PCON2	0x86	Power Control	00h
PSW	0xD0	Program Status Word	00h
SP	0x81	Stack Pointer	07h
ACC	0xE0	Accumulator	00h
B	0xF0	B Register	00h
DPH	0x83	Data Pointer high byte	00h
DPL	0x82	Data Pointer low byte	00h
DPSEL	0x92	Data Pointer selection	00h
IE	0xA8	Interrupt Enable Control	00h
IP	0xB8	Interrupt Priority Control	00h
MPAGE	0xA1	Memory page register	00h
PCON	0x87	Power Control	00h
PSW	0xD0	Program Status Word	00h
SP	0x81	Stack Pointer	07h

Table 5 ***Core SFRs***

Register	Address	Description	Reset value
AIE	0xE8	Additional interrupt enable	00h
AIF	0xC0	Additional interrupt flag	00h
AIP	0xF8	Additional interrupt priority	00h

Table 6 ***Additional interrupt SFRs***

Register	Address	Description	RST value
P0	0x80	Port0 value	0xFF
P0IN_EN_	0x91	Port input enable, active high	0xFF
P0OUT_N_	0x9A	Port output enable, active low	0xFF
P0_PU	0xA9	Port pull-up selection	0xFF
P0_PD	0xAE	Port pull-down selection	0x00
P0_OPDR	0xD8	Open drain selection	0x00
P0_WUEN	0xEB	Port wake up enable	0x00
P0_WKMOD	0xF9	Port wake up mode selection	0x00

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P1	0x80	Port0 value	0xFF
P1IN_EN_	0x93	Port input enable, active high	0xFF
P1OUT_N_	0x9E	Port output enable, active low	0xFF
P1_PU	0xAA	Port pull-up selection	0xFF
P1_PD	0xAF	Port pull-down selection	0x00
P1_OPDR	0xD9	Open drain selection	0x00
P1_WUEN	0xEC	Port wake up enable	0x00
P1_WKMOD	0xFA	Port wake up mode selection	0x00
P2	0xA0	Port0 value	0xFF
P2IN_EN_	0x94	Port input enable, active high	0xFF
P2OUT_N_	0x9F	Port output enable, active low	0xFF
P2_PU	0xAB	Port pull-up selection	0xFF
P2_PD	0XB4	Port pull-down selection	0x00
P2_OPDR	0xDA	Open drain selection	0x00
P2_WUEN	0xED	Port wake up enable	0x00
P2_WKMOD	0xFB	Port wake up mode selection	0x00
P3	0xB0	Port0 value	0xFF
P3IN_EN_	0x95	Port input enable, active high	0xFF
P3OUT_N_	0Xa5	Port output enable, active low	0xFF
P3_PU	0xAC	Port pull-up selection	0xFF
P3_PD	0xB5	Port pull-down selection	0x00
P3_OPDR	0xDB	Open drain selection	0x00
P3_WUEN	0xEE	Port wake up enable	0x00
P3_WKMOD	0xFC	Port wake up mode selection	0x00
P4	0xB7	Port0 value	0xFF
P4IN_EN_	0x96	Port input enable, active high	0xFF
P4OUT_N_	0xa7	Port output enable, active low	0xFF
P4_PU	0xAD	Port pull-up selection	0xFF
P4_PD	0xB6	Port pull-down selection	0x00
P4_OPDR	0xDC	Open drain selection	0x00
P4_WUEN	0xEF	Port wake up enable	0x00
P4_WKMOD	0xFD	Port wake up mode selection	0x00

Table 7 *I/O ports SFRs*

NOTE: some ports are not available in BK2461, please refer to the package information.

Register	Address	Description	Reset value
SBUF	0x99	Serial Buffer	00h
SCON	0x98	Serial Control	00h

Table 8 *Serial Port SFRs*

Register	Address	Description	RST value
T2CON	0xC8	Timer/Counter 2 control	00h
TCON	0x88	Timer/Counter 0 and 1 control	00h

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TH0	0x8C	Timer/Counter 0 high byte	00h
TH1	0x8D	Timer/Counter 1 high byte	00h
TH2	0xCD	Timer/Counter 2 high byte	00h
TL0	0x8A	Timer/Counter 0 low byte	00h
TL1	0x8B	Timer/Counter 1 low byte	00h
TL2	0xCC	Timer/Counter 2 low byte	00h
TMOD	0x89	Timer/Counter 0 and 1 mode control	00h
RCAP2H	0xCB	Timer 2 Reload/Capture high byte	00h
RCAP2L	0xCA	Timer 2 Reload/Capture low byte	00h
WDTRST	0xA6	WDT enable register	00h

Table 9 *Timers SFRs*

Register	Address	Description	RST value
CCMCON	0x8E	BIRD Communication Control	00h
CCMVAL	0x8F	BIRD Communication Value	00h
MMS	0x97	Reserved for emulation purpose	07h

Table 10 *BIRD SFRs*

8 Power management

For applications where power consumption is critical, the BK2461 provides all kinds of power saving modes.

8.1 Power Control Register

PCON2	7	6	5	4	3	2	1	0
0x87	SMOD	EUSB	CMD_RST	Latch_en	Deep_sleep	OSC32K_sel	RC32k_sel	IDLE

Table 11 power management register

SMOD: – Serial Port 0 baud rate doublers enable. When SMOD0=1, the baud rate for Serial Port 0 is doubled.

EUSB: R/W by software only. USB enable, the 48MHz clock will exist when EUSB=1.

CMD_RST: Write 1 to reset MCU (not include RF part).

Latch_en: this register used for deep sleep mode. In deep sleep mode, the power supply to digital part will be shut down, but the GPIO setting must be hold use this register.

Deep_sleep: System will enter deep sleep mode when setting this register. The lowest current consumption can be got by setting this register.

RC32k_sel: System will select RC32k clock when write 1 to this position. Interrupts and software can clear it.. In this state, the system clock changed to 32K RC clock, so the power consumption is very low.

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OSC32k_sel: System will select OSC32k (divided by OSC16M) clock when write 1 to this position. Interrupts and software can clear it. In this state, the system clock changed to 32K OSC clock, so the power consumption will decrease evidently.

Please note that OSC32k clock is more accurate than RC 32k clock, but need more power consumption.

IDLE: When set by software, system enter stop mode, and it can only be wake up by enabled interrupt.(Clear it to 0 by hardware). In this state, the most of clocks are shut down for power saving.

Note: set RC32k_sel and IDLE bit simultaneously can get the lowest power consumption, and in this state, all the register settings are retained.

8.2 Work State

8.2.1 IDLE MODE

An instruction that sets the IDLE bit (PCON2.0) causes the FLIP51 to enter idle mode when that instruction completes. In idle mode, CPU processing is suspended, internal registers maintain their current data. However, unlike the standard 8051, the clock is not disabled internally.

Activation of any enabled interrupt causes the hardware to clear the IDLE bit and terminate idle mode.

In idle mode, the power consumption is decreased evidently.

8.2.2 SLEEP MODE

An instruction that sets the IDLE bit (PCON2.0) causes the FLIP51 to enter idle mode when that instruction completes. Also, you can decrease the power consumption to a lower level thanks for the register PCON2.1. When setting the register, the system clock changed from 16MHz to RC32KHz. We define this state as sleep mode.

After reset, the system will enter normal mode running at 16MHz immediately.

Note: You should always clear PCON2.6 to 0 to save current when USB module doesn't need work at any time.

As showed above, the IDLE bit decide CPU run or not, the PCON2.1 bit decide the system clock source. (16MHz or RC32KHz)

8.2.3 DEEP SLEEP MODE

If you want to get the lowest power consumption, you can let BK2461 enter deep sleep mode. Firstly, you should set all the GPIO to certain setting , then, set latch_en (PCON2 [4]) to latch all the register setting, lastly, set deep sleep bit (PCON2 [3]) to enter deep sleep status. In this state, the power supplied to digital will be shut down.
Note: after wake up from this state, the instruction will run from the address zero.

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8.2.4 Wake Up

8.2.4.1 Wake Up from sleep mode

When the MCU entered IDLE/SLEEP mode, all the enabled GPIO ports and interrupt sources can be used to wake up the MCU separately. Configure the corresponding SFR bit can enable or disenable the wake up function.

PX_WKEN: port x wake up enable or disable 0: disable; 1: enable

PX_WKMOD: wake up mode setting. 0: low level trigger; 1: edge trigger

You can get the detail GPIO register address from SFR table part.

The process wake up from sleep mode is showed in next figure.

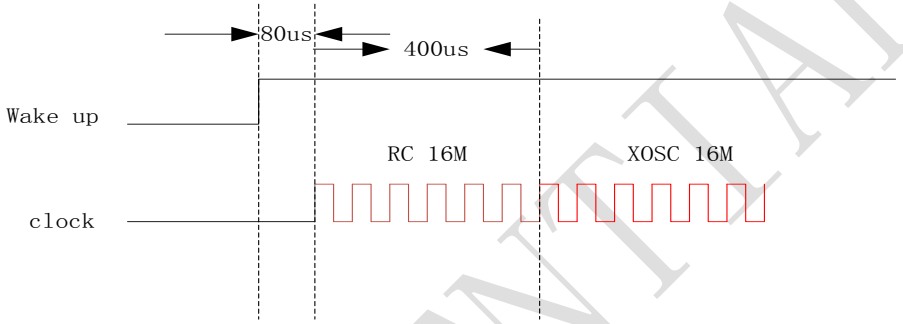


Figure 8 wake up process

After wake up, RC 16M clock will spend 80us to wake up, and after 400us, the clock source will switch to XOSC 16M automatically. RC 16M clock is not very accurate, so, during this period, you can only run ordinary MCU instruction, but cannot send or receive RF package.

Please note that: The RF part will also resume 120us for PLL locking after power up RF part. So, if you want to send/receive package through RF, you should wait 600us after wake up from sleep mode.

8.2.4.2 Wake up from deep sleep mode

All the ports can be set to wake up MCU from deep sleep status; also, you can enable or disable them separately. After wake up from deep sleep, a POR will be generated to reset the whole digital system.

9 Clock system

9.1 System clock topology

The BK2461 clock topology is showed as below. There are two clock sources, one is 16M, and the other is RC32k. You can select them by setting register according.

If the wake up time is a critical parameter for some application, a RC16M clock can be used before the OSC16M oscillating. To do this, the register XXX must be set as xxx.

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The clock source of ext timer is always fixed to 32k. In working mode, the OSC32K is used for counter, and in idle mode, the RC32k can be automatically selected. The ext timer is very suitable used for the application which has periodic behavior, such as mouse.

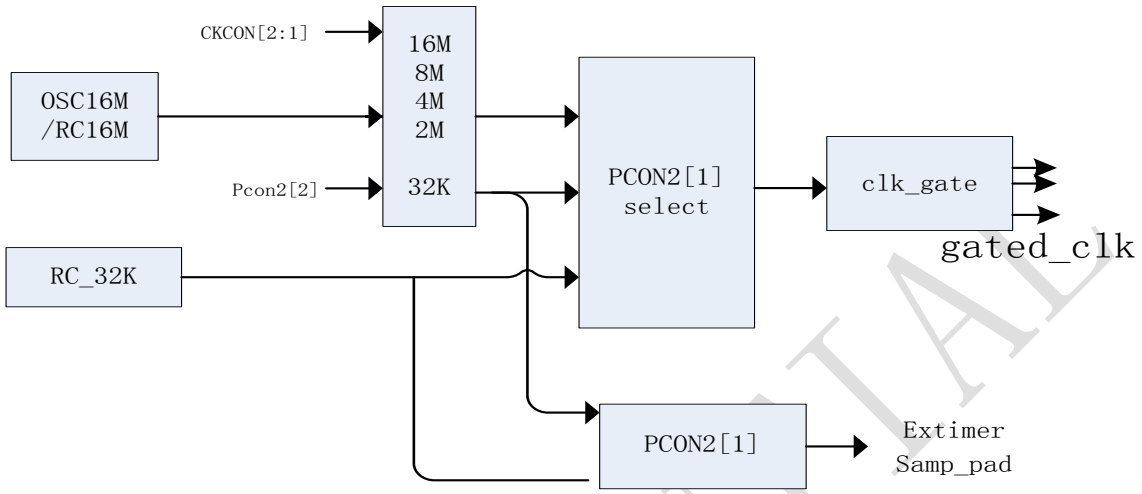


Figure 9 clock topology

9.2 Peripherals clock management

The peripherals clock source can be enabled or disenabled, to do this, you can refer to the next register. Evidently, the clock must be enabled when you want to use some peripheral equipment.

CLK_EN_CFG	7	6	5	4	3	2	1	0
0x85	**adc_en**	**timer_en**	**uart_en**	**pwm_en**		**i2c_en**		**WDT_en**

Table 12 clock enable register

CLK_EN_CFG: this register can use to power on or off all the peripheral equipment clocks for saving power.

adc_en : ADC clock enable or not (1 enable)
timer_en : TIMER 0 /1 /2 clock enable or not (1 enable)
uart_en : UART clock enable or not (1 enable)
pwm_en : PWM clock enable or not (1 enable)
i2c_en : I2C clock enable or not (1 enable)
WDT_en : MDU clock enable or not (1 enable)

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10 Reset system

There are three active low reset source in BK2461, they are power on reset, reset pin, watch dog reset. After reset, the MCU will re-start from address 0.

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11 Interrupt system

The Flip8051 has the same interrupt sources as the original 80C51. These are handled the same as on the original 80C51, however the Flip8051 has a shorter interrupt latency period, and can distinguish shorter external interrupt pulses. The interrupt sources are sampled every clock cycle (clock rising edge), and the decision of whether an interrupt will be accepted takes place at the last clock cycle of each instruction execution, or every clock cycle during idle mode.

11.17.1 Introduction

When an enabled interrupt occurs, this operation branches to a subroutine and performs some service in response to the interrupt. When the subroutine completes, execution resumes at the point where the interrupt occurred. Interrupts may occur as a result of internal activity (e.g. timer0 overflow) or at the initiation of an external device (external interrupt pin). In any case, interrupt operation is programmed by the system designer, who determines the priority of interrupt service, compare to relative normal code execution or other interrupt service routines. All the interrupts may be enabled / disabled dynamically by the system designer except the TRAP (software) and the NMI that are non-maskable.

A typical interrupt process occurs as follow:

An interrupt event on the signal, connected to an input pin and sampled by the Flip8051, is registered into a flag buffer.

 The priority of the flag is compared to the priority of the other interrupt by the interrupt controller. A higher priority causes the controller to set an interrupt flag.

 The setting of the interrupt flag indicates to the control unit to execute a context switch. This context switch breaks the current instruction execution flow1. The control unit completes the current instruction execution prior to saving the two bytes of the program counter (PC) and reloads the PC with the interrupt vector address, which is the start address of a software service routine.

The software service routine performs the assigned tasks and executes a RETI instruction as a final instruction. This instruction signals the completion of the interrupt, resets the interrupt-in-progress priority. The RETI instruction reloads the two bytes of the program counter and uses them as the 16-bit return address. Program execution then continues from the original point of interruption.

11.1.1 Interrupt source

The Flip8051 has one software interrupt, the TRAP instruction (always enabled) and up to fifteen interrupt sources controlled by hardware. Fourteen of these hardware interrupt are maskable interrupt sources and one is non-maskable (*intnmi* input, always enabled). The maskable sources include two external interrupts (*int0_n* and *int1_n*), three timer interrupts (timers 0, 1, and 2), and one serial port (UART) interrupt. Depending on configuration, eight additional external interrupt (*intextra_n[7:0]*) are available and maskable.

Each interrupt (except TRAP and *intnmi*) has an interrupt request flag, which can be set by software as well as by hardware. For some interrupts, hardware clears the request flag when it grants an interrupt. Software can clear any request flag to cancel an impending interrupt.

For BK2461, the available interrupts are showed in the next table:

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Interrupt Number	Interrupt Flag	Interrupt Source	Interrupt Routine Code Address
0	EX0	NA	
1	ET0	Flip8051 Timer0 Interrupt	0x0013
2	EX1	GPIO P1.1 Input	0x000B
3	ET1	Flip8051 Timer1 Interrupt	0x001B
4	UART	RI+TI	0x0023
5	TF2+EXF2	Flip8051 Timer2 Interrupt	0x002B
6	TRAP		0x0033
7	Intnmi	NA	
8	EX2	NA	
9	EX3	I2CM Interrupt	0x004B
10	EX4	NA	
11	EX5	BK2401 Transceiver Interrupt	0x005B
12	EX6	External Timer Interrupt	0x0063
13	EX7	NA	
14	EX8	ADC Interrupt	0x0073
15	EX9	NA	

Table 13 *interrupt sources*

11.1.2 Int0_n and int1_n

External interrupt *int0_n (not available for BK2461)* and *int1_n* may be each programmed to be level-activated or transition-activated, depending on bits IT0 and IT1 in TCON register. External interrupts are enabled with bits EX0 and EX1 in IE register. Events on *int0_n* or *int1_n* set respectively the interrupt request flag IE0 or IE1 in TCON register. If the interrupt is transition-activated, the hardware jump to the service routine clears the request flag. Otherwise, if the interrupt is level activated, then the interrupt must be de-asserted before the end of the ISR.

External interrupt pins must be de-asserted for at least two clock cycles prior to a request. External interrupt inputs are sampled at each clock cycle. A level-triggered interrupt pin held low or high for any two clock cycles time period guarantees detection. Edge-triggered external interrupts must hold the request pin low for at least two clock cycles. This ensures edge recognition and sets interrupt request bit IEx. The CPU clears IEx automatically during service routine fetch cycles for edge-triggered interrupts.

External interrupt inputs *int0_n* and *int1_n* provide both the capability to exit from idle mode on low-level signal. GPIO description

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TCON

SFR Address: 0x88

BIT	7	6	5	4	3	2	1	0
FIELD	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7	TF1	**See timer/counter chapter**
6	TR1	**See timer/counter chapter**
5	TF0	**See timer/counter chapter**
4	TR0	**See timer/counter chapter**
3	IE1	**External interrupt 1 edge flag. Hardware controlled** Set when external interrupt 1 is detected. Cleared when interrupt is processed.
2	IT1	**External interrupt 1 signal type control bit.** Set to specify External interrupt 1 as falling edge triggered. Cleared to specify External interrupt 1 as low level triggered.
1	IE0	**External interrupt 0 edge flag. Hardware controlled** Set when external interrupt 0 is detected. Cleared when interrupt is processed
0	IT0	**External interrupt 0 signal type control bit.** Set to specify External interrupt 0 as falling edge triggered. Cleared to specify External interrupt 0 as low level triggered.

Table 14 ***Timer/counter control register (TCON low)***

11.1.3 Intnmi interrupt

Intnmi input is the non-maskable interrupt input. Since *intnmi* is high level-triggered input, *Not available for BK2461*

11.1.4 Additional interrupts

This configuration requires the use of three new SFRs: Additional interrupt Flag register (AIF), Additional Interrupt Enable Register (AIE) and Additional Interrupt Priority Register (AIP).

Register	Address	Description	Reset value
AIE	0xE8	Additional interrupt enable	00h
AIF	0xC0	Additional interrupt flag	00h
AIP	0xF8	Additional interrupt priority	00h

Table 15 ***Additional interrupt registers***

The additional external sources are level-activated for *intextra_n[5:0]* and transition-activated for *intextra_n [7:6]*.

The flags that actually generate these interrupts are bits AIFj in Special Function Register AIF. When an external interrupt is generated, **the flag that generated it is NOT cleared by hardware when the service routine is vectored to. This has to be done in the user's software**.

All of the bits that generate interrupt (AIFj) can be set by software, with the same result as though it had been set by hardware. That is, interrupts can be generated in software.
Each of the additional external interrupt sources can be individually enabled or disabled by

setting or clearing bit AIEj in Special Function Register AIE.

The interrupt global disable bit EA in IE register also disables the additional interrupts. Like *int0_n* and *int0_n* inputs, *intextra_n* inputs are synchronized once on clock rising edge before internal use.

AIF

SFR Address :0xC0

BIT	7	6	5	4	3	2	1	0
FIELD	AIF7	AIF6	AIF5	AIF4	AIF3	AIF2	AIF1	AIF0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7:0	AIF7:0	**Additional Interrupt Flags:** Set when respective Additional Interrupt detected. Must be cleared by software

Table 16 ***Additional interrupt flag register (AIF)***

11.1.5 Timer Interrupts

Two timer-interrupt request bits (TF0 and TF1 in TCON register) are set by timer overflow (except Timer 0 in Mode 3). When a timer interrupt is generated, the bit is cleared by a hardware jump to an interrupt service routine. Timer interrupts are enabled by bits ET0, ET1, and ET2 in the IE register.

Timer 2 interrupts are generated by a logical OR of bits TF2 and EXF2 in register T2CON. Neither flag is cleared by a hardware jump to a service routine. In fact, the interrupt service routine must determine if TF2 or EXF2 generated the interrupt, and then clear the bit. Timer 2 interrupt is enabled by ET2 in register IE0.

NOTE: EXF2 is not available for P03(T2EX) is not exist.

11.1.6 Serial Port Interrupt

Serial port interrupts are generated by the logical OR of bits RI and TI in the SCON register. Neither flag is cleared by a hardware jump to the interrupt service routine. The service routine resolves RI or TI interrupt generation and clears the serial port request flag. The serial port interrupt is enabled by bit ES in the IE register.

11.1.7 TRAP interrupt

The function of TRAP instruction is like a software breakpoint, which is useful in software debug. The coding of this instruction is [0xA5]. By execution of the TRAP instruction, the Flip8051 generates an interrupt and executes the interrupt service routine at address 0x0033. It acts like the highest priority non-interruptible interrupt.

11.2 Interrupt enable

Each interrupt source (with the exception of TRAP) may be individually enabled or disabled by the appropriate interrupt enable bit in the IE register (or in the AIE register for additional interrupt sources). Note IE also contains a global disable bit (EA) that applies to all interrupts (except TRAP and intnmi that is not maskable). If EA is set, interrupts are individually enabled or disabled by bits in IE. If EA is clear, all interrupts are disabled.

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IE0

SFR Address: 0xA8

BIT	7	6	5	4	3	2	1	0
FIELD	EA	--	ET2	ES	ET1	EX1	ET0	EX0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7	EA	**Global Interrupt Enable** Clear to globally disable all Interrupt sources. Set to 1 to allow Individual interrupts to be enabled by their enable bits
6	--	Not used
5	ET2	**Timer2 Interrupt Enable** Set to enable Timer2 Interrupt. Cleared to disable Timer2 Interrupt
4	ES	**Serial Port Interrupt Enable** Set to enable Serial Port Interrupt. Cleared to disable Serial Port Interrupt
3	ET1	**Timer1 Interrupt Enable** Set to enable Timer1 Interrupt. Cleared to disable Timer1 Interrupt
2	EX1	**External Interrupt 1 enable** Set to enable External Interrupt 1. Cleared to disable External Interrupt 1.
1	ET0	**Timer0 Interrupt Enable** Set to enable Timer0 Interrupt. Cleared to disable Timer0 Interrupt
0	EX0	**External Interrupt 0 enable** Set to enable External Interrupt 0. Cleared to disable External Interrupt 0.

Table 17 ***Interrupt Enable 0 register (IE0)***

AIE

SFR Address :0xE8

BIT	7	6	5	4	3	2	1	0
FIELD	AIE7	AIE6	AIE5	AIE4	AIE3	AIE2	AIE1	AIE0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7:0	AIE7:0	**Additional interrupt Enable** Set to enable respective Additional Interrupt. Cleared to disable respective Additional interrupt.

Table 18 ***Additional Interrupt Enable register (AIE)***

11.3 Interrupt priority

Each of the hardware interrupt sources may be individually programmed to high or low priority levels (except the NMI input and the TRAP, which have a higher priority level). This is accomplished by clearing/setting the corresponding bit in the Interrupt Priority registers (IP or AIP)

The TRAP instruction is the highest priority level interrupt. A TRAP cannot be interrupted by any other interrupt source including the TRAP. A low-priority interrupt can be itself interrupted by a higher priority level interrupt, but not by another lower or equal priority interrupts. Higher priority level interrupts are serviced before lower priority interrupts.

NOTE: some interrupts are not available for BK2461, please refer to the interrupt source for detail.

Interrupt source	Interrupt flag	Priority level	Vector Addresses	Cleared by hardware (H) or by software (S)

TRAP	-	3 (highest - not interruptible)	0x0033	-
Intnmi	-	2	0x003B	-
int0_n	IE0	0 or 1	0x0003	H if edge
Timer 0	TF0	0 or 1	0x000B	H
int1_n	IE1	0 or 1	0x0013	H if edge
Timer 1	TF1	0 or 1	0x001B	H
UART	RI+TI	0 or 1	0x0023	S
Timer2	TF2+EXF2	0 or 1	0x002B	S
Intextra_n[0]	AIF0	0 or 1	0x0043	S
Intextra_n[1]	AIF1	0 or 1	0x004B	S
Intextra_n[2]	AIF2	0 or 1	0x0053	S
Intextra_n[3]	AIF3	0 or 1	0x005B	S
Intextra_n[4]	AIF4	0 or 1	0x0063	S
Intextra_n[5]	AIF5	0 or 1	0x006B	S
Intextra_n[6]	AIF6	0 or 1	0x0073	S
Intextra_n[7]	AIF7	0 or 1	0x007B	S

Table 19 ***Interrupt priority levels and vector addresses***

If two interrupt requests with the same priority level (0 or 1) are received simultaneously, an internal polling sequence determines which request is serviced, according to the table below:

Interrupt source	Interrupt flag	Servicing priority order
int0_n	IE0	1 (highest)
Timer 0	TF0	2
int1_n	IE1	3
Timer 1	TF1	4
UART	RI+TI	5
Timer2	TF2+EXF2	6
Intextra_n[0]	AIF0	7
Intextra_n[1]	AIF1	8
Intextra_n[2]	AIF2	9
Intextra_n[3]	AIF3	10
Intextra_n[4]	AIF4	11
Intextra_n[5]	AIF5	12
Intextra_n[6]	AIF6	13

Intextra_n[7]	AIF7	14 (lowest)

Table 20 ***Interrupt priority within a same priority level (0 or 1)***

IP

SFR Address :0xB8

BIT	7	6	5	4	3	2	1	0
FIELD	--	--	PT2	PS	PT1	PX1	PT0	PX0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7:6	--	Not used
5	PT2	**Priority of timer 2 Interrupt:** Timer 2 Interrupt priority is determined by default priority order when cleared to 0. Timer 2 Interrupts set to high priority level when set to 1.
4	PS	**Serial Port Interrupt priority level.** UART interrupt priority determined by default priority order when cleared to 0. UART interrupts set to high priority level when set to 1
3	PT1	**Timer1 overflow Interrupt priority level** Timer 1 Interrupt priority determined by default priority order when cleared to 0 Timer 1 Interrupts set to high priority level when set to 1.
2	PX1	**External Interrupt 1 priority level** External Interrupt 1 priority determined by default priority order when cleared to 0. External Interrupt 1 set to high priority level when set to 1.
1	PT0	**Timer0 overflow Interrupt priority level** Timer 0 Interrupt priority determined by default priority order when cleared to 0. Timer 0 interrupt set to high priority level when set to 1.
0	PX0	**External Interrupt priority level** External Interrupt 0 priority determined by default priority order when cleared to 0. External Interrupt 0 set to high priority level when set to 1.

Table 21 ***Interrupt Priority Register (IP)***

AIP

SFR Address: 0xF8

BIT	7	6	5	4	3	2	1	0
FIELD	AIP7	AIP6	AIP5	AIP4	AIP3	AIP2	AIP1	AIP0
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7:0	AIP7:0	**Additional Interrupt priority level** Respective Additional interrupt set to high priority level when set to 1

Table 22 ***Additional Interrupt Priority Register (AIP)***

11.4 Interrupt blocking conditions

If all enable and priority requirements have been met, a single prioritized interrupt request at a time branches to an interrupt service routine. There are 3 causes of blocking conditions with hardware-generated interrupt request:

1. An interrupt of equal or higher priority level is already in progress (defined as any point after the flag has been set and the RETI of the ISR has not executed).
2. The current polling cycle is not the final cycle of the instruction in progress.
3. The instruction in progress is RETI or any write to the IE, IP, AIE or AIP registers.

Any of these conditions blocks calls to interrupt service routines. Condition 2 ensures the

instruction in progress completes before the system vectors to the ISR. Condition 3 ensures at least one more instruction executes before the system vectors to interrupts if the instruction in progress is a RETI or any write to an interrupt control registers.

: *If the interrupt flag for a level-triggered external interrupt is set but denied for one of the above conditions and is clear when the blocking condition is removed, then the denied interrupt is ignored. In other words, blocked interrupt requests are not buffered for retention.*

12 Peripheral module

12.1 OVERVIEW

12.2 UART

12.2.1 Serial port overview

The Flip8051 provides a standard serial communication interface (UART). The Serial Port uses the signals Serial In and Serial Out to receive and transmit serial data. The modes of operation and baud rate generation are the same as the original 80C51. The serial interface in the Flip8051 supports all operation modes, as in standard 80C51.

12.2.2 Operation mode

12.2.2.1 Mode 0 (synchronous mode, half duplex)

Not supported for BK2461

12.2.2.2 Mode 1 (asynchronous mode, full duplex)

In Mode 1, data is transmitted through *serial out* signal and received through *serial in* signal. The data is composed of 10 bits: starting with a start bit “0”, then followed by 8 data bits (LSB first, MSB last), and then the stop bit “1”. The Baud Rate in Mode 1 is controlled by Timer1 or Timer2 and is programmable. Please refer to Programming the Baud Rate, in later part of this chapter for details. To select the mode 1, clear SCON.SM0 and set SCON.SM1.

12.2.2.2.1 Transmission

To send out data, clear the SCON.REN bit and write the data into the SBUF special function register. The data will then be shifted out (LSB first, MSB last), at the *serial out* pin.

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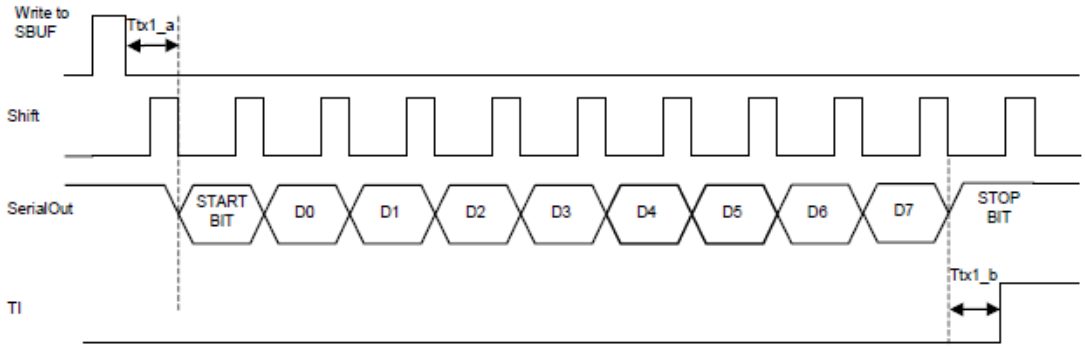


Figure 10 ***Serial Transmit Mode 1***

12.2.2.2.2 Reception

To receive data, set the SCON.REN bit and clear the SCON.RI, this will enable the receive function. When received the data value can be read from the SBUF special function register.

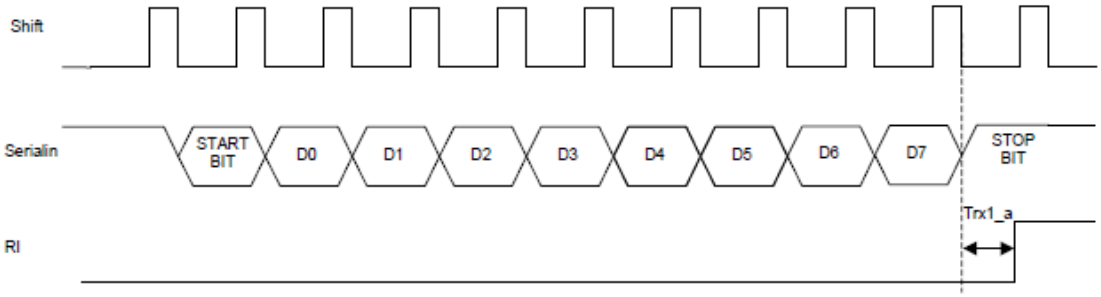


Figure 11 ***Serial receive Mode 1***

12.2.2.3 Mode 2 (asynchronous mode, full duplex)

In Mode 1, data is transmitted through *serial out* signal and received through *serial in* signal. The data is composed of 11 bits: 1 start bit, 8 data bits, 1 TB8 bit (in SCON) and the stop bit. The extra TB8 bit is for use in a multiprocessor communication environment. When multiprocessor communication support is not needed, this bit can also be used as a parity bit. The data transfer rate in Mode 2 is fixed as clock/32 or clock/64. Timer 1 and Timer 2 are independent of the Baud Rate generation and can be used for other purposes. To select the mode 2, set SCON.SM0 and clear SCON.SM1.

12.2.2.3.1 Transmission

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To send out data, clear the SCON.REN bit and write the data into the SBUF special function register. The data will then be shifted out (LSB first, MSB last), at the *serial out* pin.

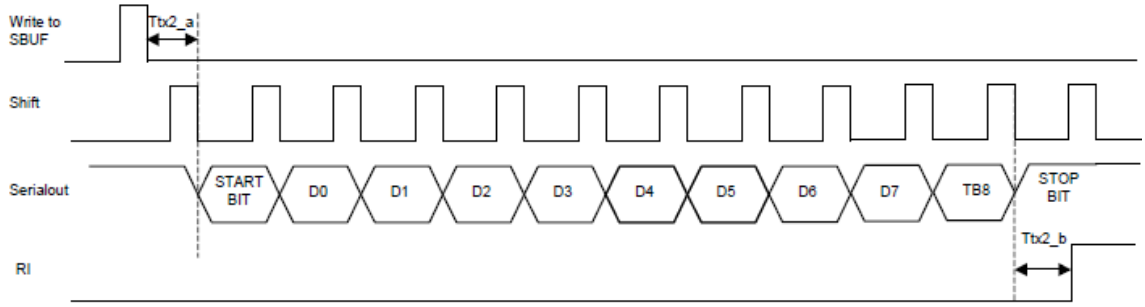


Figure 12 ***Serial Transmit Mode 2***

12.2.2.3.2 Reception

To receive data, set the SCON.REN bit and clear the SCON.RI, this will enable the receive function. When received the data value can be read from the SBUF special function register.

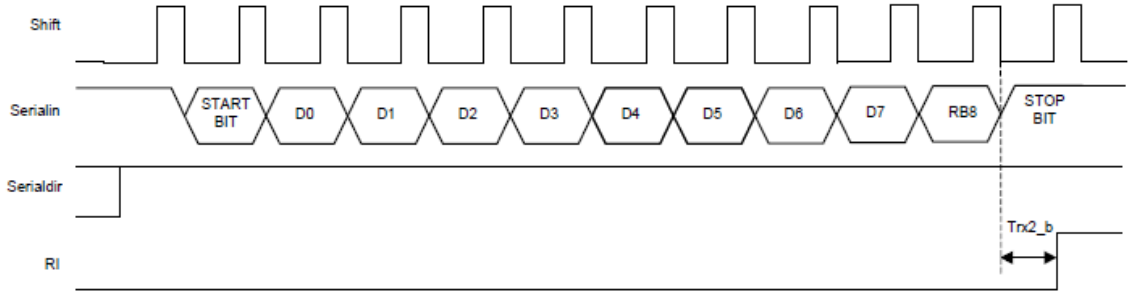


Figure 13 ***Serial receive Mode 2***

12.2.2.4 Mode 3 (asynchronous mode, full duplex)

The operation of Mode 3 is same as Mode 2. The only difference is that Timer1 (or Timer 2) controls the Baud Rate. Serial Mode 3 has the same timing diagram as Mode 2 (above), but the source of the shift pulse is different. To select the mode 1, set SCON.SM0 and SCON.SM1.

12.2.3 Programming the Baud Rate

12.2.3.1 Mode 0

Not available for BK2461.

12.2.3.2 Modes 1 & 3 - Timer1 generating Baud Rate

Timer 1 generates the Receive Clock when T2CON.RCLK=0 and the Transmit Clock when T2CON.TCLK=0, (or always in the Flip8051 without the Timer2). Timer1 should be set up in timer auto-reload mode.
Baud Rate = ((PCON2.SMOD+1)*clock)/(32*12*(256-TH1))
Given a baud rate, the reload value for TH1 is
TH1 = (256 - (PCON2.SMOD+1)*clock)/(384*Baud Rate)
If TH1 is not an integer value then either the Baud Rate or clock frequency must be changed.

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12.2.3.3 Modes 1 & 3 - Timer2 generating Baud Rate

Timer 2 can generate the Receive Clock in the Flip8051, when T2CON.RCLK=1 and the Transmit Clock when T2CON.TCLK=1. If Timer2 is being clocked internally,
Baud Rate = clock /(32*(65536-(RCAP2H,RCAP2L)))
The reload value for RCAP2H, RCAP2L is given by
RCAP2H, RCAP2L = 65536 - clock /(32*Baud Rate)
Otherwise if Timer2 is being clocked by the Timer2 signal, Baud Rate = Timer2 Overflow rate/16.

12.2.3.4 Mode 2

In serial mode 2 the Baud Rate is fixed to (PCON2.SMOD +1)/64.

12.2.4 Serial port registers

The serial port uses two SFR registers.

Register	Address	Description	Reset value
SCON	0x98	Serial Control	00h
SBUF	0x99	Serial Buffer	00h

Table 23 *Serial Port registers*

SCON

SFR Address: 0x98

BIT	7	6	5	4	3	2	1	0
FIELD	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
RESET	0x00							

Bit Number	Bit Mnemonic	Function
7:6	SM0, SM1	**Serial port mode bit** SM0 / SM1 / Mode / Description / Baud rate 0 / 0 / 0 / Shift register / Clk/12 0 / 1 / 1 / 8 bit UART / Variable 1 / 0 / 2 / 9 bit UART / Clk/32 or Clk/64 1 / 1 / 3 / 9 bit UART / Variable
5	SM2	**Serial port mode bit 2** If set in serial modes 2 or 3, RI is only activated if the 9th received data bit (RB8) is 1. If set in serial mode 1, then RI is only activated if a valid stop bit is received.
4	REN	**Receiver Enable Bit** Set for reception, clear for transmission
3	TB8	**Transmit bit 8** In serial modes 2 and 3, the 9th data bit transmitted
2	RB8	**Receiver bit 8** In serial modes 2 and 3, the 9th data bit received.
1	TI	**Transmit interrupt flag** Set at the beginning of the stop bit, or at the end of the 8th bit time in mode 0. Cleared by software.

0	RI	**Receive interrupt flag** Set halfway through the stop bit, or at the end of the 8th bit time in mode 0. Cleared by software.

Table 24 ***Serial Port control register (SCON)***

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12.1 ADC

12.1.1 introduction

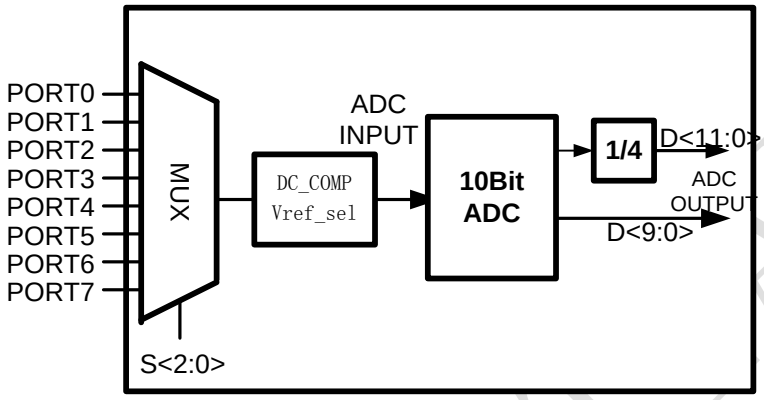


Figure 14 ***ADC***

A 10bits/12bits SAR ADC is integrated in BK2535. Total 8 channels can be selected used for ADC transfer. The ADC supports continue mode and single transfer mode, and the sample rate can be 1kHz to 32kHz. In single transfer mode, it will generate interrupt every time after transform. The input of ADC is share with P3 general I/O port.

In single transfer mode, the time used to convert is very little.

Convert time < 30us(single mode) → Convert Done),

The ADC register located at the XRAM space, the basic address is 0X920.

12.1.2 Register explain

ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x0922	adc_mode		adc_chnn			intr_en	adc_ch_en	ready
adc_mode:=00, power down mode adc_mode:=01, single mode adc_mode:=10, soft mode adc_mode:=10, continue mode; 12bitsmode(filt_mode=1) is only effective for this mode. adc_chnn：eight channel corresponding to GPIO3.0- GPIO3.7 intr_en: generate interrupt or not to MCU adc_ch_en: ADC channel enable. If no GPIO port used to ADC transfer, this bit should be set to 0. ready： when the transfer is done, the bit will be set to zero. After read, it will be set to 1 automatically.								

Table 25 ADC register

ADDR	adc_dataL[7:0]
0x0920	adc_data low 8 bits

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Table 26 ADC register

ADDR	[7]	[6:4]	[3:0]
0x0921	adc_setting	pre_divid[2:0]	adc_dataH
adc_setting: the setting time for ADC after power on，1：40us。 0：20us pre_divid[2:0]: clock divider (the number should be set as 0x01) adc_dataH：the higher 4 bits for adc_dat. high resolution mode:{adc_dataH[3:0],adc_dataL[7:0]}, normal mode: {adc_dataH[1:0],adc_dataL[7:0]}.			

Table 27 ADC的SFR

ADDR	*adc_rate*
0x0923	*adc_rate low 8 bits*

Table 28 ADC register

ADDR	[7]	[6:5]	[4]	[3:0]
0x0924	High_res_mode	adc_dly[1：0]	vdd_chnn	adc_rate[11:8]
High_res_mode: 12 bits mode or 10 bits mode adc_dly: the valid sample for the first conversion. Please set as 2 or 3 for this register. vdd_chnn: 1: set VDD as the input of ADC; 0: GPIO3 will be the input of ADC adc_rate： the high 4 bits for adc_rate				

Table 29 ADC register

12.1.3 Sample rate:

Given a ADC sample rate, you can calculate the adc_rate value as below:
ADC sample = system_clk/((pre_divid+1)*(adc_rate+1))
ADC sample = system_clk/((pre_divid+1)*(adc_rate+1))/4 High_res_mode

adc_rate = system_clk/((pre_divid+1)*(ADC sample))-1
= system_clk/(2*(ADC sample)) -1
Note1: the sample rate should be not greater than 85k for 10bits mode.
Note2: the sample rate will decrease 4 times for high resolution mode.
Note3: the pre_divid should be set as 1.
Note4: In continue mode, the sample rate is fixed in spite of read or not by MCU. In software mode, ADC will enter waiting state until the result is read by MCU

12.1.4 ADC usage

The reference voltage can be set as 1.2V or Vdd/2 for different application. Also, you can decide whether add DC compensation for improving the negative input voltage.

BANK1		
Reg07[26]	Select the reference voltage. 0: 1.2V; 1: VDD/2	
Reg07[25]	Compensate the DC or not. 0: not compensate; 1: yes	

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Table 30 ADC analog register

12.2 PWM

12.2.1 OVERVIEW

The PWM peripheral is an additional peripheral. The PWM is connected to the Flip8051 through the external RAM interface.The Pulse Width Modulation can be used in several kinds of applications. Typically, the PWM can be used to drive DC motors in automotive applications, to generate DTMF in telecom applications or to generate AM radio quality equivalent audio signals.

12.2.2 FUNCTIONAL DESCRIPTION

The PWM generates pulses of programmable length and period. To set up the duty cycle, four registers are needed (depending on the resolution mode): one control register PWMC, one register for the resolution, one register for the duty cycle PWMDCLSB and in the case of high resolution, one other register for the duty cycle PWMDCMSB. The PWM can operate in two modes:

• High-resolution mode (10 bits): registers PWMDCLSB and PWMDCMSB are used.
• Standard-resolution mode (8 bits): the register PWMDCMSB is not used.

When operating in the standard-resolution mode, only the PWMDCLSB is taken into account.

When the resolution for the application is decided, **it's advised not to change it again.**

The PWM address is show as below; the basic address is 0XA00 in external RAM space.

ADDRESS	PWM_CTRL	PWM_DCLSB	PWM_DCMSB	PWM_RESOLUTION
PWM0	0XA00	0XA01	0XA02	0XA03
PWM1	0XA04	0XA05	0XA06	0XA07
PWM2	0XA08	0XA09	0XA0A	0XA0B
PWM3	0XA0C	0XA0D	0XA0E	0XA0F
PWM4	0XA10	0XA11	0XA12	0XA13

Table 31 *PWM register address*

All the five PWM have the same operation. Next, we will describe the detail usage of PWM0.

register[bit]	控制信号名	ADDR	Operation	Function
[7]	pwm0_dcresol	0XA00	R/W	PWM0 Duty Cycle Resolution 1'b0 => standard resolution 1'b1 => high resolution
[6]	en_pwm0	0XA00	R/W	Enable PWM0
[5:0]	pwm0_prescaler	0XA00	R/W	PWM0 prescaler
[7:0]	pwm0_dclsb	0XA01	R/W	PWM0 Duty Cycle LSB

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[7:0]	pwm0_dcmsb	0XA02	R/W	PWM0 Duty Cycle MSB
[7:0]	pwm0_resol	0XA03	R/W	PWM0 resolution

pwm0_dcresol: Duty Cycle Resolution.

This bit is used to select the duty cycle resolution. It is advised to set the resolution only once, at the beginning of the application and not to change it after.

0 = the 8-bit resolution mode is selected (Standard resolution).

1 = the 10-bit resolution mode is selected (High resolution).

ENPWM: Enable Pulse Width Modulation.

This bit controls the pulse width modulation output. While this bit is low, the output is disabled.

0 = The PWM output is disabled.

1 = The PWM output is enabled.

When the bit ENPWM is cleared, the user can change the prescaler, and then the period of the pulse width modulation output is modified. The period can be changed at each cycle of clock.

The way to configure the output period is:

Disable the bit ENPWM

Write the value of the prescaler (bits 5 downto 0 of the register PWMCTRL)

Enable the bit ENPWM (bit 6 of the register PWMCTRL).

PWMPESCALER: Pulse Width Modulation Prescaler.

This field is used to set the repetition rate of the square wave available at output PWM. The frequency of this square wave is given by the following formula:

PWM_resoluation: the 8 bit register decide the stop counter of the PWM. It can be used to adjust the resolution of PWM.

PWMDCLSB and **PWMDCMSB** registers are used to set the duty cycle of the square wave generated. These registers are constantly compared to an internal counter. The size of this counter is function of the resolution (8 or 10 bits). This gives a pulse width modulation in the range of 0/(1~255) to 255/(1~255) for the standard-resolution and 0/(769~1023) to 1023/(769~1023)for the high-resolution.

The PWMDC value indicates the duration of the high level:

If PWMDC=all zeros, PWMOUT stays low.

If PWMDC=all ones, PWMOUT stays high.

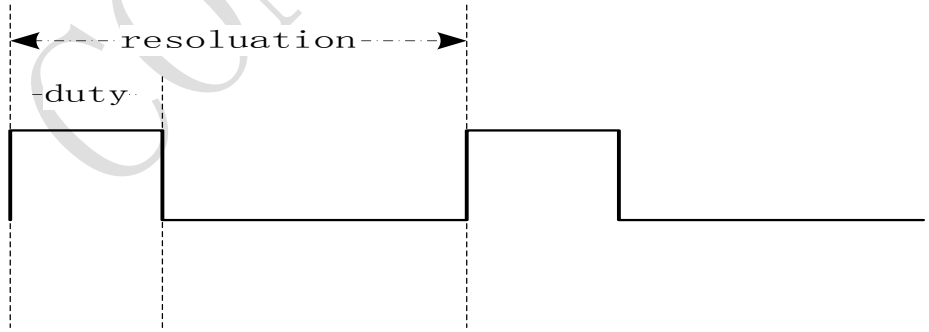


Figure 15 ***PWM parameter***

12.2.3 Frequency of PWM

The frequency of PWM can be calculated by the next formula.

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$$F_{pwm} = \frac{F_{osc}}{2 * (PWMP + 1) * pwm_resol} \ (Standard\ resolution\ mode)$$

$$F_{pwm} = \frac{F_{osc}}{2 * (PWMP + 1) * (pwm_resol + 768)} \ (High\ resolution\ mode)$$

NOTE: the default value of pwm_resol is 255, it cannot be set as zero. The value is preferred be set more than127.

NOTE: **PWMPESCALER cannot be set as zero, or overflow will be happened.**

NOTE: The duty cycle is set dynamically. During a period, it is possible to change the duty cycle.

12.3 I2C master

12.3.1 Overview

The Inter-Integrated Circuit (I2C) master controller is a simple bi-directional 2-wire bus, which provides an interface between BK2461 and an I2C bus.

The I2C mater handles all functions necessary to establish and maintain data link:

- Fast and standard transfer rates.
- 7-bit addressing on I2C.
- Simple master operations.
- Clock Stretching and Wait State generation.
- Operates from a wide range of input frequencies.
- Interrupt generation.
- Fully synthesizable, static synchronous design.

Received and Transmit Data are stored respectively in Receive Buffer and Transmit Buffer. Only one byte at a time can be stored in each buffer. During an I2C transaction, the CPU needs to read regularly the Receive Buffer and to write regularly the Transmit Buffer.

NOTE: Arbitration for multi-master use is not supported by BK2461.

12.3.2 List of I2CM register

Mnemonic	Name	Addre
MCON	I2CM Control register	S:0E1
MRXBUF	I2CM Reception buffer	S:0E2
MTXBUF	I2CM Transmission Buffer	S:0E3
MPRESC	I2CM Pre-scalar clock register	S:0E4
MSTAT0	I2CM Status register 0	S:0E5
MSTAT1	I2CM Status register 1	S:0E6
MIEN0	I2CM Interrupt Enable register 0	S:0E7
MIEN1	I2CM Interrupt Enable register 1	S:0D2
MCADDR	I2CM Call Address register	S:0D4

Table 32 *I2CM register*

MCON (S:E1h) I2CM Control Register

BIT	7	6	5	4	3	2	1	0
FIELD	--	--	WAIT	--	STOP	SRST	STA	BUSY

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RESET	0000 0000b

Bit Number	Bit Mnemonic	Function
7	--	**Reserved** The value read from this bit is indeterminate.
6		**Reserved** The value read from this bit is indeterminate.
5	WAIT	**Wait state mode** '1': Generate wait state on SCL line when RX overflows. '0': Send "Not Acknowledge" to stop the transmission when RX
4	--	**Reserved** The value read from this bit is 0.
3	STOP	**Generate Stop condition** When this bit is set, the current byte ends normally and a STOP condition is generated just after the acknowledge cycle. This bit is automatically cleared by the controller when the STOP
2	SRST	**Software reset** This bit is automatically cleared once IDLE state is reached.
1	STA	**Generate Start condition** This bit is automatically cleared by the controller when the transmission has begun or if an error is detected.
0	BUSY	**BUSY flag** This bit is set to '1' when an I2C frame transfer is in progress on I2C bus.

Table 33 *I2CM Control Register (MCON)*

MRXBUF (S:E2h) Read only I2CM Receive Buffer

Bit Number	Bit Mnemonic	Function
7:0	RXBUF	**Data received by I2CM**

Table 34 *I2CM Receive Register (MRXBUF)*

MTXBUF (S:E3h) Write only I2CM Transmit Buffer

Bit Number	Bit Mnemonic	Function
7:0	TXBUF	**Data transmitted by I2CM**

Table 35 *I2CM Transmit Buffer (MTXBUF)*

MPRESC (S:E4h) I2CM Clock Prescalar Register

MPRESC register enables to generate *OSCL* output from a large range of CLK frequency.

Bit Number	Bit Mnemonic	Function	Default value
7:0	PRESC	**Clock pre scalar register** Fscl = $Fclk/10*(1+PRESC)$	**'h00**

Table 36 *I2CM MPRESC Register*

Note: This register should not be written during a transmission.

MSTAT0 (S:E5h) I2CM Status Register 0

Bit Number	Bit Mnemonic	Function
7	--	**Reserved** The value read from this bit is indeterminate.
6	--	**Reserved** The value read from this bit is indeterminate.

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5	--	**Reserved** The value read from this bit is indeterminate.
4	DNA	**Data byte not acknowledged** Data byte not acknowledged during transmission. Stop condition sent.
3	SANA	**Slave Address Not Acknowledged** Slave Address not acknowledged. Stop condition sent.
2	UNF	**Under Flow** Transmit Data Byte not ready (Transmit Buffer is empty) while a new data byte needs to be sent. A STOP condition is sent.
1	OVF	**Receive Overflow** Received Data Byte could not be written (Receive Buffer is full) while a new byte was received. A Not Acknowledge and a STOP condition are sent.
0	NEND	**Normal End (End of access with no error)** Set when a stop is sent at the end of a successful access. Clear automatically when a new I2C access starts.

Table 37 *I2CM Status Register 0 (MSTAT0)*

These interrupt sources are automatically cleared after a read access to this register.

When DNA, SANA, UNF or OVF flags have been set, reception and transmission processes are disabled until the CPU has read MSTAT0 register. This read operation automatically resets MSTAT0 register and MCON.STA bit, if one of these error bits is set. If this read operation is performed while no error bit is set, MCON.STA bit is not cleared.

These interrupt sources can all be individually enabled/disabled by MIEN0 register.

MSTAT1 (S:E6h) Read only I2CM Status Register 1

Bit Number	Bit Mnemonic	Function
7	--	**Reserved** The value read from this bit is indeterminate.
6	--	**Reserved** The value read from this bit is indeterminate.
5	TBE	**Transmission buffer is empty** **'1'**: Transmit Buffer empty. This flag is cleared when the CPU performs a write access to TXDATA register. **'0'**: At least one Transmit Data Byte is available.
4	--	**Reserved** The value read from this bit is 0.
3	TBF	**Transmission buffer is full** **'1'**: Transmit Buffer full. No more write operation into transmit buffer or memory is performed (CPU write request to TXDATA not taken in account). This flag is cleared when a new Data Byte is requested by the TXRX controller. **'0'**: Transmit Buffer is empty
2	RBE	**Reception buffer is empty** **'1'**: Receive Buffer empty. No more write operation into receive buffer or memory is performed (CPU read request to RXDATA not taken in account). This flag is cleared when a new Data Byte is received by the TXRX controller. **'0'**: At least one received Data Byte is available.
1	--	**Reserved** The value read from this bit is indeterminate.
0	RBF	**Reception buffer is full** **'1'**: Receive Buffer full. This flag is cleared when the CPU performs a read operation to RXDATA register. **'0'**: Receive Buffer is empty

Table 38 *I2CM Status Register 1 (MSTAT1)*

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These interrupt sources can all be individually enabled/disabled by MIEN1 register.

MIEN0 (S:E7h) I2CM Interrupt Enable Register 0

Bit Number	Bit Mnemonic	Function
7	--	**Reserved** The value read from this bit is indeterminate.
6	--	**Reserved** The value read from this bit is indeterminate.
5	--	**Reserved** The value read from this bit is indeterminate.
4	EDNA	**Data byte Not Acknowledged Interrupt enable bit** Clear to disable MSTAT0.DNA bit to generate an interrupt request Set to enable MSTAT0.DNA bit to generate an interrupt request
3	ESANA	**Slave Address Not Acknowledged Interrupt enable bit** Clear to disable MSTAT0.SANA bit to generate an interrupt request Set to enable MSTAT0.SANA bit to generate an interrupt request
2	EUNF	**Underflow Interrupt enable bit** Clear to disable MSTAT0.UNF bit to generate an interrupt request Set to enable MSTAT0.UNF bit to generate an interrupt request
1	EOVF	**Overflow Interrupt enable bit** Clear to disable MSTAT0.OVF bit to generate an interrupt request Set to enable MSTAT0.OVF bit to generate an interrupt request
0	ENEND	**Normal End Interrupt enable bit** Clear to disable MSTAT0.NEND bit to generate an interrupt request Set to enable MSTAT0.NEND bit to generate an interrupt request

Table 39 ***I2CM Interrupt Enable register 0 (MIEN0)***

MIEN1 (S:D2h) I2CM Interrupt Enable Register 1

Bit Number	Bit Mnemonic	Function
7	--	**Reserved** The value read from this bit is indeterminate.
6	--	**Reserved** The value read from this bit is indeterminate.
5	ETBE	**Transmission Buffer Empty Interrupt enable bit** Clear to disable MSTAT1.TBE bit to generate an interrupt request Set to enable MSTAT1.TBE bit to generate an interrupt request
4	--	**Reserved** The value read from this bit is indeterminate.
3	ETBF	**Transmission Buffer Full Interrupt enable bit** Clear to disable MSTAT1.TBF bit to generate an interrupt request Set to enable MSTAT1.TBF bit to generate an interrupt request
2	ERBE	**Reception Buffer Empty Interrupt enable bit** Clear to disable MSTAT1.RBE bit to generate an interrupt request Set to enable MSTAT1.RBE bit to generate an interrupt request
1	--	**Reserved** The value read from this bit is indeterminate.
0	ERBF	**Reception Buffer Full Interrupt enable bit** Clear to disable MSTAT1.RBF bit to generate an interrupt request Set to enable MSTAT1.RBF bit to generate an interrupt request

Table 40 ***I2CM Interrupt Enable register 1 (MIEN1)***

MCADDR (S:D4h)I2CM Call Address Register

Bit Number	Bit Mnemonic	Function

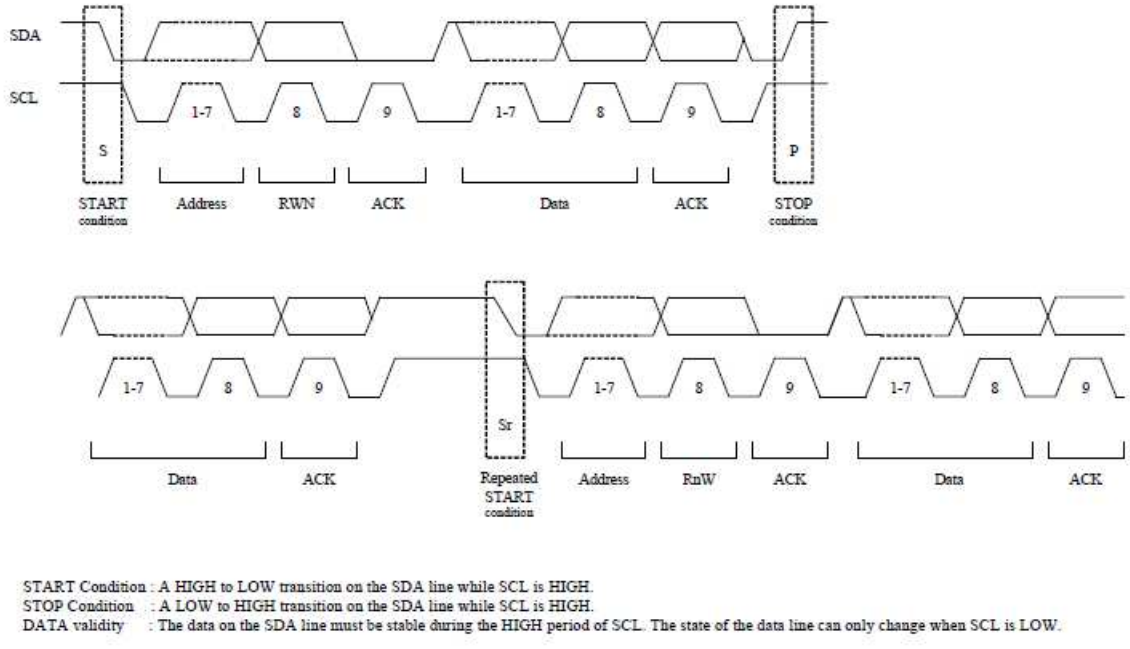
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7	RWN	**Read/write control bit for I2C transaction** Set to read data from addressed slave device Clear to write data to the addressed slave device
6:0	CADDR	**7-bit Call Address** This register must be written before the beginning of an I2C transaction.

Table 41 ***I2CM Call address register (MCADDR)***

12.3.3 I2C frame data format

This I2C master controller only support 7-bit format as shown on the figure below:



START Condition : A HIGH to LOW transition on the SDA line while SCL is HIGH.
STOP Condition : A LOW to HIGH transition on the SDA line while SCL is HIGH.
DATA validity : The data on the SDA line must be stable during the HIGH period of SCL. The state of the data line can only change when SCL is LOW.

Figure 16 ***Complete data transfer***

All words put on the SDA line are 8-bits long

Each byte is followed by an acknowledge bit set by receiver. Data is transferred with the most significant bit (MSB) first.

After the Start condition (S), a slave address is sent. This address is 7 bits long. The eighth bit determines the direction of the message (R/WN): a '0' means that the master will write data to a selected slave, a '1' means that the master will read data from a selected slave.

A data transfer is always terminated by Stop condition (P). However, if the master still wishes to communicate on the bus, it can generate a Repeated Start (Sr) that this to say to generate another START without first generating a STOP. Various combinations of read/write formats are then possible within such a transfer.

Note that two groups of eight addresses (0000XXX and 1111XXX) are reserved for purposed shown in the following table.

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CALL ADDRESS	RWN Bit	Description
0000 000	0	General call address. It is used to address every device connected to I2C-bus.
0000 000	1	START byte(1)
0000 001	X	CBUS address (2).
0000 010	X	Reserved for different bus format.
0000 011	X	Reserved for future purposes.
0000 1XX	X	High Speed master code.
1111 1XX	X	Reserved for future purposes.
1111 0XX	X	10-bit slave addressing. Not yet supported.
(1) : No device enables to acknowledge at the reception of the START byte.		
(2) : The CBUS address has been reserved to enable the intermixing of CBUS compatible and the I2C-bus compatible devices in the same system. I2C-bus compatible devices are not allowed to respond on reception of this address.		

Table 42 ***Reserved addresses for I2Cansactions***

12.3.4 Acknowledge

Data transfer with acknowledge is mandatory. The clock pulse related to acknowledge is generated by the master. The transmitter releases the SDA line (High) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge pulse so that it remains stable Low during the High period of this clock pulse.

When a slave does not acknowledge the slave address or the data, the data line SDA must be left high by the slave. Then the master can generate a Stop condition to abort the transfer.

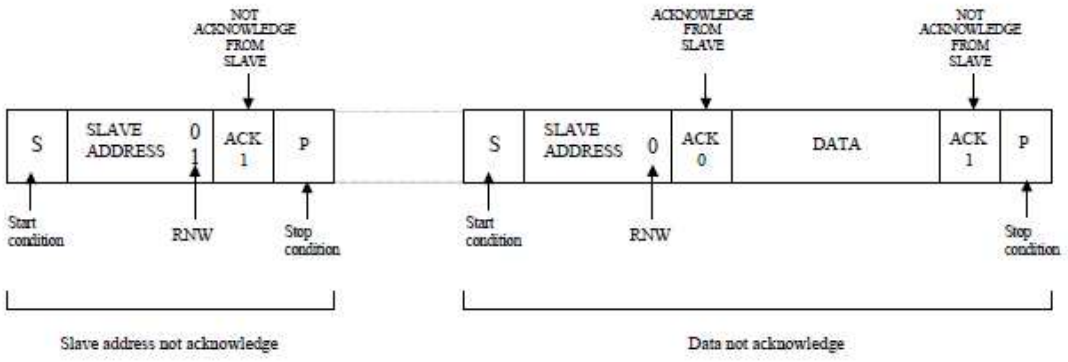


Figure 17 ***"not acknowledge" by slave***

If a master receiver is involved in a transfer it must signal the end of data to the slave transmitter by not generating an acknowledgement after sending a byte. The slave will release SDA line to allow the master to generate Stop or repeated condition.

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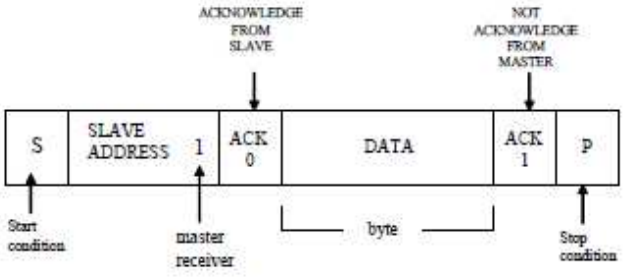


Figure 18 ***"not acknowledge" by master (end of transmission)***

12.3.5 Clock synchronization and wait state

For this device the clock synchronization will be used to enable slaves to hold the SCL line Low after reception and acknowledgement of a byte to force the master into a wait state. This enables to slave devices to get more time to store a received byte or prepare another byte to be transmitted.

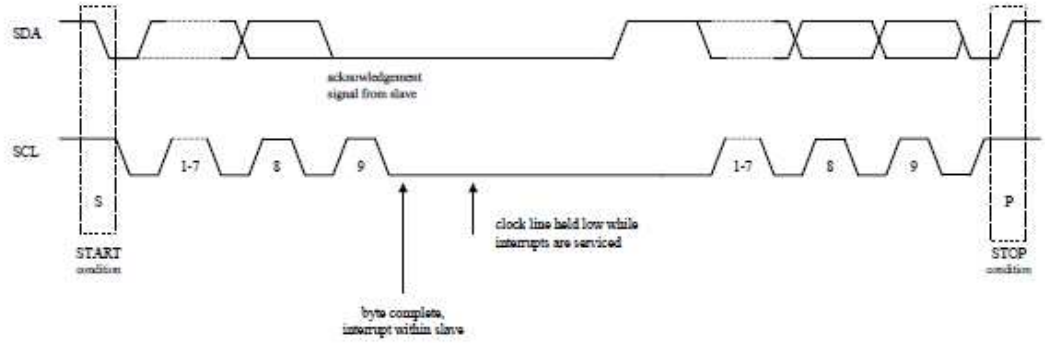


Figure 19 ***Clock synchronization as handshake***

Clock synchronization is performed using the “wired AND” connection of I2C interface to the SCL line. This means that a High to Low transition on the SCL line will cause devices concerned to start counting off their Low period. At the end of their own Low period, devices will set their clocks High. However, SCL line will stay Low as long as one clock is still within its Low period. The SCL line will therefore be held Low by the device with the longest Low period. Devices with shorter Low periods enter a High wait state during this time. When all devices concerned have counted off their Low period, SCL line will be released and go High. There will then be no difference between device clocks and SCL line, and all devices will start counting their High periods. The first device to complete its High period will again pull the SCL line Low. In this way, a synchronized clock is generated.

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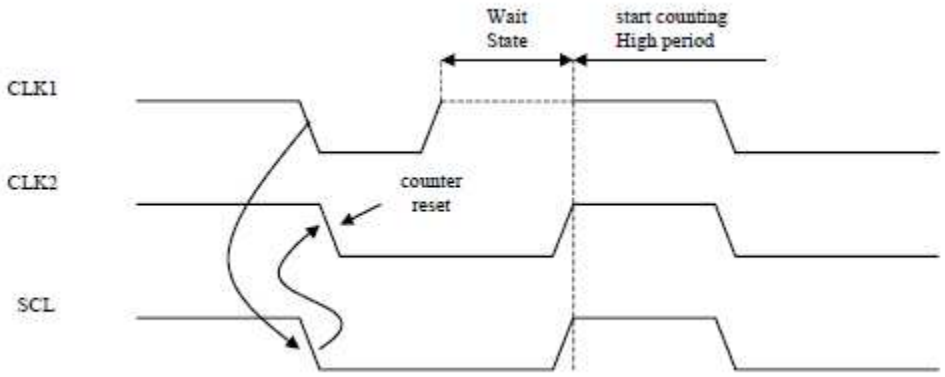


Figure 20 ***Clock synchronization***

12.3.6 Master mode: Transmission

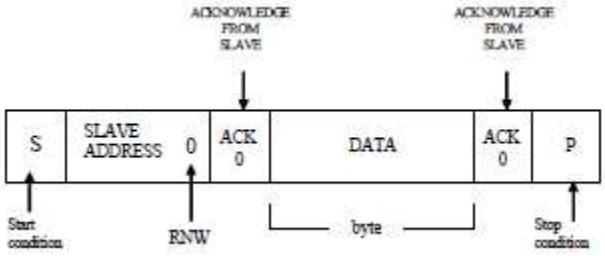


Figure 21 ***Typical transmission***

12.3.6.1 Initialization

Before starting the transmission, the CPU has to write slave address into MCADDR register. Note that for a write request the LSB of the slave address must be set to '0'.
The CPU will have to write a data byte regularly into the Transmit Buffer (MTXBUF register) during the transaction (care must be taken to avoid underflow). TBF (Transmit Buffer Full) or TBE (Transmit Buffer Empty) flags can be used to check the status of the Transmit Buffer.

12.3.6.2 Start

After initialization, CPU can start the transmission by setting the STA bit of the MCON register. Then, the master controller generates the Start condition on the I2C-bus. The STA bit is automatically cleared when the transmission has begun slave address transmission.

After that start has been sent, the slave address is loaded in the shift register to be transmitted on the I2C-bus and the master controller requests the first data byte to the Transmit. Once the slave address had been transmitted, the master controller waits for the slave address Acknowledge from the slave controller.

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12.3.6.3 Data transmission

If the slave controller returns a slave address acknowledge, the master controller loads the data byte in the shift register to be transmitted on the I2C-bus. If this data byte was not the last one, the master sends a request to read the next data byte. Once data byte had been transmitted, the master controller waits for the data acknowledge from slave controller. In case of acknowledge and if data byte sent was not the last one, the controller sends another data byte.

Detection of last data byte:

The data byte is the last data byte if STOP bit is set.

Note: Due to the size of the transmit buffer (1 byte), the first transmitted data byte is also the last data byte.

12.3.6.4 Stop and Repeated Start

Once last data byte had been transmitted, the master controller waits for the data acknowledge from slave controller. In case of acknowledge, if STA is set to '1' by the CPU, the controller will generate a Repeated Start in order to access to an other slave device or change the direction of the transfer (Master Mode Reception) else a Stop condition is sent to finish the communication. The STOP bit is automatically cleared once the Stop condition or repeated Start has been sent.

In case of Repeated Start, the CPU must initialize the next transmission (write of Slave address, length and data bytes) before the end of the current transmission.

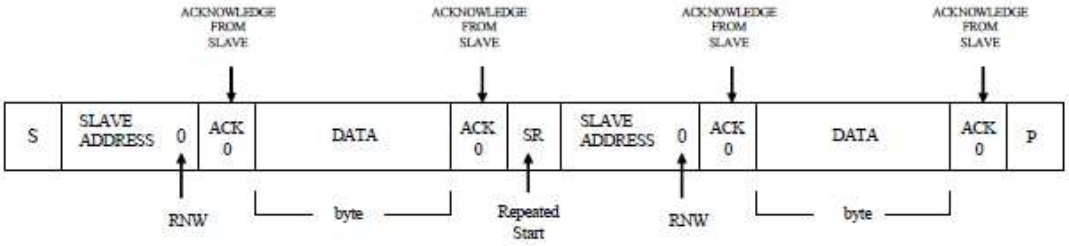


Figure 22 ***Repeated Start or Stop condition after last byte***

12.3.6.5 Transmission error

Not acknowledge from Slave Controller

If the slave address is not acknowledged by the slave controller, the master interrupts the transmission by sending a Stop condition, and sets SANA flag.

If data is not acknowledged by the slave controller, the master interrupts the transmission by sending a Stop condition, and sets DNA flag.

Transmit Underflow

If no data byte is valid from the Transmit Buffer when the controller needs to transmit a data byte, the master interrupts the transmission by sending a Stop condition, and sets UNF flag.

Such underflow occurs when the Transmit Buffer is empty (the CPU did not fill in time the Transmit Buffer).

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End of error

When an error is detected, *OTXRXINT* output is set if the corresponding interrupt source is enabled. The Controller is blocked until MSTAT0 register is read by the CPU. This read operation resets MSTAT0 register and STA bit to disable potential Repeated Start. To pursue the transmission, the CPU must set STA only. To restart the same transmission from the beginning, the CPU must set software reset, refill MTXBUF and then set STA.

12.3.6.6 Transmission FSM

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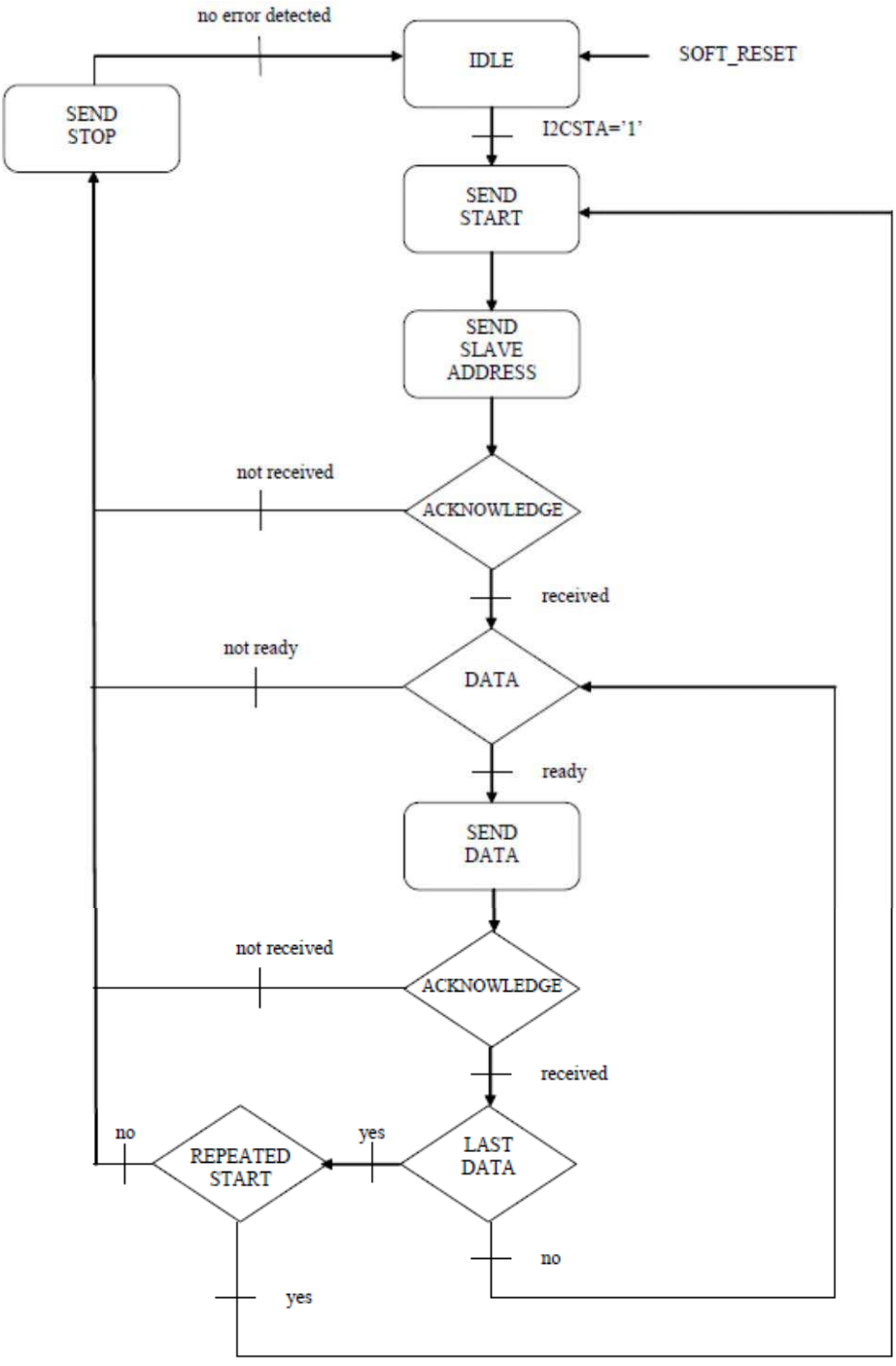


Figure 23 ***Transmission FSM***

Note: If an error occurs during the transmission, FSM will stay into “SEND STOP” state until MSTAT0 register had been read by the CPU. This read operation will clear the STA bit of MCON register and MSTAT0 register. Since MSTAT0 register and MCON register had been reinitialized, the FSM is released into “IDLE” state.

12.3.7 Master mode: Reception

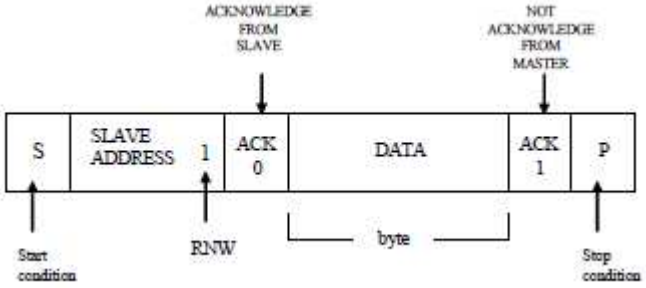


Figure 24 ***Typical reception***

12.3.7.1 Initialization

Before starting the reception, the CPU has to write Slave address into the MCADDR register. Note that for a read request the LSB of the slave address must be set to '1'.
The CPU will have to read the received data bytes in the Receive Buffer (MRXBUF register) regularly during the transaction (care must be taken to avoid overflow).

12.3.7.2 Start

After initialization, the CPU can start the reception by setting the STA bit of the MCON register. Then, the master controller generates the Start condition on the I2C-bus. The STA bit is automatically cleared when the transmission has begun.
Now the slave address is loaded in the shift register to be transmitted on the I2C-bus. Once the slave address had been transmitted, the master controller waits for the slave address acknowledge from the slave controller. If the slave controller returns a slave address acknowledgement, the master controller is waiting for first received data byte.

12.3.7.3 Reception

Once a data byte had been received, it is stored by the master controller in the Receive. More over, if received data byte is not the last one, the master controller sends an acknowledgement on the I2C-bus. Otherwise a "Not Acknowledge" is sent to indicate that it was the last read request and that slave controller must release the I2C bus to allow generating stop condition.
After the data acknowledge transmission, a new data reception can be done and the CPU can read the stored data using MRXBUF register.
Detection of last data byte:
The data byte is the last data byte if STOP bit is set.
Note: Due to the size of the receive buffer (1 byte), the first received data byte is also the last data byte.

12.3.8 Stop and Repeated Start

After the "data not acknowledge" transmission, if STA is set to '1' by the CPU, the controller

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will generate a Repeated Start in order to access to another slave device or change the direction of the transfer (Master mode Transmission) else a Stop condition is sent to finish the communication. The STOP bit is automatically cleared once the Stop condition or repeated Start has been sent.

In case of Repeated Start, the CPU must initialize the next transmission (write of Slave address, length and data bytes) before the end of the current reception.

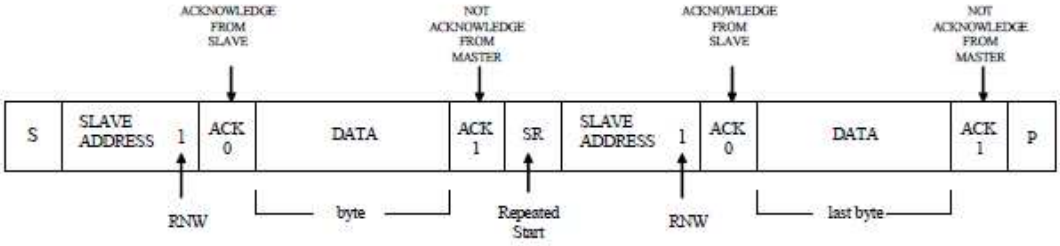


Figure 25 ***Repeated Start or Stop condition after last byte***

12.3.8.1 Reception error

Not acknowledge from Slave Controller

If the slave address is not acknowledged by the slave controller, the master interrupts the transmission by sending a Stop condition, and sets SANA flag.

Receive Overflow

When a data byte is received, the TXRX controller checks that the previous data byte has been handled. If it is not the case (RXBUF overflow), the master interrupts the reception by sending “not acknowledge “ and a Stop condition, and sets OVF flag.

End of error

When an error is detected, OTXRXINT output is set if the corresponding interrupt source is enabled. The controller is blocked until MSTAT0 register is read by the CPU. This read operation resets MSTAT0 register and STA bit to disable a potential Repeated Start. If the CPU wants to discard previous received data byte, it must set software reset. To restart the same transmission, the CPU just has to set STA.

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12.3.9 Reception FSM

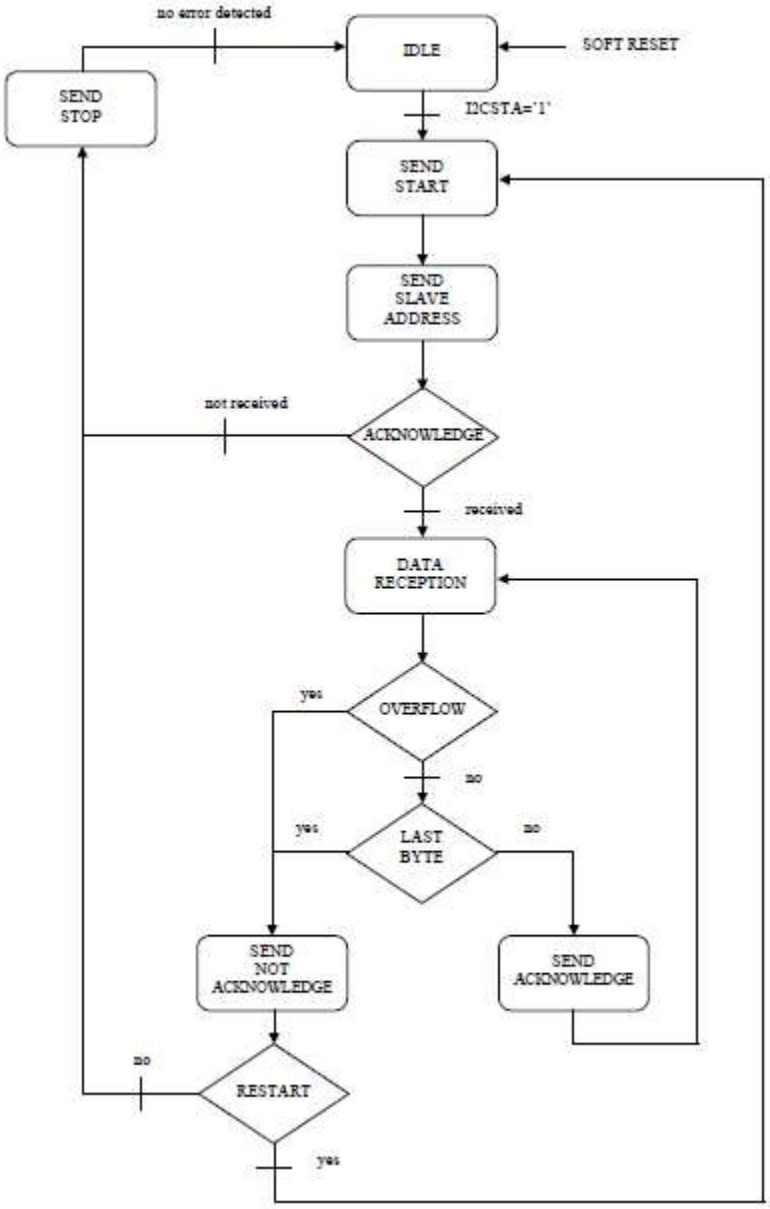


Figure 26 ***Reception FSM***

Note: If an error occurs during the reception, FSM will stay into “SEND STOP” state until MSTAT0 register had been read by the CPU. This read operation will clear the STA bit of MCON register and MSTAT0 register. Since MSTAT0 register and MCON register had been reinitialized, the FSM is released into “IDLE” state.

12.3.10 Data Handling

The Data Bytes exchanged on the I2C line are available in MRXBUF (received data) and

MTXBUF (transmitted data) registers.

It is up to the user of the FlipI2CM to read/write data byte exchanged on the I2C line when they are available. This can be handled by software routine thanks to the status flags.

12.3.11 Software Reset

The software reset is activated by CPU setting bit SRST of control register (MCON). The software reset is used to stop current access on I2C bus.

Software reset initializes MCON, MSTAT0 registers and also TXRX controller.

If a software reset occurs during an I2C access, the master controller finishes the transmit or reception of current data byte, it send a Stop condition (in case of reception, send a ”not acknowledge" first) and next, MCON and MSTAT0 registers and TXRX controller are cleared.

At the end of software reset process, the master controller is ready to restart a new or the same access. For same access, the CPU must refill TXBUF (for transmission only) and set STA (MCADDR register is not affected by software reset).

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12.4 Ext_timer

A simple timer is integrated in BK2535 for fixed time interrupt for some special application, such as mouse. (8ms wake up)

This timer selects 32k clock always for avoiding the effect brought by clock switch. The period can be set precisely through the register descript below:

ADDR	[7:3]	[2]	[1:0] **timer_div**	
0X918	reserved	RTC enable	RTC clock divider	
	[7:0] **timer_count**			
0X919	RTC counter high byte			Counter[15:0]= [0X919,0X91A]
0X91A	RTC counter low byte			

Table 43 RTC Register

RTC period = **1/32e3 *（2+ timer_div） * (1+timer_count)**

For example, if you want to get 8ms period wakeup, you can set timer_div=2 and timer_count=63.

Note: to enable the RTC interrupt, you should set EA= 1 and EX6 = 1.

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12.5 WDT

There is a watch dog timer in BK2535. When overflow happened, the WDT will trigger the CPU into reset status and rerun from the beginning location. The software need feed the dog timely to avoid the overflow happen.

Note: the reset does not affect the RF part.

There are two methods to enable the WDT.

One is writing 0Xa5 on SFR address 0XA6(WDCON) and this operation will clear the WDT counter also (feed dog). Once the WDT enabled by this method, you can disable the WDT through writing 0XDE and 0XAD consecutively during eight clock periods. When the WDT enabled by this method, you can also set whether running in IDLE state. To do this, you can enable it by writing 0XD1 on SFR address 0XA6 or disable it by writing 0XDE and 0XDA consecutively during eight clock periods.

The other method is writing 0XFF on SFR address 0XA6. You cannot close it once you enable the WDT with this method except any reset happened. In this status, the WDT will run always even in IDLE state.

WDCON	7	6	5	4	3	2	1	0
0XA6	/	/	/	state	/	ps2	ps1	ps0

Table 44 Watch Dog Register

State: read only 1: the WDT in active status 0: the WDT in inactive status
Ps2, ps1, ps0: the prescale of watch dog clock.
Note: when write the prescale value, the bit7 must be set as 0.

PS2	PS1	PS0	PRE_scale
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

Table 45 the Prescale of Watch Dog clock

The overflow time of watch dog：

$$WatchdogOverflowTime = \frac{PRE_scale \times 32768}{\text{system clock}}$$

When overflow occur, the whole system will be reset.

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13 BK2461 RF transceiver

13.1 General Description

A RF transceiver (BK-RF) is embedded in BK2461, and the BK-RF is a high performance IP of Beken corporation.
BK-RF is a GFSK transceiver operating in the world wide ISM frequency band at 2400-2483.5 MHz Burst mode transmission and up to 2Mbps air data rate make them suitable for applications requiring ultra low power consumption. The embedded packet processing engines enable their full operation with a very simple MCU as a radio system. Auto re-transmission and auto acknowledge give reliable link without any MCU interference.

The BK-RF operates in TDD mode, either as a transmitter or as a receiver.

The RF channel frequency determines the center of the channel used by BK-RF. The frequency is set by the RF_CH register in register bank 0 according to the following formula: F0= 2400 + RF_CH (MHz). The resolution of the RF channel frequency is 1MHz.

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

The output power of BK-RF is set by the RF_PWR bits in the RF_SETUP register.

Demodulation is done with embedded data slicer and bit recovery logic. The air data rate can be programmed to 1Mbps or 2Mbps by RF_DR register. A transmitter and a receiver must be programmed with the same setting.

In the following chapters, all registers are in register bank 0 except with explicit claim.

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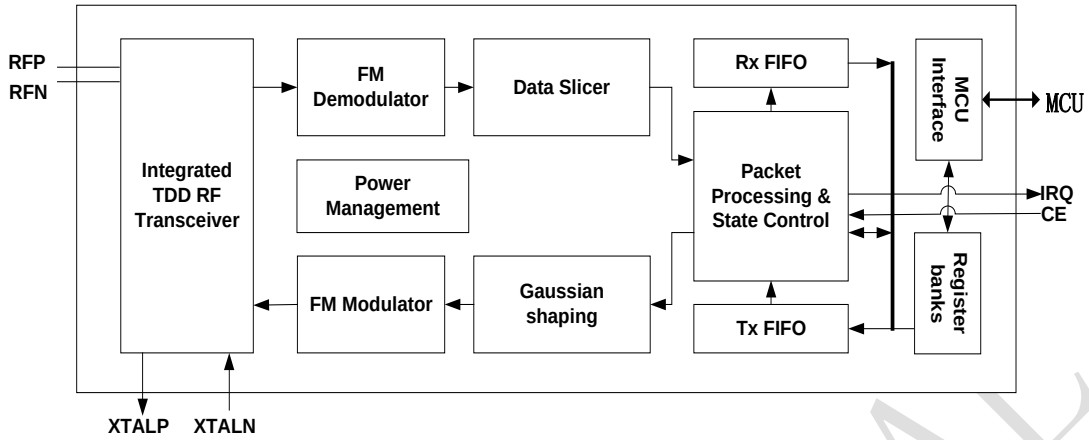


Figure 27 BK2461 RF Block Diagram

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13.2 Abbreviations

ACK	Acknowledgement
ARC	Auto Retransmission Count
ARD	Auto Retransmission Delay
CD	Carrier Detection
CE	Chip Enable
CRC	Cyclic Redundancy Check
CSN	Chip Select Not
DPL	Dynamic Payload Length
FIFO	First-In-First-Out
GFSK	Gaussian Frequency Shift Keying
GHz	Gigahertz
LNA	Low Noise Amplifier
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LSB	Least Significant Bit
MAX_RT	Maximum Retransmit
Mbps	Megabit per second
MCU	Microcontroller Unit
MHz	Megahertz
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
PA	Power Amplifier
PID	Packet Identity Bits
PLD	Payload
PRX	Primary RX
PTX	Primary TX
PWD_DWN	Power Down
PWD_UP	Power Up
RF_CH	Radio Frequency Channel
RSSI	Received Signal Strength Indicator
RX	Receive
RX_DR	Receive Data Ready
SCK	SPI Clock
SPI	Serial Peripheral Interface
TDD	Time Division Duplex
TX	Transmit
TX_DS	Transmit Data Sent
XTAL	Crystal

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13.3 State Control

13.3.1 State Control Diagram

- Internal signal: POR,VDD
- SPI register: CE, PWR_UP, PRIM_RX, EN_AA, NO_ACK, ARC, ARD
- System information: Time out, ACK received, ARD elapsed, ARC_CNT, TX FIFO empty, ACK packet transmitted, Packet received

BK-RF has built-in state machines that control the state transition between different modes.

When auto acknowledge feature is disabled, state transition will be fully controlled by MCU.

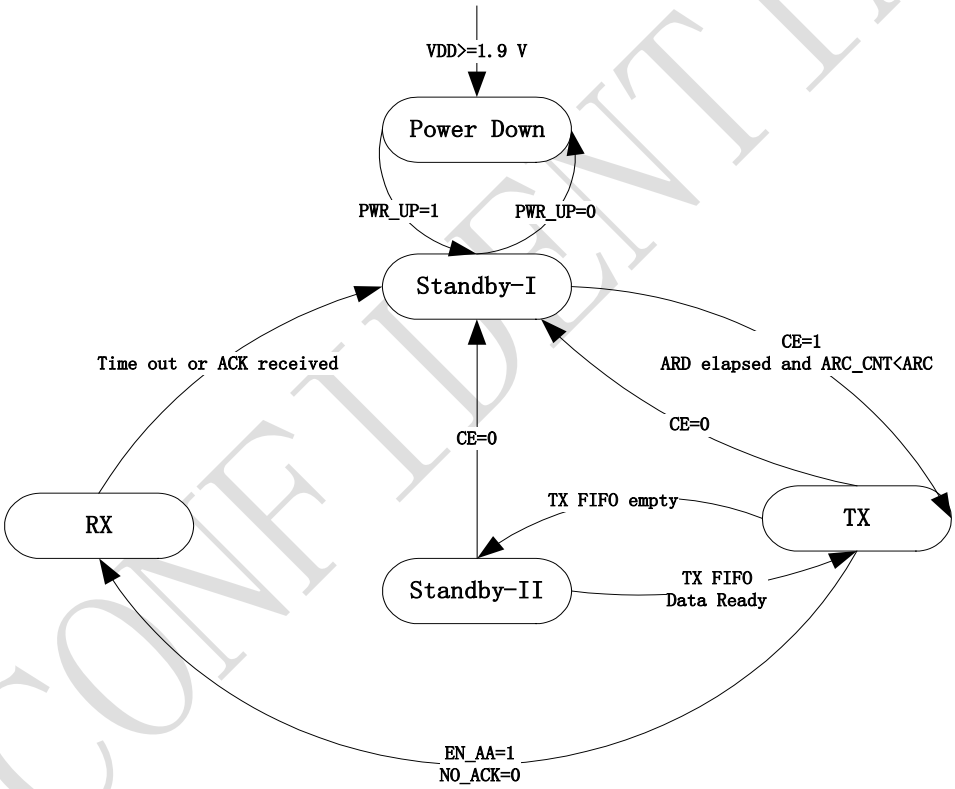


Figure 28 PTX (PRIM_RX=0) state control diagram

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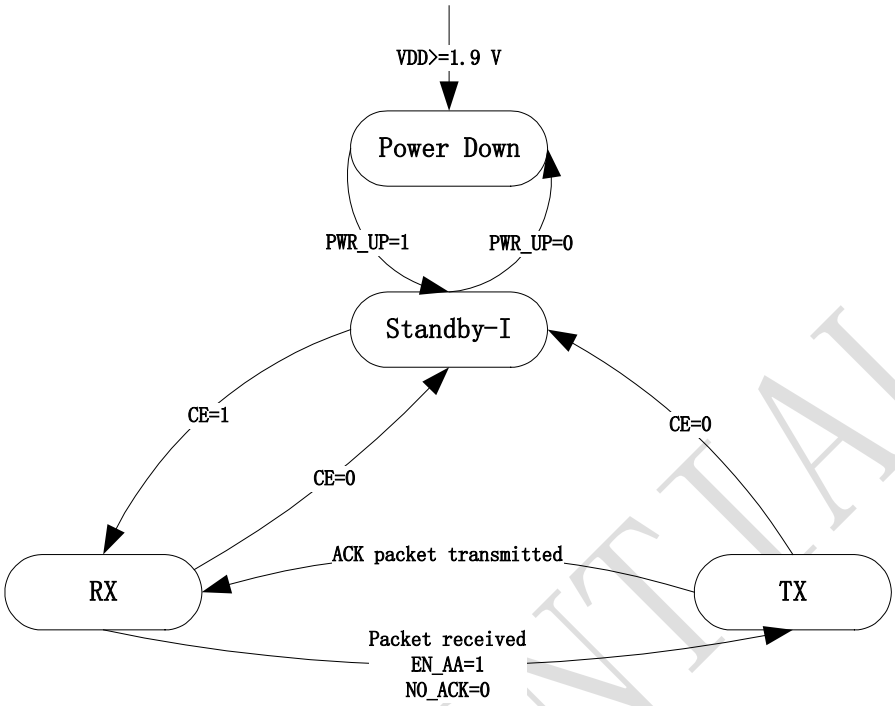


Figure 29 PRX (PRIM_RX=1) state control diagram

13.3.2 Power Down Mode

In power down mode the BK-RF is in sleep mode with minimal current consumption. SPI interface is still active in this mode, and all register values are available by SPI. Power down mode is entered by setting the PWR_UP bit in the CONFIG register to low.

13.3.3 Standby-I Mode

By setting the PWR_UP bit in the CONFIG register to 1 and de-asserting CE to 0, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start-up time. In this mode, part of the crystal oscillator is active. This is also the mode which the BK-RF returns to from TX or RX mode when CE is set low.

13.3.4 Standby-II Mode

In standby-II mode more clock buffers are active than in standby-I mode and much more current is used. Standby-II occurs when CE is held high on a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO in this mode, the device will automatically enter TX mode and the packet is transmitted.

13.3.5 TX Mode

- PTX device (PRIM_RX=0)

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The TX mode is an active mode where the PTX device transmits a packet. To enter this mode from power down mode, the PTX device must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO, and a high pulse on the CE for more than 10μs.
The PTX device stays in TX mode until it finishes transmitting the current packet. If CE = 0 it returns to standby-I mode. If CE = 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the PTX device remains in TX mode, transmitting the next packet. If the TX FIFO is empty the PTX device goes into standby-II mode.

If the auto retransmit is enabled (EN_AA=1) and auto acknowledge is required (NO_ACK=0), the PTX device will enter TX mode from standby-I mode when ARD elapsed and number of retried is less than ARC.

- PRX device (PRIM_RX=1)

The PRX device will enter TX mode from RX mode only when EN_AA=1 and NO_ACK=0 in received packet to transmit acknowledge packet with pending payload in TX FIFO.

13.3.6 RX Mode

- PRX device (PRIM_RX=1)

The RX mode is an active mode where the BK-RF radio is configured to be a receiver. To enter this mode from standby-I mode, the PRX device must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high. Or PRX device can enter this mode from TX mode after transmitting an acknowledge packet when EN_AA=1 and NO_ACK=0 in received packet.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the packet processing engine. The packet processing engine continuously searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The PRX device remains in RX mode until the MCU configures it to standby-I mode or power down mode.

In RX mode a carrier detection (CD) signal is available. The CD is set to high when a RF signal is detected inside the receiving frequency channel. The internal CD signal is filtered before presented to CD register. The RF signal must be present for at least 128 μs before the CD is set high.

- PTX device (PRIM_RX=0)

The PTX device will enter RX mode from TX mode only when EN_AA=1 and NO_ACK=0 to receive acknowledge packet.

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13.4 Packet Processing

13.4.1 Packet Format

The packet format has a preamble, address, packet control, payload and CRC field.

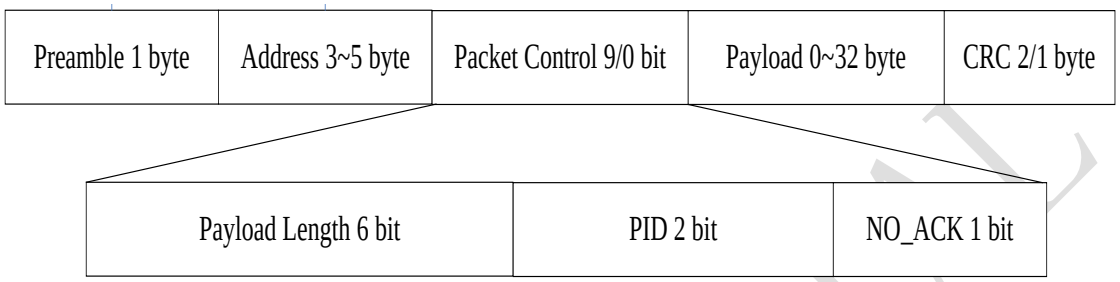


Figure 30 Packet Format

➢ Preamble

The preamble is a bit sequence used to detect 0 and 1 levels in the receiver. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

➢ Address

This is the address for the receiver. An address ensures that the packet is detected by the target receiver. The address field can be configured to be 3, 4, or 5 bytes long by the AW register.

The PRX device can open up to six data pipes to support up to six PTX devices with unique addresses. All six PTX device addresses are searched simultaneously. In PRX side, the data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the RX_ADDR_PX registers.

Each pipe can have up to 5 bytes configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSB byte must be unique for all 6 pipes.

To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet.

On the PRX the RX_ADDR_Pn, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 on the PTX, and as the pipe address for the designated pipe on the PRX.

No other data pipe can receive data until

CONFIDENTIAL

a complete packet is received by a data pipe that has detected its address. When multiple PTX devices are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

➢ Packet Control

When Dynamic Payload Length function is enabled, the packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and, a 1 bit NO_ACK flag.

➢ Payload length

The payload length field is only used if the Dynamic Payload Length function is enabled.

➢ PID

The 2 bit PID field is used to detect whether the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields are used by the PRX device to determine whether a packet is old or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, BK-RF compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

➢ NO_ACK

The NO_ACK flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

The PTX can set the NO_ACK flag bit in the Packet Control Field with the command: W_TX_PAYLOAD_NOACK.However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet and the PRX does not transmit an ACK packet when it receives the packet.

➢ Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide, and it is transmitted on-air as it is uploaded (unmodified) to the device.

The BK-RF provides two alternatives for handling payload lengths, static and dynamic payload length. The static payload length of each of six data pipes can be individually set.

The default alternative is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side. Each pipe has its own payload length.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets

CONFIDENTIAL

with variable payload length to the receiver. This means for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With DPL feature the BK-RF can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the command: R_RX_PL_WID.

In order to enable DPL the EN_DPL bit in the FEATURE register must be set. In RX mode the DYNPD register has to be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

- CRC

The CRC is the error detection mechanism in the packet. The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. It may be either 1 or 2 bytes and is calculated over the address, Packet Control Field, and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value is 0xFF.
The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value is 0xFFFF.

No packet is accepted by receiver side if the CRC fails.

13.4.2 Packet Handling

BK-RF uses burst mode for payload transmission and receive.

The transmitter fetches payload from TX FIFO, automatically assembles it into packet and transmits the packet in a very short burst period with 1Mbps or 2Mbps air data rate.

After transmission, if the PTX packet has the NO_ACK flag set, BK-RF sets TX_DS and gives an active low interrupt IRQ to MCU. If the PTX is ACK packet, the PTX needs receive ACK from the PRX and then asserts the TX_DS IRQ.

The receiver automatically validates and disassembles received packet, if there is a valid packet within the new payload, it will write the payload into RX FIFO, set RX_DR and give an active low interrupt IRQ to MCU.

When auto acknowledge is enabled (EN_AA=1), the PTX device will automatically wait for acknowledge packet after transmission, and re-transmit original packet with the delay of ARD until an acknowledge packet is received or the number of re-transmission exceeds a threshold ARC. If the later one happens, BK-RF will set MAX_RT and give an active low interrupt IRQ to MCU. Two packet loss counters (ARC_CNT and PLOS_CNT) are incremented each time a packet is lost. The ARC_CNT counts the number of retransmissions for the current transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. ARC_CNT is reset by initiating a new transaction. PLOS_CNT is reset by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of

CONFIDENTIAL

the channel quality.

The PTX device will retransmit if its RX FIFO is full but received ACK frame has payload.

As an alternative for PTX device to auto retransmit it is possible to manually set the BK-RF to retransmit a packet a number of times. This is done by the REUSE_TX_PL command.

When auto acknowledge is enabled, the PRX device will automatically check the NO_ACK field in received packet, and if NO_ACK=0, it will automatically send an acknowledge packet to PTX device. If EN_ACK_PAY is set, and the acknowledge packet can also include pending payload in TX FIFO.

13.5 Data and Control Interface

13.5.1 TX/RX FIFO

The data FIFOs are used to store payload that is to be transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFO is accessible in both PTX mode and PRX mode.

There are three levels 32 bytes FIFO for both TX and RX, supporting both acknowledge mode or no acknowledge mode with up to six pipes.

- TX three levels, 32 byte FIFO
- RX three levels, 32 byte FIFO

Both FIFOs have a controller and are accessible by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH_TX command.

The RX FIFO in PRX may contain payload from up to three different PTX devices.
.
A TX FIFO in PTX can have up to three payloads stored.

The TX FIFO can be written to by three commands, W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands give access to the TX_PLD register.

The RX FIFO can be read by the command R_RX_PAYLOAD in both PTX and PRX mode. This command gives access to the RX_PLD register.

The payload in TX FIFO in a PTX is NOT removed if the MAX_RT IRQ is asserted.

In the FIFO_STATUS register it is possible to read if the TX and RX FIFO are full or empty. The TX_REUSE bit is also available in the FIFO_STATUS register. TX_REUSE is set by the command REUSE_TX_PL, and is reset by the command: W_TX_PAYLOAD or FLUSH TX.

CONFIDENTIAL

13.5.2 Interrupt

In BK2461-RF there is an active low interrupt (IRQ), which is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

The 3 bit pipe information in the STATUS register is updated during the IRQ high to low transition. If the STATUS register is read during an IRQ high to low transition, the pipe information is unreliable.

CONFIDENTIAL

13.6 RF Command

The RF commands are shown in the table:

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	Read directly		
W_REGISTER	Write directly		
W_ANALOG_REG	Write through register0X8B8-0X8BC		
R_RX_PAYLOAD	8'b01000000	1 to 32 LSB byte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	8'b01100000	1 to 32 LSB byte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload. This command used for ENABLE_ACK payload
FLUSH_TX	8'b10100000	0	Flush TX FIFO, used in TX mode
FLUSH_RX	8'b10000000	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	8'b00010000	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission

CONFIDENTIAL

R_RX_PL_WID	Read register 0x8C4 directly		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD	8'b01101ppp	1 to 32 LSB byte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACK	8'b01101000	1 to 32 LSB byte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	8'b00000000	0	No Operation.

Table 46 RF command

CONFIDENTIAL

13.7 Register Map

There are two register groups in BK2461 that is digital register and analog register.

13.7.1 Digital Register

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0x0880	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the IRQ pin 0: Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' - 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control, 1: PRX, 0: PTX
0x0881	EN_AA				Enable 'Auto Acknowledgment' Function (only used by RX part) Need match with TX part
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0

CONFIDENTIAL

0x0882	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
0x0883	SETUP_AW				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' - 5 bytes LSB bytes are used if address width is below 5 bytes
0x0884	SETUP_RETR				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Retransmission Delay ‘0000’ – Wait 250 us ‘0001’ – Wait 500 us ‘0010’ – Wait 750 us …….. ‘1111’ – Wait 4000 us (Delay defined from end of transmission to start of next transmission)
	ARC	3:0	0011	R/W	Auto Retransmission Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmission on fail of AA …… ‘1111’ – Up to 15 Re-Transmission on fail of AA
0x0885	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel
0 x0886	RF_SETUP				RF Setup Register
	Reserved	7	0	R/W	Reserved
		6	0	R/W	Reserved
	En_250k_rate	5	0	R/W	Set RF datarate to 250k
		4	0		Reserved,pls don’t change it
	RF_DR	3	1	R/W	Air Data Rate ,decide by 0x886 bit {[5],[3]} ‘00’ – 1Mbps ‘01’ – 2Mbps ‘10’ – 250kbps ‘11’ – reserved
	RF_PWR[1:0]	2:1	11	R/W	Set RF output power in TX mode RF_PWR[1:0] '00' – -10 dBm '01' – -5 dBm

CONFIDENTIAL

					'10' – 0 dBm '11' – 5 dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain 0:Low gain(20dB down) 1:High gain
0 x0887 0 x0888 0 x0889 0 x088A 0 x088B	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. Write the number of bytes defined by SETUP_AW) {X88B,X88A,X889,X888,X887}
0 x088C 0 x088D 0 x088E 0 x088F 0 x0890	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. Write the number of bytes defined by SETUP_AW)
0 x0891	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0 x0892	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0 x0893	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0 x0894	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSB bytes is equal to RX_ADDR_P1[39:8]
0 x0895 0 x0896 0 x0897 0 x0898 0 x0899	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSB byte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device
0 x089A	RX_PW_P0				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	000000	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
0 x089B	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	000000	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
0 x089C	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	000000	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes

CONFIDENTIAL

0 x089D	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	000000	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
0 x089E	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	000000	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
0 x089F	RX_PW_P5				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	000000	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0: not used 1 = 1 byte … 32 = 32 bytes
0 x08A0	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only ‘00’ allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
0 x08A1	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only ‘00000’ allowed
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK

CONFIDENTIAL

					command
0 x08A5 0 x08A4 0 x08A3 0 x08A2	(cfg0c0--3)	31:0	0		Please initialize with 0x00731200
0 x08A9 0 x08A8 0 x08A7 0 x08A6	NEW_FEATURE (cfg0d0--3)	31:0	0		Please initialize with 0x0080B436
0 x08B4 0 x08B3 0 x08B2 0 x08B1 0 x08B0 0 x08AF 0 x08AE 0 x08AD 0 x08AC 0 x08AB 0 x08AA	RAMP (2402table_0 --2401table_A)	87:0	NA	W	Ramp curve Please write with 0xFFFFFEF7CF208104082041
0 x08B5	BK-RF_ce				
		7:1			reserved
		0			ce
0 x08B6	BK-RF_cmd				8'b10000000 : Flush RX 8'b10100000 : Flush TX 8'b00010000 : Reusle TX PL 8'b01000000 : Read RX Payload 8'b01100000 : Write TX Payload 8'b01101ppp : W_ACK_PAYLOAD 8'b01101000 : W_TX_PAYLAOD_NOACK 8'b00000000 : NOP
0 x08B7	BK-RF_FIFO			R/W	TX MODE: TX data payload register 1 - 32 bytes. RX MODE: RX data payload register 1 - 32 bytes.
0 x08B8	BK-RF_sdata_0				Analog register0[7:0]
0 x08B9	BK-RF_sdata_1				Analog register1[15:8]
0 x08BA	BK-RF_sdata_2				Analog register2[23:16]
0 x08BB	BK-RF_sdata_3				Analog register3[31:24]
0 x08BC	BK-RF_sctrl				Write address of Analog rgister (only can be writen)
0 x08C0	BK-RF_status				Status, read only
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt Asserted when new data arrives RX FIFO Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.

CONFIDENTIAL

	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full 0: Available locations in TX FIFO
0 x08C1	BK-RF_observetx				Status, read only
	PLOS_CNT	7:4	0000	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
	ARC_CNT	3:0	0000	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts.
0 x08C2	BK-RF_cdstatus				Status, read only
	Reserved	7:1	000000	R	
	CD	0	0	R	Carrier Detect
0 x08C3	BK-RF_fifostatus				Status, read only
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Reuse last transmitted data packet if set high. The packet is repeatedly retransmitted as long as CE is high. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI command W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag 1: TX FIFO full; 0: Available locations in TX FIFO
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty 0: Data in TX FIFO
	Reserved	3:2	00	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag 1: RX FIFO full 0: Available locations in RX FIFO
	RX_EMPTY	0	1	R	RX FIFO empty flag 1: RX FIFO empty 0: Data in RX FIFO
0 x08 C4	BK-RF_rpl_width				Status, read only
					The width of the payload
0X8C5	BK-RF_mbist_st				Status, read only
	reseved			R	5'b0
	Done	2		R	test_done
	Pass	1		R	test_pass
	Fail	0		R	test_fail
0X8C6~0X8C7	Chip_id			R	
				R	Chip_id[7:0]

CONFIDENTIAL

				R	Chip_id [15:8]
0X8C8~0X8CB	BK-RF_bit_cnt			R	Status, read only Total number of bits received register
0X8CC~0X8CF	BK-RF_err_cnt			R	Status, read only Error counter register
0X8D0~0X8D3	Tx_freq_offset			RW	RF MOD/DEMOD config
0X8D4~0X8D7	Rx_freq_offset			RW	RF MOD/DEMOD config
0X8D8[7:4]	Mod_sdm_dly			RW	RF MOD/DEMOD config
0X8D8[3:0]	Mod_dac_dly			RW	RF MOD/DEMOD config
0xd9[7]	clksel_cfg			R/W	pll sdm output latch edge 1: posedge 0:negedge
0xd9[6]	sdm3bit_cfg			R/W	sdm 2nd/3nd selection 1:3nd 0:2nd
0xd9[5]	pn25ena_cfg			R/W	PN25 enable
0xd9[4]	open_loop_en			R/W	1: FracN = 0
0xd9[3]	rx_if_select			R/W	lo direction select 0:+500k 1: -500k
0xd9[2]	tbfalcon_reset			R/W	sdm reset 1: reset
0xd9[1]	bp_kmod			R/W	bypass kmod calibration
0xd9[0]	vco_cal_en			R/W	vco calibriation enable
0xda[0] 0xdb[7:0]	fm_gain			R/W	vco after calibriation value is set in this register
0xda[1]	rx_if_select			R/W	tx mod direction select 0:+500k 1: -500k
0xda[2]	rf_test_en			R/W	rf test enable if it is 1, then gpio3 and gpio4 output testsignal
0xdc[0] 0xdd[7:0]	fm_kmod_set			R/W	if bp_kmod is 1 auto channel compensation is stopped, this register value is the default value
0xde[7:0] 0xdf[7:0]	mod_coefficient			R/W	tx N value compensation
0xe0[7]	pwdRSSI			R/W	powerdown RSSI
0xe0[6:4]	dsplpctrl			R/W	analog control
0xe0[3]	p11_pusel			R/W	analog control
0xe0[2]	p10_pusel			R/W	analog control
0xe0[1]	PAD_DR			R/W	analog control
0xe0[0]	boost_mode			R/W	boost mode select 0: auto boost 1: digital control
0xe1[7]	lnag			R/W	analog control
0xe1[6:5]]	HQ			R/W	analog control
0xe1[4:0]]	gPA			R/W	analog control
0xe2[7:3]	lbd_thre			R/W	analog control
0xe2[2:0]	lbd_hys			R/W	analog control
0xe3[7]	pwdlbd			R/W	analog control

CONFIDENTIAL

0xe3[6]	lbd_intset			R/W	analog control
0xe3[5]	TXCWEN			R/W	analog control
0xe3[0]	samp_pad_c			R/W	analog control
0xf9[7:3]	fltcal			R	analog indicator
0xf9[2]	pll48_fast			R	analog indicator
0xf9[1]	pll48_slow			R	analog indicator
0xf9[0]	vco_amp_ind			R	analog indicator
0xfa[7:0] 0xfb[7:0]	chip_id			R	chip id/2461
0xfc[7:0] 0xfd[7:0] 0xfe[7:0] 0xff[7:0]	device_id			R	device id
Note: Don't write reserved registers and registers at other addresses in register bank 0					

Table 47 Digital Register

Note:

1. ARD-auto retransmission delay. If the ACK payload is more than 15 byte in 2Mbps mode the ARD must be 500μS or more, if the ACK payload is more than 5byte in 1Mbps mode the ARD must be 500μS or more. In 250kbps mode (even when the payload is not in ACK) the ARD must be 500μS or more.
2. The RX_DR IRQ is asserted by a new packet arrival event. The procedure for handling this interrupt should be: 1) read payload from FIFO, 2) clear RX_DR IRQ, 3) read FIFO_STATUS to check if thereare more payloads available in RX FIFO, 4) if there are more data in RX FIFO, repeat from step 1).
3. Register 0x881 EN_AA only used for RX part now. For TX part, the command W_TX_PAYLOAD used for auto-ack payload, the command W_TX_PAYLOAD_NOACK used for disable-ack payload.

13.7.2 Analog Register

The analog registers can be written through writing 0X8B8 to 0X8BC.
Analog register data [31:0] = {0X8BB, 0X8Ba, 0X8B9, 0X8B8}
Analog register address [7:0] = {0X8BC}
Writing corresponding data and address into these serial registers can update the analog register value.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00		31:0		W	
01		31:0		W	
02		31:0		W	
03		31:0		W	
04		31:0		W	
		25		W	
05		31:0		W	

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		29:26		W	
		11		W	
06		31:0		W	Reserved
07		31:0		W	Reserved
08					Reserved
09					Reserved
0A					Reserved
0B					Reserved
Note: Don't write reserved registers and no definition registers in register bank 1					

Table 48 Register Bank 1

Please contact BEKEN FAE for the default setting used by the analog register.

13.7.3 TX power control setting

The transmit power can be set from -51dBm to 5dBm, to do this, please refer to the next table.

PALDO<1:0> Ana.Reg3<23:22>	PCsel Ana.Reg4<16>	HQ<1:0> Dig.61h<6:5>	gPA<4:0> dig.61h<4:0> Hex	TX Power (dBm)	RF Current (mA)

Table 49 TX power setting

14 Electrical Specifications

RF part

Name	Parameter (Condition)	Min	Typical	Max	Unit	Comment
	Operating Condition					
VDD	Voltage	2.2		3.6	V	

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PSR						
TEMP	Temperature	-20		85	ºC	
	Digital input Pin					
VIH	High level	VDD-0.3		VDD	V	
VIL	Low level	VSS		0.3VDD	V	
	Digital output Pin					
VOH	High level (IOH=-0.25mA)	VDD- 0.3		VDD	V	
VOL	Low level(IOL=0.25mA)	0		0.3	V	
	Normal condition					
IVDD	Dsleep current		3		uA	Total current
IVDD	Idle 16M current		1.3		mA	Total current
IVDD	Idle 32K current		6.5		uA	Total current
	Normal RF condition					
FOP	Operating frequency	2400		2527	MHz	
FXTAL	Crystal frequency		16		MHz	
RFSK	Air data rate	0.25	1	2	Mbps	
	Transmitter					
PRF	Output power		12		dBm	
PBW	Modulation 20 dB bandwidth(2Mbps)		2.5		MHz	
PBW	Modulation 20 dB bandwidth (1Mbps)		2		MHz	
PBW	Modulation 20 dB bandwidth (250Kbps)		1.6		MHz	
PRF1	Out of band emission 2 MHz				dBm	1MHz,RBW=100K TXPOWER=5dBm Maxhold
PRF2	Out of band emission 4 MHz				dBm	
IVDD	Current at -36 dBm output power				mA	Include MCU part
IVDD	Current at -30 dBm output power				mA	
IVDD	Current at -22 dBm output power				mA	
IVDD	Current at -18 dBm output power				mA	
IVDD	Current at -12 dBm output power				mA	
IVDD	Current at -9 dBm output power				mA	
IVDD	Current at -6 dBm output power				mA	
IVDD	Current at -3dBm output power				mA	
IVDD	Current at 0 dBm output power				mA	
IVDD	Current at 3 dBm output power				mA	
IVDD	Current at 12 dBm output power				mA	
	Receiver					
IVDD	Current (2Mbps)		25		mA	
IVDD	Current (1Mbps)		24		mA	
IVDD	Current (250Kbps)		23.5		mA	
Max Input	1 E-3 BER			10	dBm	
RXSENS	1 E-3 BER sensitivity (2Mbps)		-87		dBm	
RXSENS	1 E-3 BER sensitivity (1Mbps)		-90		dBm	
RXSENS	1 E-3 BER sensitivity (250Kbps)		-95		dBm	
C/ICO	Co-channel C/I (2Mbps)				dB	
C/I1ST	ACS C/I 2MHz (2Mbps)				dB	

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C/I2ND	ACS C/I 4MHz (2Mbps)				dB	
C/I3RD	ACS C/I 6MHz (2Mbps)				dB	
C/ICO	Co-channel C/I (1Mbps)		6		dB	
C/I1ST	ACS C/I 1MHz (1Mbps)		6		dB	
C/I2ND	ACS C/I 2MHz (1Mbps)		-17		dB	
C/I3RD	ACS C/I 3MHz (1Mbps)		-32		dB	

MCU part

Name	Parameter (Condition)	Min	Typical （3V）	Max	Unit	Comment
	Core functions					
	Sleep mode		6		uA	RC32K
	Deep sleep mode		2.6 @3V 1.6@2.1V		uA	
	Idle mode at 16M		0.8		mA	
	Idle mode at 8M		0.44		mA	
	Idle mode at 4M		0.26		mA	
	Idle mode at XOSC32k(16M running)		95		uA	
	Active mode (16M)		2.9		mA	
	Active mode (8M)		1.5		mA	
	Active mode (4M)		0.84		mA	
	Active mode (2M)		0.49		mA	
	Active mode (32k)		0.16		mA	
	Active mode (RC32k)		61		uA	
	ADC (8k byte rates)		3.87MA		uA	
	ADC SINAD (fin=1khz, fs=8khz)				DB	
	LBD (always on)				uA	
	GPIO					
	Drive ability		4	8	mA	

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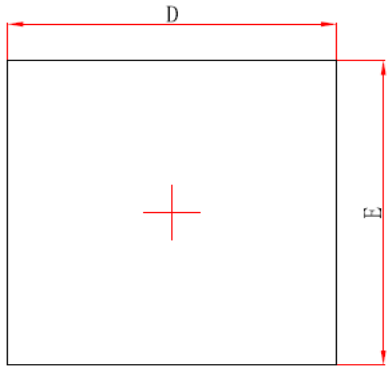
15 Typical Application Schematic

Please refer to the separate documents for detail.

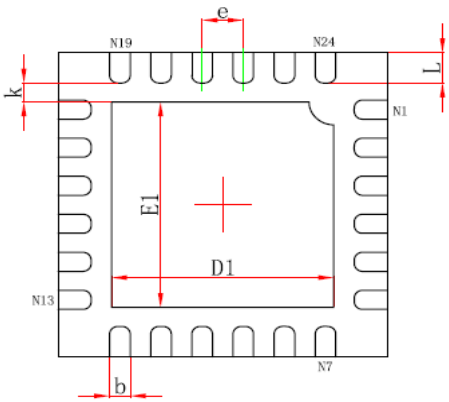
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16 Package Information

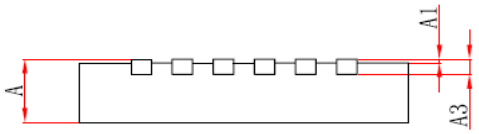
24pin 4X4



Top View

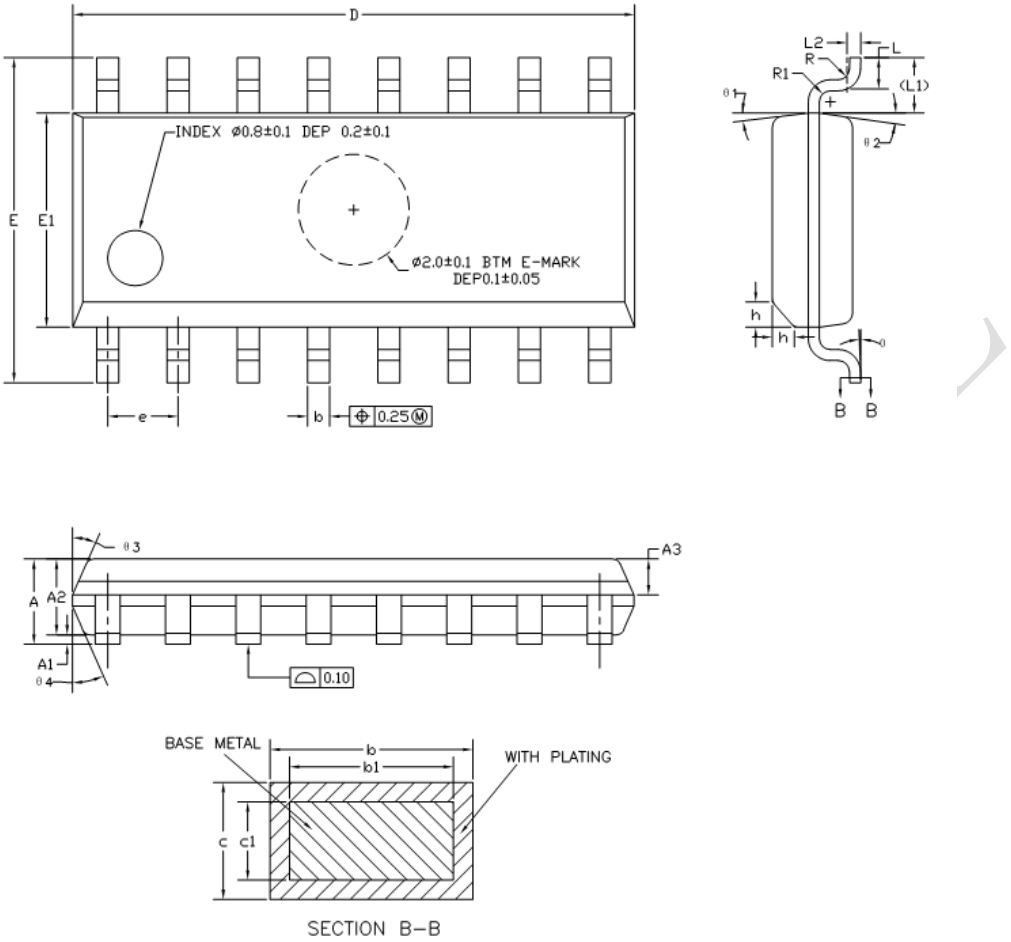


Bottom View



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.020TYP.	
L	0.300	0.500	0.012	0.020

16pin SOP



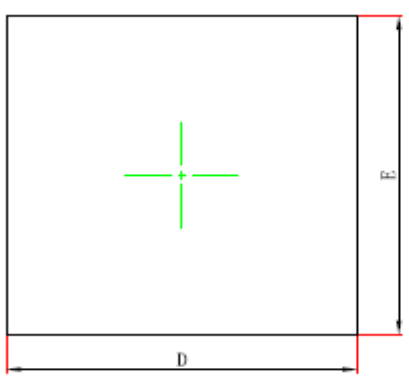
参数	最小	典型	最大	单位
A	1.35	1.60	1.75	mm
A1	0.10	0.15	0.25	mm
A2	1.25	1.45	1.65	mm
A3	0.55	0.65	0.75	mm
b	0.36	-	0.51	mm
b1	0.35	0.40	0.45	mm
c	0.17	-	0.25	mm
c1	0.17	0.20	0.23	mm
D	9.80	9.90	10.00	mm
E	5.80	6.00	6.20	mm
E1	3.80	3.90	4.00	mm
e	1.27 BSC			mm
L	0.45	0.60	0.80	mm
L1	1.04 REF			mm

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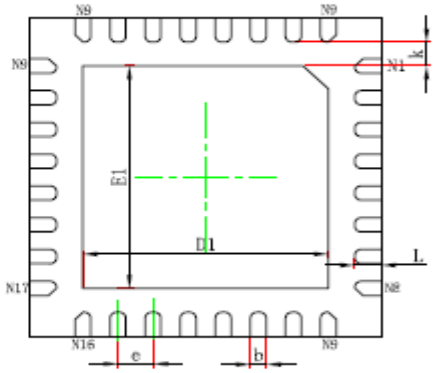
L2	0.25 BSC			mm
R	0.07	-	-	mm
R1	0.07	-	-	mm
h	0.30	0.40	0.50	mm
θ	0	-	8	°
θ1	6	8	10	°
θ2	6	8	10	°
θ3	5	7	9	°
θ4	5	7	9	°

QFN32-4X4

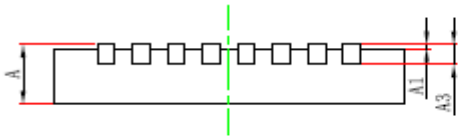
QFNWB4×4-32L-A (P0.40T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.700	2.900	0.106	0.114
E1	2.700	2.900	0.106	0.114
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.224	0.376	0.009	0.015

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17 Solder Reflow Profile

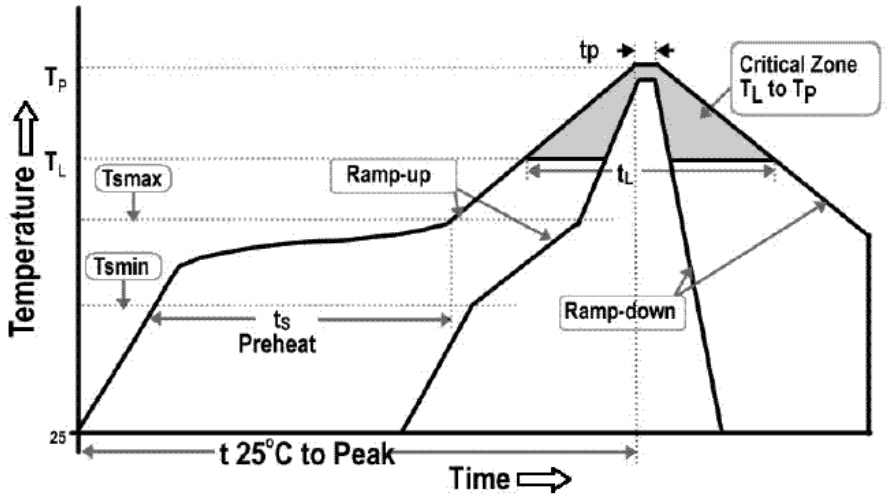


Figure 31 Classification Reflow Profile

Table 50 Solder Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3°C/second max.
Pre_heat	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217°C
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate 6		6°C/second max.
Time 25°C to Peak Temperature 8		8 minutes max.

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18 Order Information

19 Solder Reflow Profile

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20 Contact Information

Beken Corporation Technical Support Center

Shanghai office
Building 41, 1387 Zhangdong Road, Zhangjiang High-Tech Park, Pudong New District, Shanghai, China
Phone: 86-21-51086811
Fax: 86-21-60871089
Postal Code: 201203
Email: info@bekencorp.com
Website: www.bekencorp.com

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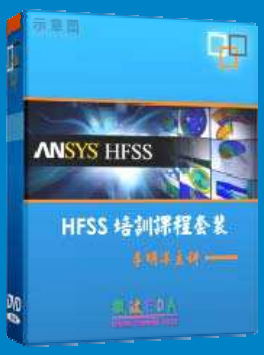
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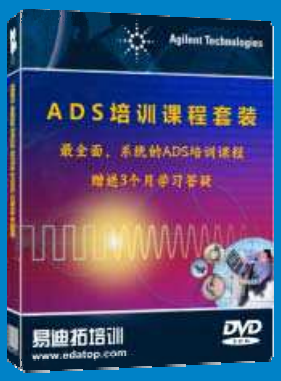


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