128MB – 32Mx40 DDR2 SDRAM UNBUFFERED, ECC, w/PLL

FEATURES

- Unbuffered 200-pin, Small-Outline DIMM (SO-DIMM)
- Suppot ECC error detection and correction
- Fast data transfer rates: PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 667*, 533 and 400 Mb/s DDR2 SDRAM components
- V_{CC} = 1.8V ±0.1V
- V_{CCSPD} = 1.7V to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit prefetch architecture
- Programmable CAS# latency (CL): 3, 4, and 5
- Posted CAS# additive latency; 0, 1, 2, 3 and 4
- Programmable burst: length (4, 8)
- On-die termination (ODT)
- On memory PLL clock
- Serial Presence Detect (SPD) with EEPROM
- Auto & self refresh (64ms: 8,192 cycle refresh)
- Gold edge contacts
- RoHS Compliant
- JEDEC proposed Pin-out
- Package option:
  - 200 Pin (SO-DIMM)
  - PCB – 30.00mm (1.181") TYP.

DESCRIPTION

The WV3HG32M40SEU is a 32Mx40 Double Data Rate 2 SDRAM memory module based on 512Mb DDR2 SDRAM components. The module consists of three 32Mx16, in FBGA package mounted on a 200 pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	333MHz	266MHz	200MHz
CL-t_{RCD}-t_{RP}	5-5-5	4-4-4	3-3-3

Note:
- Consult factory for availability

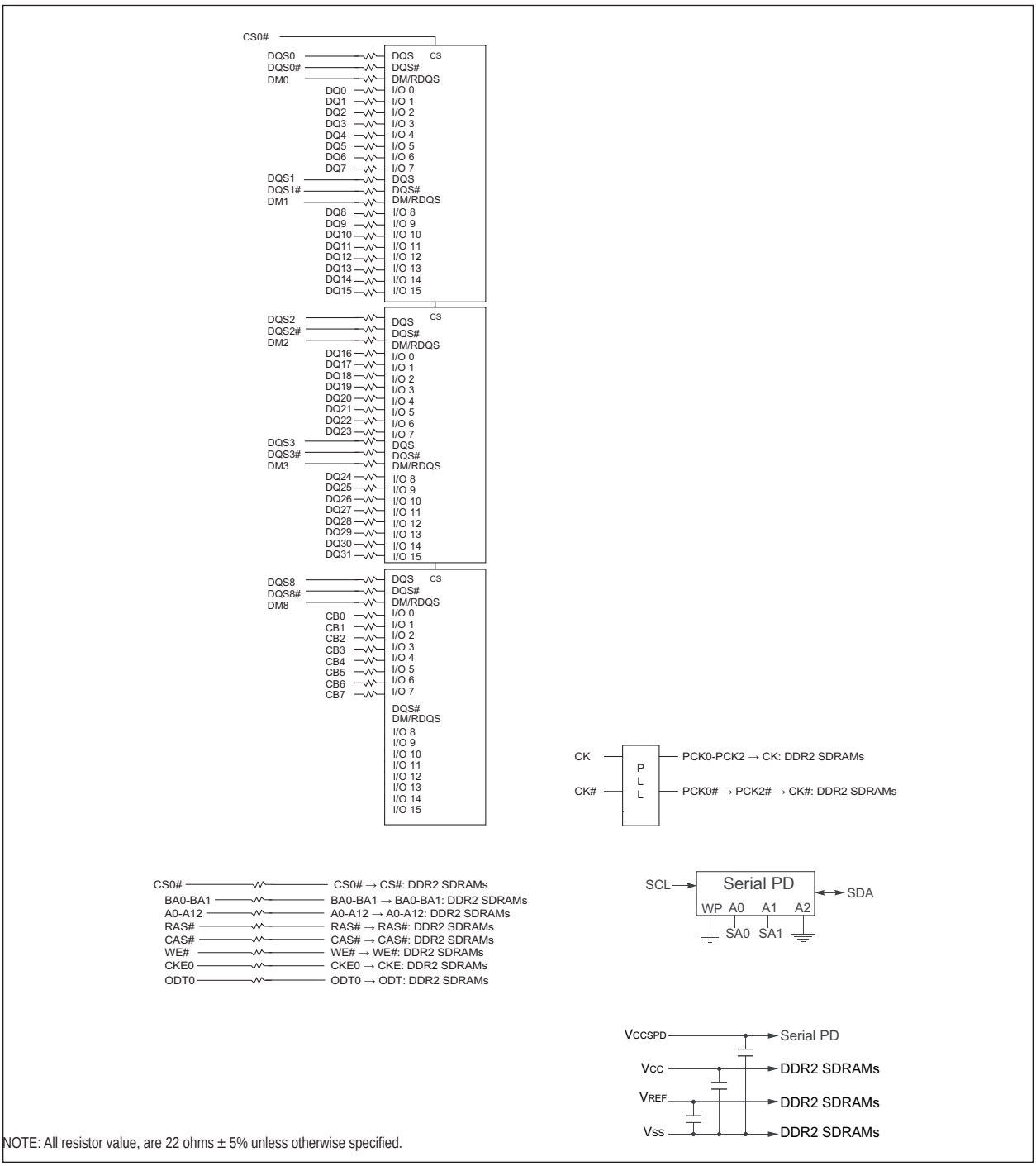
PIN CONFIGURATION

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V_{REF}	51	DQ18	101	V_{CC}	151	V_{SS}
2	V_{SS}	52	V_{SS}	102	A6	152	V_{SS}
3	DQ0	53	DQ19	103	A5	153	NC
4	DQ4	54	DQ28	104	A4	154	NC
5	V_{SS}	55	V_{SS}	105	A3	155	NC
6	DQ5	56	DQ29	106	V_{CC}	156	V_{SS}
7	DQ1	57	DQ24	107	A2	157	V_{SS}
8	V_{SS}	58	V_{SS}	108	A1	158	NC
9	DQS0#	59	DQ25	109	V_{CC}	159	NC
10	DM0	60	DM3	110	A0	160	NC
11	DQS0	61	V_{SS}	111	A10/AP	161	NC
12	V_{SS}	62	V_{SS}	112	BA1	162	V_{SS}
13	V_{SS}	63	DQS3#	113	BA0	163	V_{SS}
14	DQ6	64	DQ30	114	V_{CC}	164	NC
15	DQ2	65	DQS3	115	RAS#	165	NC
16	DQ7	66	DQ31	116	WE#	166	NC
17	DQ3	67	V_{SS}	117	V_{CC}	167	NC
18	V_{SS}	68	V_{SS}	118	CS0#	168	V_{SS}
19	V_{SS}	69	DQ26	119	CAS#	169	V_{SS}
20	DQ12	70	CB4	120	ODT0	170	NC
21	DQ8	71	DQ27	121	NC	171	NC
22	DQ13	72	CB5	122	NC	172	V_{SS}
23	DQ9	73	V_{SS}	123	V_{CC}	173	NC
24	V_{SS}	74	V_{SS}	124	V_{CC}	174	NC
25	V_{SS}	75	CB0	125	NC	175	V_{SS}
26	DM1	76	DM8	126	CK	176	NC
27	DQS1#	77	CB1	127	NC	177	NC
28	V_{SS}	78	V_{SS}	128	CK#	178	V_{SS}
29	DQS1	79	V_{SS}	129	NC	179	NC
30	DQ14	80	CB6	130	V_{SS}	180	NC
31	V_{SS}	81	DQS8#	131	V_{SS}	181	V_{SS}
32	DQ15	82	CB7	132	NC	182	NC
33	DQ10	83	DQS8	133	NC	183	NC
34	V_{SS}	84	V_{SS}	134	NC	184	V_{SS}
35	DQ11	85	V_{SS}	135	NC	185	NC
36	DQ20	86	CB2	136	V_{SS}	186	NC
37	V_{SS}	87	CKE0	137	NC	187	V_{SS}
38	DQ21	88	CB3	138	NC	188	NC
39	DQ16	89	NC	139	V_{SS}	189	NC
40	V_{SS}	90	V_{SS}	140	V_{SS}	190	V_{SS}
41	DQ17	91	NC	141	NC	191	NC
42	NC	92	NC	142	NC	192	NC
43	V_{SS}	93	V_{CC}	143	NC	193	NC
44	DM2	94	NC	144	NC	194	SDA
45	DQS2#	95	A12	145	V_{SS}	195	V_{SS}
46	V_{SS}	96	A11	146	V_{SS}	196	SCL
47	DQS2	97	A9	147	NC	197	NC
48	DQ22	98	V_{CC}	148	NC	198	SA1
49	V_{SS}	99	A7	149	NC	199	V_{CC}SPD
50	DQ23	100	A8	150	NC	200	SA0

PIN NAMES

SYMBOL	DESCRIPTION
A0-A12	Address input
ODT0	On-Die Termination
CK, CK#	Clock Input
CB0 - CB7	Check Bits
CKE0	Clock Enable input
CS0#	Chip select
RAS#, CAS#, WE#	Command Inputs
BA0, BA1	Bank Address Inputs
DM0-DM3, DM8	Input Data Mask
DQ0-DQ31	Data Input/Output
DQS0-DQS3, DQS8	Data Strobe
DQS03-DQS3#, DQS8#	Data Strobe Complement
SCL	SPD Clock Input
SA0-SA1	SPD Address Inputs
SDA	Serial Data Input/Output
V_{CC}	Power Supply
V_{REF}	Input/Output reference voltage
V_{SS}	Ground
V_{CCSPD}	Serial EEPROM Power Supply
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: All resistor value, are 22 ohms ± 5% unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	˚C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V<V_{IN}<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#	-15	15	µA
		CS#, CKE	-15	15	µA
		CK, CK#	-10	10	µA
		DM	-5	5	µA
I_{OZ}	Output leakage current; 0V<V_{IN}<V_{CC}; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-6	6	µA

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Rating			Units	Notes
		Min.	Type	Max.		
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	3
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.50 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	2
SPD Supply Voltage	V_{CCSPD}	1.7	-	3.6	V	

Notes:

1. V_{REF} is expected to equal V_{CC}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
2. V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
3. V_{CCQ} of all IC's are tied to V_{CC}.

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	7	10	pF
Input Capacitance CKE0, ODT0	C_{IN2}	7	10	pF
Input Capacitance CS0#	C_{IN3}	7	10	pF
Input Capacitance (CK, CK#)	C_{IN4}	6	7	pF
Input Capacitance (DM0 ~ DM3, DM8), (DQS0 ~ DQS3, DQS8)	C_{IN5} (665)	6.5	7.5	pF
	C_{IN5} (534)	6.5	8	pF
Input Capacitance (DQ0 ~ DQ31) (CB0 ~ CB7)	C_{OUT1} (665)	6.5	7.5	pF
	C_{OUT1} (534)	6.5	8	pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature (Commercial)	TOPER	0° to 85°	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(AC)	V_{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V_{IH}(AC)	V_{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(AC)	-	V_{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667	V_{IL}(AC)	-	V_{REF} - 0.200	V

DDR2 I_{CC} SPECIFICATION AND CONDITIONS

Symbol	Proposed Conditions		665	534	403	Units
I_{CC0}*	Operating one bank active-precharge; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}\min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		660	630	615	mA
I_{CC1}*	Operating one bank active-read-precharge; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}\min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		720	690	675	mA
I_{CC2P}**	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		330	330	324	mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		390	375	360	mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		405	390	375	mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	405	390	330	mA
		Slow PDN Exit MRS(12) = 1	360	360	360	mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC}, t_{RAS} = t_{RAS}\min(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		480	450	450	mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}\max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		990	885	780	mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}\max(I_{CC})$, $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W		990	885	780	mA
I_{CC5}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1,110	1,050	990	mA
I_{CC6}**	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	18	18	18	mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = $t_{RC}D(I_{CC})$-1*$t_{CK}(I_{CC})$; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, t_{RCD} = 1*$t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		1,725	1,470	1,245	mA

I_{CC} specification is based on ELPIDA components. Other DRAM manufactures specification may be different.

Note:

*: Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
	Clock Cycle Time	CL = 5	$t_{CK\ (5)}$	3,000	8,000					ps
		CL = 4	$t_{CK\ (4)}$	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	$t_{CK\ (3)}$	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
	Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		MIN (t_{CH}, t_{CL})		ps
	Clock jitter		t_{JIT}	-125	125	-125	125	-125	125	ps
Data	DQ output access time from CK/CK#		t_{AC}	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t_{HZ}		t_{AC} MAX		t_{AC} MAX		t_{AC} MAX	ps
	Data-out low-impedance window from CK/CK#		t_{LZ}	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	t_{AC} MIN	t_{AC} MAX	ps
	DQ and DM input setup time relative to DQS		t_{DS}	100		100		150		ps
	DQ and DM input hold time relative to DQS		t_{DH}	175		225		275		ps
	DQ and DM input pulse width (for each input)		t_{DIPW}	0.35		0.35		0.35		t_{CK}
	Data hold skew factor		t_{QHS}		340		400		450	ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ps
	Data valid output window (DVW)		t_{DVW}	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
Data Strobe	DQS input high pulse width		t_{DQSH}	0.35		0.35		0.35		t_{CK}
	DQS input low pulse width		t_{DQSL}	0.35		0.35		0.35		t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}	-400	+400	-450	+450	-500	+500	ps
	DQS falling edge to CK rising ... setup time		t_{DSS}	0.2		0.2		0.2		t_{CK}
	DQS falling edge from CK rising ... hold time		t_{DSH}	0.2		0.2		0.2		t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		240		300		350	ps
	DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
	DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	DQS write preamble setup time		t_{WPRES}	0		0		0		ps
	DQS write preamble		t_{WPRE}	0.35		0.35		0.35		t_{CK}
	DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
	Write command to first DQS latching transition		t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}
	Address and control input pulse width for each input		t_{IPW}	0.6		0.6		0.6		t_{CK}
	Address and control input setup time		t_{IS}	200		250		350		ps
	Address and control input hold time		t_{IH}	275		375		475		ps
	Address and control input hold time		t_{CCD}	2		2		2		t_{CK}

Note:
AC specification is based on ELPIDA components. Other DRAM manufactures specification may be different.
Continued on next page

AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}	55		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10		10		10		ns
	ACTIVE to READ or WRITE delay	t_{RCD}	15		15		15		ns
	Four Bank Activate period	t_{FAW}	50		50		50		ns
	ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	ns
	Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		ns
	Write recovery time	t_{WR}	15		15		15		ns
	Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns
	Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		10		ns
	PRECHARGE command period	t_{RP}	15		15		15		ns
	PRECHARGE ALL command period	t_{RPA}	$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		$t_{RP}+t_{CK}$		ns
	LOAD MODE command cycle time	t_{MRD}	2		2		2		t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		$t_{IS} + t_{CK} + t_{IH}$		ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t_{RFC}	105	70,000	105	70,000	105	70,000	ns
	Average periodic refresh interval	t_{REF}I		7.8		7.8		7.8	µs
	Exit self refresh to non-READ command	t_{XSNR}	t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		t_{RFC} (MIN) + 10		ns
	Exit self refresh to READ command	t_{XSRD}	200		200		200		t_{CK}
	Exit self refresh timing reference	tI_{SXR}	t_{IS}		t_{IS}		t_{IS}		ps
ODT	ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
	ODT turn-on	t_{AON}	t_{AC} (MIN)	t_{AC} (MAX) + 700	t_{AC} (MIN)	t_{AC} (MAX) + 1000	t_{AC} (MIN)	t_{AC} (MAX) + 1000	ps
	ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
	ODT turn-off	t_{AOF}	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	t_{AC} (MIN)	t_{AC} (MAX) + 600	ps
	ODT turn-on (power-down mode)	t_{AONPD}	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	t_{AC} (MIN) + 2000	2.5 x t_{CK} + t_{AC} (MAX) + 1000	ps
	ODT to power-down entry latency	t_{ANPD}	3		3		3		t_{CK}
	ODT power-down exit latency	t_{AXPD}	8		8		8		t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2		2		2		t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7 - AL		6 - AL		6 - AL		t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}	2		2		2		t_{CK}
	CKE minimum high/low time	t_{CKE}	3		3		3		t_{CK}

Note:
AC specification is based on ELPIDA components. Other DRAM manufactures specification may be different.

ORDERING INFORMATION FOR PD4

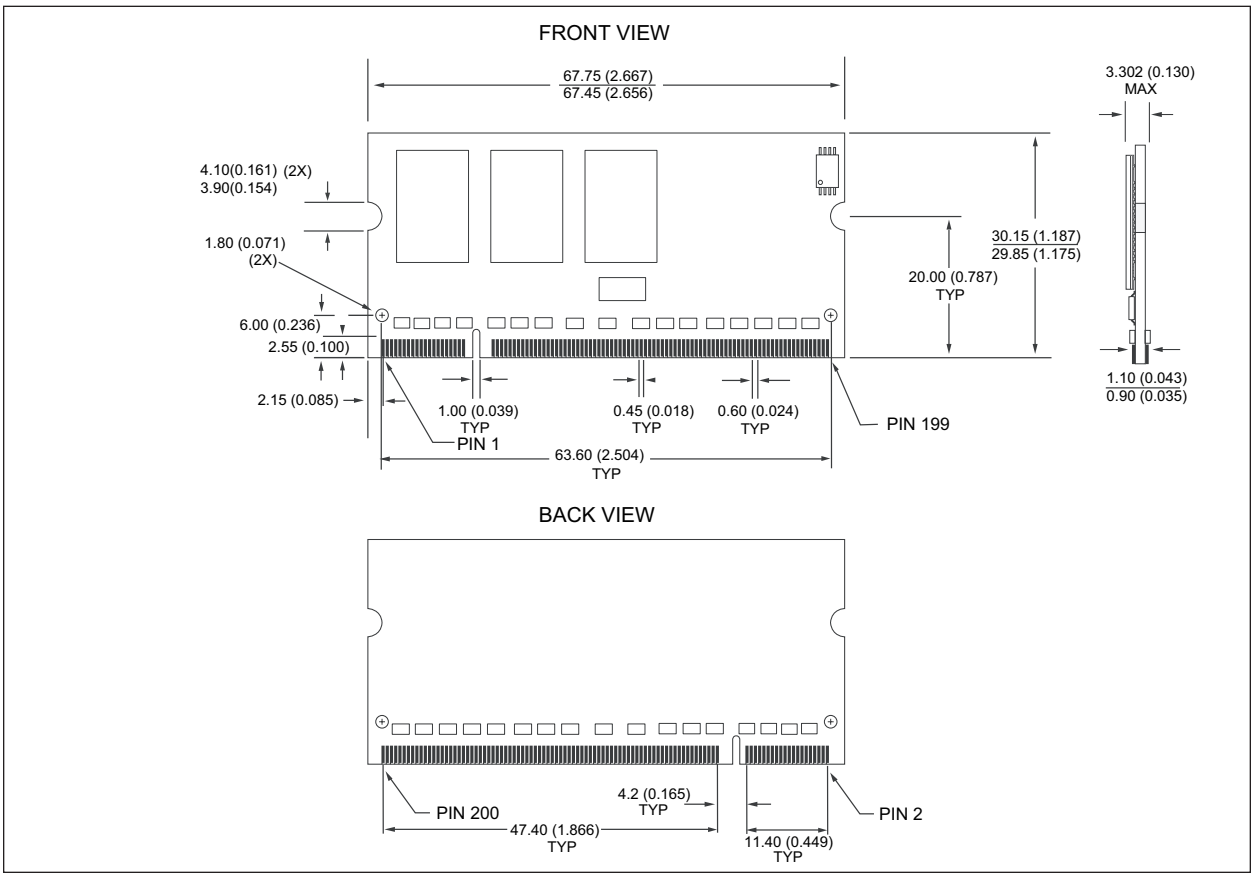
Part Number	Clock/Data Rate Frequency	CAS Latency	t_{RCD}	t_{RP}	Height**
WV3HG32M40SEU665PD4xxG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG32M40SEU534PD4xxG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG32M40SEU403PD4xxG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

* Consult Factory for availability

NOTES:

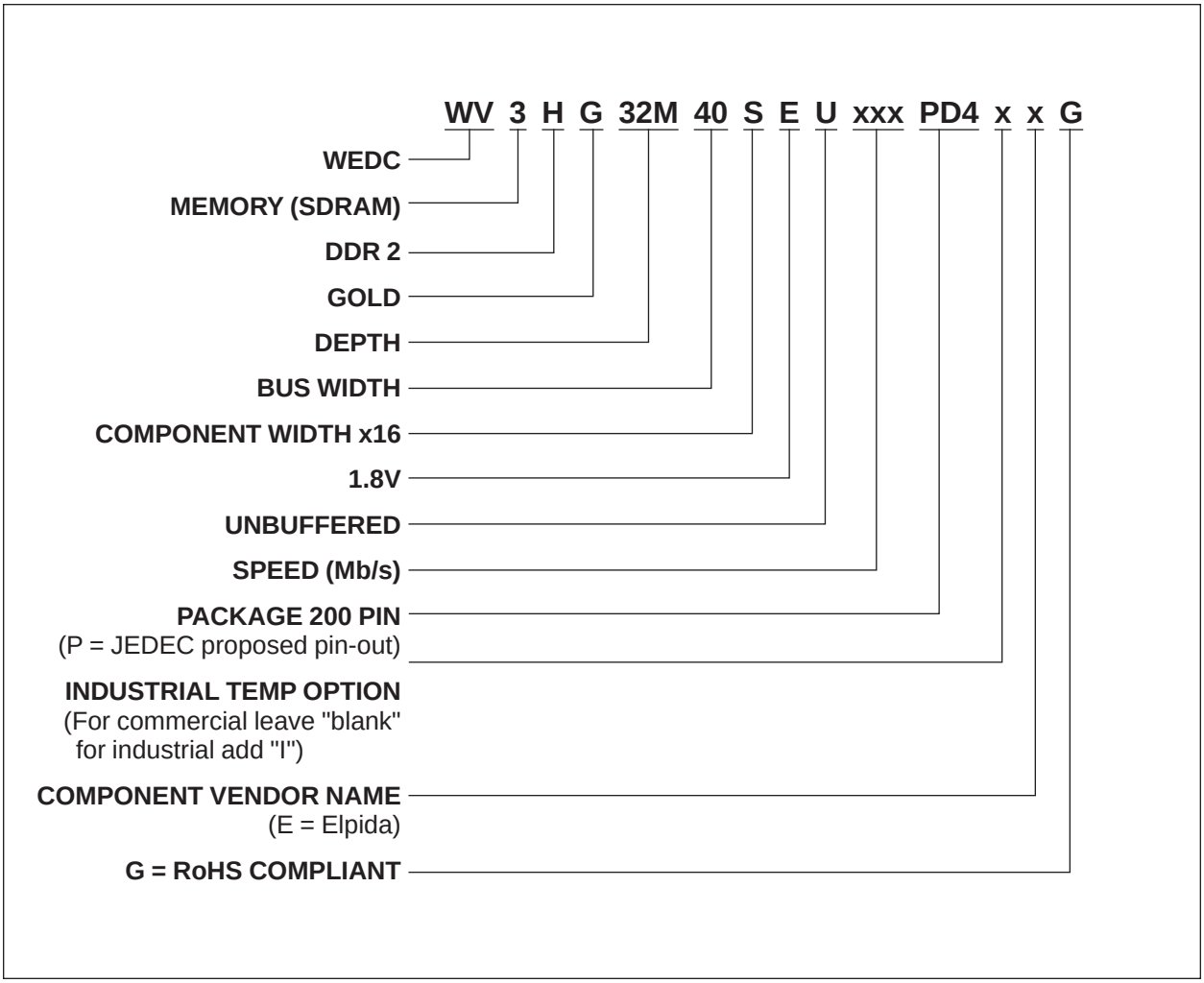
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung, Elpida & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR PD4



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

128MB – 32Mx40 DDR2 SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- ELPIDA: F-Die

Rev #	History	Release Date	Status
Rev 0	Created	6-06	Concept
Rev 1	1.0 Update to x40 depth 1.1 Added CB4, CB5, CB6, and CB7 1.2 Indicated SPD supply voltage 1.3 Change part number to indicated x40 (8 ECC bits)	6-8-06	Concept
Rev 2	2.0 Moved from concept to advanced	6-9-06	Advanced