FEATURES

- 5V to 7V gate drivers with 6A GATEL sink current and 4A GATEH sink current
- 4.5V to 14V VIN range
- Local lossless inductor current sensing with improved noise immunity and accuracy
- Single reference based current reporting output
- Integrated bootstrap synchronous PFET
- Tri-state PWM diode emulation mode for optimal light load efficiency
- 7V tolerant PWM input compatible with 3.3V logic
- MOSFET monitoring with PHSFLT output
- Over temperature reporting
- Only four external components per phase
- Self-calibration of current sense amplifier input offset to maximize accuracy
- Body-Braking™ feature with active low logic
- RoHS compliant , small thermally enhanced 16L 3 X 3mm MLPQ package

APPLICATIONS

- Server, notebook and desktop computers
- Game consoles
- Consumer electronics – STB, LCD, TV, printers
- General purpose POL DC-DC converters

DESCRIPTION

The IR3535 is a high performance, floating N-channel MOSFET driver that is optimized for maximum efficiency delivery of a synchronous buck converter. It is a "Smart" driver that continually monitors MOSFET conditions, contains self-calibrating inductor current sense amplifier, and provides diode emulation mode with local zero current detection.

The integrated current sense amplifier achieves superior current sense accuracy vs. best-in-class controller based inductor DCR sense methods while delivering the clean and accurate current report information.

The IR patented Body-Braking™ feature reduces inductor to output capacitor energy transfer during load release which allows the output capacitor bank to be reduced.

Diode emulation mode in the IR3535 alleviates the zero-current detection and control burden from the PWM controller and increases system light load efficiency.

The IR3535 monitors MOSFET conditions and temperature and reports phase fault if MOSFET short, MOSFET open or over temperature is detected.

Up to 1.0MHz switching frequency capability enables high performance transient response, miniaturization of output inductors, as well as reduced input and output capacitors while maintaining industry leading efficiency. Solution size, thermal performance and cost can be optimized by combining with IR's DirectFET™ MOSFETs and utilizing a dual sided layout.

BASIC APPLICATION

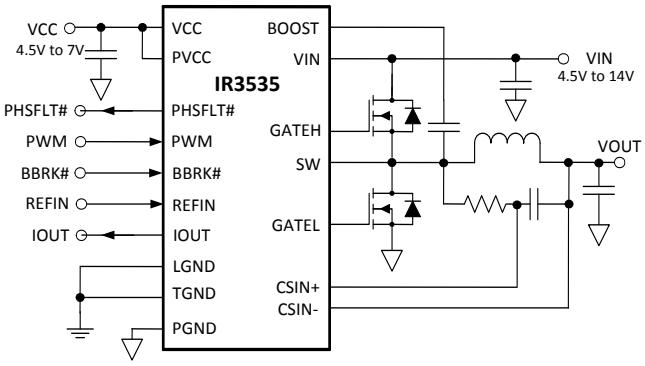

Figure 1: IR3535 Basic Application Circuit

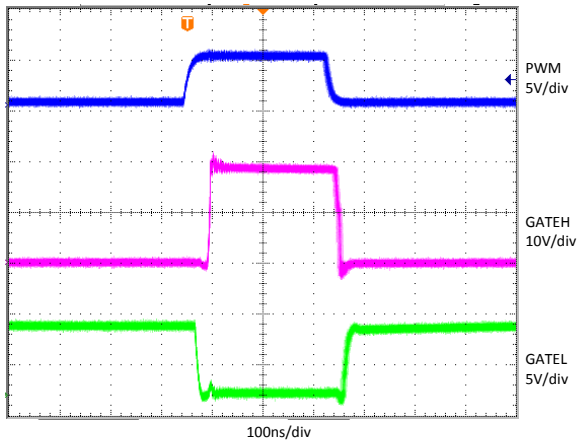

Figure 2: IR3535 Gate Driver Waveforms

ORDERING INFORMATION

Package	Tape & Reel Qty	Part Number
16 Lead MLPQ (3 x 3 mm body)	3000	**IR3535MTRPBF**

PIN DIAGRAM

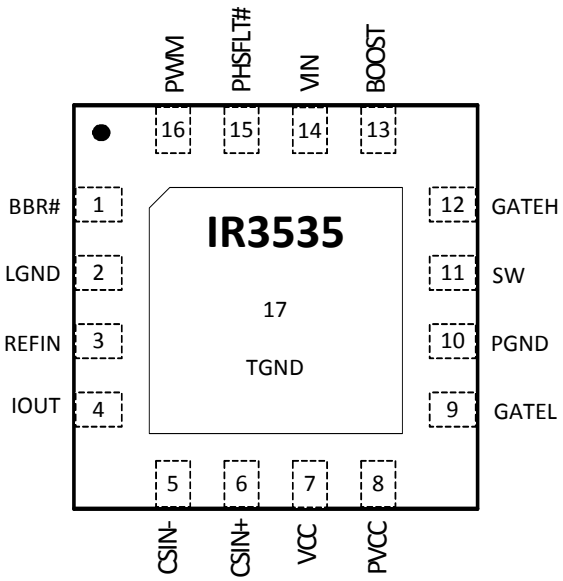

Figure 3: IR3535 Pin Diagram (Top View)

FUNCTIONAL BLOCK DIAGRAM

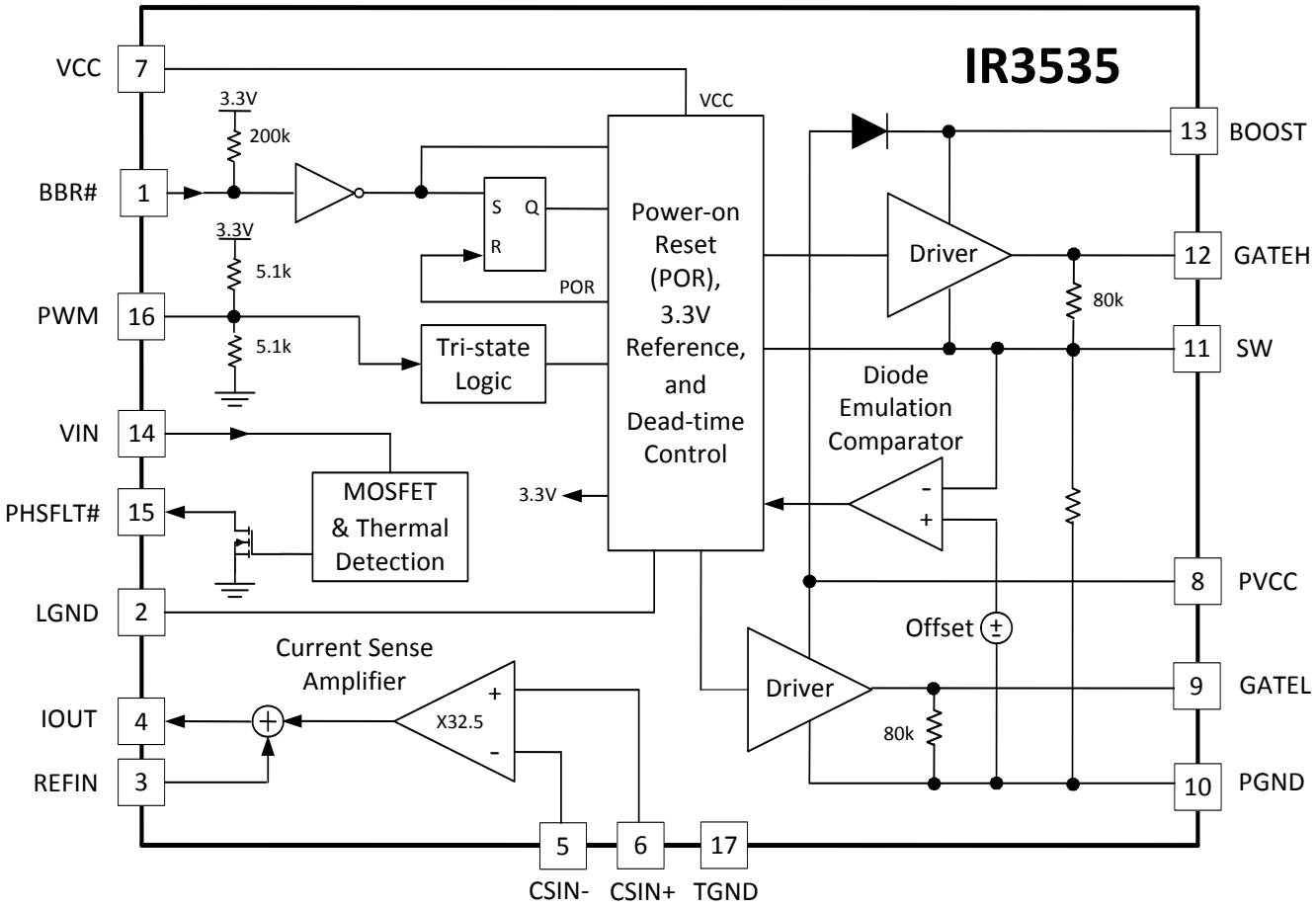

Figure 4: IR3535 Functional Block Diagram

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	BBR#	3.3V logic level input, 7V tolerant, with internal weak pull-up to 3.3V. Logic "Low" to disable both MOSFETs. Pulling BBR# low momentarily after VCC passes its UVLO threshold activates the Diode Emulation Mode.
2	LGND	Ground for control logic and analog circuits. IC substrate is connected to this pin.
3	REFIN	Reference voltage input from the PWM controller. The current sense signal is referenced to the voltage on this pin. Connect to LGND if the current sense amplifier is not used.
4	IOUT	Voltage on this pin is equal to V(REFIN) + 32.5 * [V(CSIN+) – V(CSIN-)]. Float this pin if the current sense amplifier is not used.
5	CSIN-	Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
6	CSIN+	Non-Inverting input to the current sense amplifier. Connect to LGND if the current sense amplifier is not used.
7	VCC	Bias voltage for control logic and analog functions.
8	PVCC	Voltage for low-side MOSFET driver. Internal bootstrap synchronous PFET is connected from this pin to the BOOST pin. Connect a 1uF capacitor between PVCC and PGND.
9	GATEL	Low-side driver output and input to GATEH non-overlap comparator.
10	PGND	Return for low side driver and reference for GATEH non-overlap comparator.
11	SW	Return for high-side driver and reference for GATEL non-overlap comparator.
12	GATEH	High-side driver output and input to GATEL non-overlap comparator.
13	BOOST	Supply for high-side driver. Internal bootstrap synchronous PFET is connected between this pin and the PVCC pin. Connect a minimum 0.22µF 16Vdc capacitor from BOOST to SW pin.
14	VIN	Power rail input for phase fault detection.
15	PHSFLT#	Open collector output of the phase fault comparators. 7V tolerant, connect to an external pull-up resistor. Output is low when a MOSFET fault or over temperature condition is detected.
16	PWM	3.3V logic level Tri-state PWM input, 7V tolerant. "High" turns the control MOSFET on, and "Low" turns the synchronous MOSFET on. "Tri-state" turns the control MOSFET off without delay. Depending on the mode the IR3535, "Tri-state" either turns the synchronous MOSFET off without delay in Body-Braking™ mode or turns synchronous MOEFET off when the current reaches zero in diode emulation mode. See "Theory of Operation" section for further details.
17	TGND	Ground pad for thermal dissipation. Connected to IC substrate. Connect this pad to ground planes through four vias.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Storage Temperature Range	-65°C to 150°C
Operating Junction Temperature	0°C to 150°C
ESD Rating	HBM Class 1C JEDEC Standard
MSL Rating	2
Reflow Temperature	260°C

PIN Number	PIN NAME	V_{MAX}	V_{MIN}	I_{SOURCE}	I_{SINK}
1	BBR#	8V	-0.3V	1mA	1mA
2	LGND	n/a	n/a	n/a	n/a
3	REFIN	3.5V	-0.3V	1mA	1mA
4	IOUT	8V	-0.3V	5mA	5mA
5	CSIN-	8V	-0.3V	1mA	1mA
6	CSIN+	8V	-0.3V	1mA	1mA
7	VCC	8V	-0.3V	n/a	15mA
8	PVCC	8V	-0.3V	n/a	5A for 100ns, 100mA DC
9	GATEL	8V	-0.3V DC, -5V for 100ns	5A for 100ns, 200mA DC	7A for 100ns, 200mA DC
10	PGND	0.3V	-0.3V	7A for 100ns, 200mA DC	n/a
11	SW	25V	-0.3V DC, -10V for 100ns	5A for 100ns, 100mA DC	n/a
12	GATEH	33V	-0.3V DC, -10V for 100ns	5A for 100ns, 100mA DC	5A for 100ns, 100mA DC
13	BOOST	33V	-0.3V	1A for 100ns, 100mA DC	3A for 100ns, 100mA DC
14	VIN	16V	-0.3V	n/a	1mA
15	PHSFLT#	8V	-0.3V	1mA	20mA
16	PWM	8V	-0.3V	1mA	1mA

Note:
1. Maximum GATEH – SW = 8V
2. Maximum BOOST – GATEH = 8V

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

	SYMBOL	MIN	MAX	UNITS
Recommended VIN Range	VIN	4.5	14	V
Recommended VCC Range	VCC	4.5	7	V
Recommended REFIN Range (V_{CC} = 4.5V to 5.5V)	REFIN	0.25	2.0	V
Recommended REFIN Range (V_{CC} = 5.5V to 7V)	REFIN	0.25	3.3	V
Recommended Switching Frequency	F_{SW}	200	1000	kHz
Recommended Operating Junction Temperature	T_J	0	125	°C

ELECTRICAL CHARACTERISTICS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C.

C_{GATEH} = 3.3nF, C_{GATEL} = 6.8nF (unless otherwise specified).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Gate Drivers					
GATEH Source Resistance	BOOST – SW = 7V		670		MΩ
GATEH Sink Resistance	BOOST – SW = 7V		670		MΩ
GATEL Source Resistance	PVCC – PGND = 7V		670		MΩ
GATEL Sink Resistance	PVCC – PGND = 7V		300		MΩ
GATEH Source Current	BOOST = 7V, GATEH = 2.5V, SW = 0V		3		A
GATEH Sink Current	BOOST = 7V, GATEH = 2.5V, SW = 0V		4		A
GATEL Source Current	PVCC = 7V, GATEL = 2.5V, SW = 0V		4		A
GATEL Sink Current	PVCC = 7V, GATEL = 2.5V, SW = 0V		6		A
GATEH Rise Time	BOOST – SW = 7V, measure 1V to 4V transition time		5	10	ns
GATEH Fall Time	BOOST – SW = 7V, measure 4V to 1V transition time		4	8	ns
GATEL Rise Time	PVCC – PGND = 7V, measure 1V to 4V transition time		10	20	ns
GATEL Fall Time	PVCC – PGND = 7V, measure 4V to 1V transition time		5	10	ns
GATEL Low to GATEH High Delay	BOOST = PVCC = 7V, SW = PGND = 0V, measure time from GATEL falling to 1V to GATEH rising to 1V	10	15	30	ns
GATEH Low to GATEL High Delay	BOOST = PVCC = 7V, SW = PGND = 0V, measure time from GATEH falling to 1V to GATEL rising to 1V	10	15	30	ns
Disable Pull Down Resistance	GATEH to SW, GATEL to PGND	30	80	130	KΩ

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PWM Comparator					
High Side Switch Threshold	PWM Low or PWM Tri-State to High	2.5			V
Low Side Switch Threshold	PWM High or PWM Tri-State to Low			0.8	V
PWM Tri-State Float Voltage	Floating	1.2	1.65	2.1	V
Hysteresis	Active to Tri-State to Active, Note 1	65	76	100	mV
Tri-State Propagation Delay Time	C_{PWM} = 20pF, measure from V(PWM) = 0V to GATEL < 1V			190	ns
	C_{PWM} = 20pF, measure from V(PWM) = 5V release to GATEH < 1V			380	ns
PWM Input					
Sinking Impedance		3.67	5.1	8.7	KΩ
Source Impedance		3.67	5.1	8.7	KΩ
GATEH Turn-Off Propagation Delay	Measure from V(PWM) falling edge to GATEH < 1V		25	45	ns
Current Sense Amplifier					
CSIN+/- Bias Current		-100	0	100	nA
Input Offset Voltage	CSIN+ = CSIN- = REFIN, measure input referred offset from REFIN	-750		750	µV
Calibrated Input Offset Voltage	Self-calibrated offset, Note 1	-450	0	450	µV
Gain	0.5V ≤ V(REFIN) < 2.25	30	32.5	35	V/V
Unity Gain Bandwidth	C(IOUT) = 10pF, measure at IOUT. Note 1	4.8	6.8	8.8	MHz
Slew Rate			6		V/µs
Differential Input Range	0.8V ≤ V(REFIN) ≤ 2.25V, Note 1	-10		25	mV
	0.25V ≤ V(REFIN) ≤ 0.8V, Note 1	-5		25	mV
Common Mode Input Range		0		VCC – 2.5	V
Output Impedance			62	200	Ω
IOUT Sink Current	Driving external 3 kΩ	0.5	0.8	1.1	mA
Bootstrap Diode					
Forward Voltage	I(BOOST) = 30mA, VCC = 6.8V	360	520	960	mV
Digital Output — Phase Fault					
VOH	HIGH Level Pull-Up Voltage			7	V
VOL	I(PHSFLT#) = 4mA		150	300	mV
Leakage Current	V(PHSFLT#) = 5.5V		0	1	µA
Phase Fault Detection					
Top Side Threshold	Measure from Vin to SW	1.9	2.2	2.5	V
Bottom Side Threshold		150	200	250	mV
Bottom FET Open Threshold		-250	-215	-180	mV
Propagation Delay	PWM High to PWM Low Cycles		15		Cycles

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Bias Voltage		4.5		7	V
Digital Input — BBR#					
VIL	Input Low Threshold	0.8			V
VIH	Input High Threshold			2.0	V
Internal Pull Up Resistance	VCC > UVLO	69	200	340	KΩ
Internal Pull Up Voltage	VCC > UVLO		3.3		V
General					
VCC Supply Current		4	8	12	mA
VIN Supply Curent	4.5 ≤ V(VIN) ≤ 14V	0.05	0.15	0.4	mA
Switch Node Bias Current				5	mA
BOOST Supply Current	4.75 ≤ V(BOOST) – V(SW) ≤ 7V	0.5	1.5	3	mA
REFIN Bias Current		-1.5	0	1	µA
SW Floating Voltage	CSIN- tied to SW, PWM Tri-State	0.1	0.3	0.4	V
Diode Emulation Mode Comparator					
Input Offset Voltage	Note 2	-12	-3	3	mV
Leading Edge Blanking Time	V(GATEL) > 1V Starts Timer, Note 1	100	150	200	ns
Propagation Delay	Blanking Expired, +2.5mV overdrive to V(GATEL) < 1V, Note 1		41	50	ns
Negative Current Time-Out	PWM = Tri-State, V(SW) < = -10mV	20	30	45	µs
VCC Under Voltage Lockout					
Start		3.3	3.7	4.1	V
Stop		3	3.4	3.8	V
Hysteresis		0.25	0.35	0.45	V
Thermal Flag					
Rising Threshold	PHSFLT# Drives Low. Note 1		115		°C
Falling Threshold	Note 1		95		°C

Note:

1. Guaranteed by design but not tested in production
2. The Diode Emulation Mode (DEM) comparator measures the SW against PGND. The input offset is biased slightly to the negative so that a slightly positive current in the synchronous MOSFET is treated as zero current to accommodate propagation delays and untrimmed accuracy.

THEORY OF OPERATION

DESCRIPTION

The IR3535 is a synchronous buck driver which provides system designers with ease of use and flexibility required in cutting edge CPU, GPU and memory power delivery designs. The IR3535 is designed to work with a controller that provides the PWM signal. The IR3535 incorporates a continuously self-calibrated current sense amplifier, optimized for use with inductor DCR sensing. The current sense amplifier provides signal gain and noise immunity, providing multiphase systems with a superior design toolbox for programmed impedance designs.

The IR3535 also provides a phase fault signal capable of detecting open or shorted MOSFETs, or an over-temperature condition in the vicinity of the driver.

The IR3535 accepts an active low Body-Braking™ input which disables the output MOSFETs to enhance transient performance or provide a high impedance output.

The IR3535 PWM input is compatible with 3.3V logic and 7V tolerant. It accepts 3-level PWM input signals, with a diode emulation feature when the PWM signal is floated, allowing designers to maximize system efficiency at light loads without compromising transient performance.

BODY-BRAKING™ MODE

There are two ways to place the IR3535 in Body-Braking™ mode, in which two MOSFETs are turned off.

Pulling BBR# low forces the IR3535 into Body-Braking™ mode rapidly, which is used to enhance transient response after load release or provide a high impedance output.

If the BBR# input is high and has not been low since power on, the Body-Braking™ is activated when the PWM input enters the tri-state region, which is withing a range around 1.65V. The Body-Braking™ response is slower due to the hold-off time created by the paracitic capacitor with pull-up or pull-down resistor at PWM pin. For better performance, no more than 100pF parasitic capacitive load should be present on the PWM line of IR3535.

DIODE EMULATION MODE

An additional feature of the IR3535 is diode emulation mode. This function improves efficiency by preventing negative inductor current from flowing in the synchronous MOSFET.

As shown in Figure 5, when the PWM input enters the tri-state region the control MOSFET is turned off first, and the synchronous MOSFET is initially turned on and then is turned off when the output current reaches zero. If the sensed output current does not reach zero within a set amount of time the gate driver will assume that the output is de-biased and turn off the synchronous MOSFET, allowing the switch node to float.

This is in contrast to the Body-Braking® mode shown in Figure 6, where GATEL follows PWM input. The Schottky diode in parallel with the synchronous MOSFET conducts for a longer period of time and therefore lowers the light load efficiency.

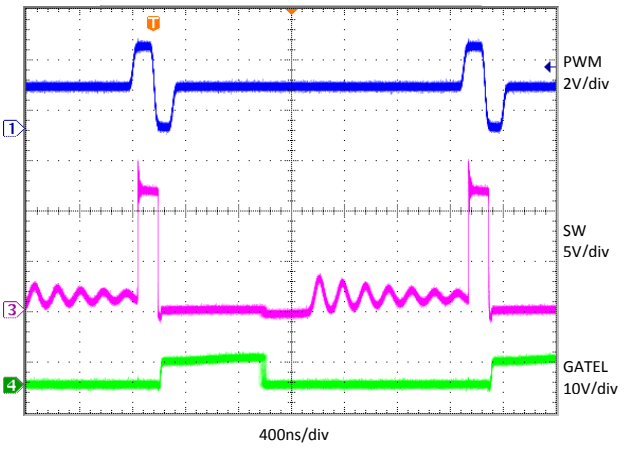

Figure 5: Diode Emulation Mode

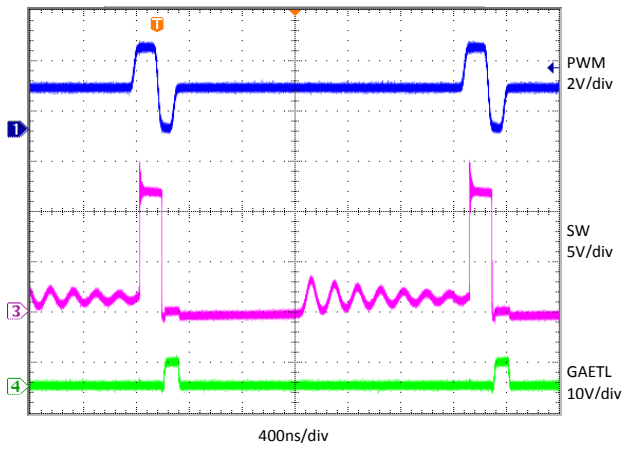

Figure 6: Body-Braking® Mode

The zero current detection circuit in the IR3535 is independent of the current sense amplifier and therefore still functions even if the current sense amplifier is not used. As shown in Figure 4, an offset is added to the diode emulation comparator so that a slightly positive output current in the inductor and synchronous MOSFET is treated as zero current to accommodate propagation delays, preventing any negative current flowing in the synchronous MOSFET. This causes the Schottky diode in parallel with the synchronous MOSFET to conduct before the inductor current actually reaches zero, and the conduction time increases with inductance of the output inductor.

To set the IR3535 in diode emulation mode, the BBR# pin must be toggled low at least once after the VCC passes its UVLO threshold during power up. One simple way is to use the internal BBR# pull-up resistor (200kΩ typical) with an external capacitor from BBR# pin to LGND. To ensure the diode emulation mode is properly set, the BBR# voltage should be lower than 0.8V when the VCC voltage passes its UVLO threshold (3.3V minimum and 3.7V typical), as shown in Figure 7. A digital signal from the PWM controller can also be used to set the diode emulation mode. The BBR# signal can either be pulled low for at least 20ns after the VCC passes its UVLO threshold, as shown in Figure 8, or be pulled low before VCC power up and then released after the VCC passes its UVLO threshold, as shown in Figure 9.

Once the diode emulation mode is set, it cannot be reset until the VCC power is recycled.

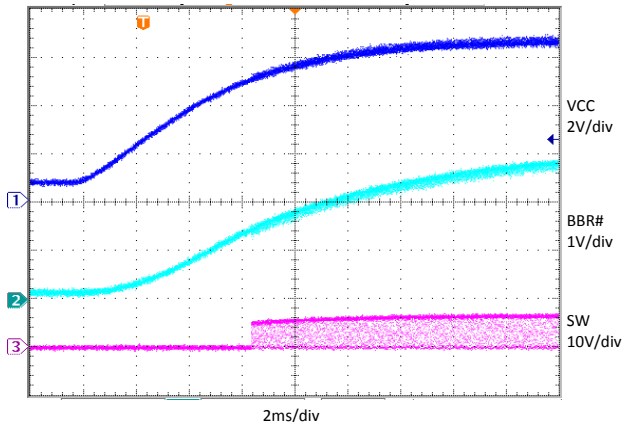

Figure 7: Diode Emulation Setup through BBR# Capacitor

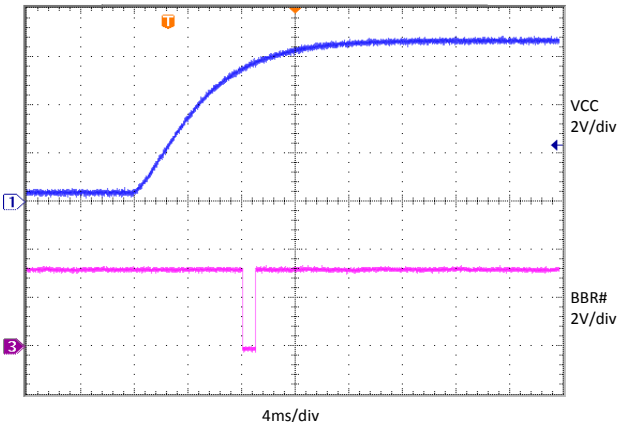

Figure 8: Diode Emulation Setup through BBR# Input

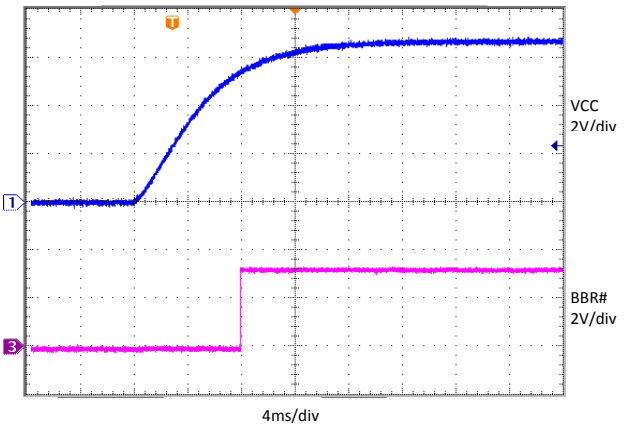

Figure 9: Diode Emulation Setup through BBR# Input

TRI-STATE GATE DRIVERS

The gate drivers can deliver up to 4A peak current and 6A sink current for low side driver. An adaptive non-overlap circuit monitors the voltage on the internal GATEH and GATEL pins to prevent MOSFET shoot-through current while minimizing body diode conduction. Tri-state operation prevents negative inductor current and negative output voltage during power-down. The gate driver incorporates pull down resistors on the MOSFET gates to prevent spurious turn-on of the output stage even when the IC is off and there is a high dV/dt event on the VIN supply rail. The gate drivers pull low if the supply voltages are below the normal operating range.

PHASE FAULT CIRCUIT AND THERMAL FLAG CIRCUIT (PHSFLT#)

The IR3535 phase fault circuit monitors the switch node with respect to VIN and ground to determine whether there is a defective MOSFET in the converter. The output of the PHSFLT# is high during normal operation and becomes low when there is a fault. The driver monitors the

MOSFETs it drives. If the switch node is a certain voltage lower than VIN when the PWM signal goes low or if the switch node is a certain voltage above ground when the PWM signal rises, this gives a possible fault signal. If there are a number of consecutive possible faults the phase fault signal is asserted.

Thermal flag circuit monitors the temperature of the IR3535 driver. If the temperature goes above 115°C (typical) the PHSFLT# pin is pulled low after a maximum delay of 100us. The PHSFLT# becomes high once the temperature drops below 95°C (typical).

The PHSFLT# pin can be pulled low by either the MOSFET fault circuit or the thermal flag circuit. The PHSFLT# signal could be used to turn off the AC/DC converter or blow a fuse to disconnect the DC/DC converter input from the supply.

If PHSFLT# is not used it can be floated or connected to LGND.

LOSSLESS AVERAGE INDUCTOR CURRENT SENSING

Inductor current can be sensed by connecting a series resistor and a capacitor network in parallel with the inductor and measuring the voltage across the capacitor, as shown in Figure 10.

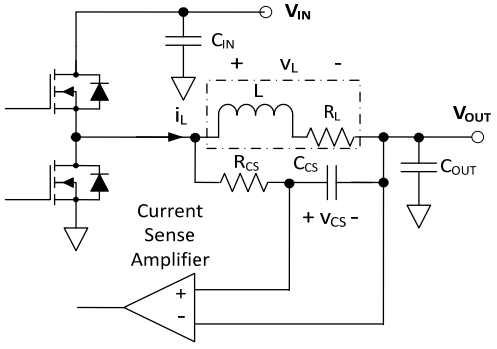

Figure 10: Inductor Current Sensing

The equation of the sensing network is as follows.

$$v_{CS}(s) = v_L(s)\frac{1}{1+sR_{CS}C_{CS}} = i_L(s)R_L\frac{1+s\frac{L}{R_L}}{1+sR_{CS}C_{CS}}$$

$$= i_L(s)R_L \quad when \quad L/R_L = R_{CS}C_{CS}$$

Usually the resistor R_{CS} and capacitor C_{CS} are chosen so that the time constant of R_{CS} and C_{CS} equals the time constant of the inductor which is the inductance L over the inductor DCR (R_L). If the two time constants match, the voltage across C_{CS} is proportional to the current through L, and the sense circuit can be treated as if only a sense resistor with the value of R_L was used. The mismatch of the time constants does not affect the measurement of inductor DC current, but affects the AC component of the inductor current.

The advantage of sensing the inductor current versus high side or low side sensing is that actual output current being delivered to the load is obtained rather than peak or sampled information about the switch currents. The output voltage can be positioned to meet a load line based on real time information. Except for a sense resistor in series with the inductor, this is the only sense method that can support a single cycle transient response. Other methods provide no information during either load increase (low side sensing) or load decrease (high side sensing).

CURRENT SENSE AMPLIFIER

A high speed differential current sense amplifier is located in the IR3535, as shown in Figure 4. Its gain is nominally 32.5, and the inductor DCR increase with temperature is not compensated inside the IR3535 and should be compensated in the voltage loop feedback path or inside the PWM controller. The current sense amplifier output IOUT is referenced to REFIN, which is usually connected to a reference voltage from the PWM controller.

The current sense amplifier can accept up to 25mV positive differential signal and up to -10mV negative differential signal before clipping. The output of the current sense amplifier is summed with the reference voltage at REFIN pin and sent to the PWM controller through IOUT pin. The current signal can be used for adaptive voltage positioning and over current protection. The input offset of this amplifier is calibrated to +/- 450uV in order to reduce the current sense error.

The input offset voltage is the primary source of error for the current signal. In order to obtain very accurate current signal, the current sense amplifier continuously calibrates itself. This calibration algorithm creates ripple on IOUT with a frequency of $f_{sw}/128$.

DESIGN PROCEDURES

INDUCTOR CURRENT SENSING CAPACITOR C_{CS} AND RESISTOR R_{CS}

The DC resistance of the inductor is utilized to sense the inductor current. Usually the resistor R_{CS} and capacitor C_{CS} in parallel with the inductor are chosen to match the time constant of the inductor, and therefore the voltage across the capacitor C_{CS} represents the inductor current.

Determine the inductance L and the inductor DC resistance R_L based on measurement or the datasheet specifications. Pre-select the capacitor C_{CS} and calculate R_{CS} as follows:

$$R_{CS} = \frac{L / R_L}{C_{CS}}$$

BOOTSTRAP CAPACITOR C_{BOOST}

A minimum of 0.22uF 0402 16Vdc capacitor is required for the bootstrap circuit. A high temperature 0.22uF or greater value 0603 capacitor is recommended.

VCC AND PVCC DECOUPLING CAPACITOR C_{VCC}

A 1uF ceramic decoupling capacitor is required at the VCC and PVCC pins.

BODY-BRAKING® FEATURE

The BBR# pin should be pulled up to VCC if the feature is not used by the PWM controller. Use of a small value resistor or a direct connection to VCC is recommended.

METAL AND COMPONENT PLACEMENT

- Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize *prevent* shorting.
- Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.
- Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper)
- Four 0.30mm diameter vias shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.
- No PCB traces should routed nor Vias placed under any of the 4 corners of the IC package. Doing so can cause the IC to raise up from the pcb resulting in poor solder joints to the IC leads.

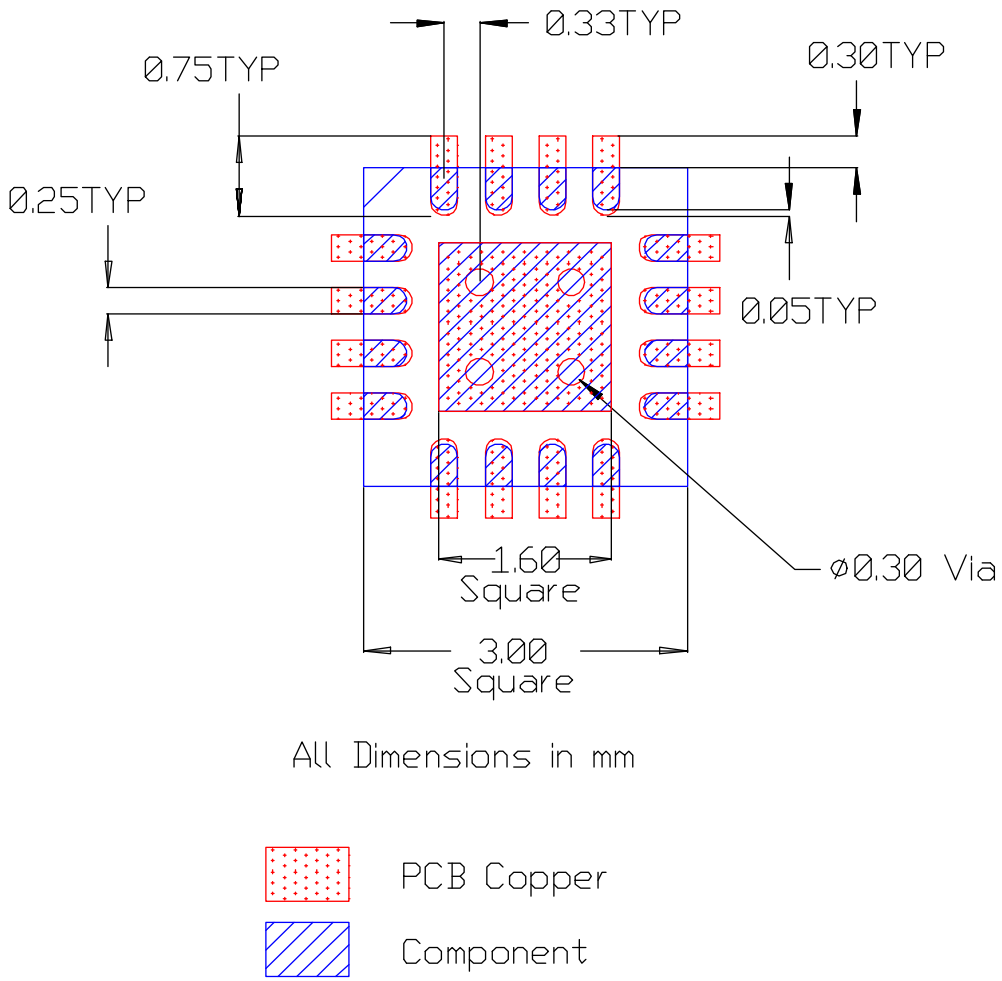

Figure 11: Metal and component placement

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SOLDER RESIST

- The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist miss-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.
- The minimum solder resist width is 0.13mm.
- At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.
- The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist miss-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.
- Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.
- The four vias in the land pad should be tented or plugged from bottom board side with solder resist.

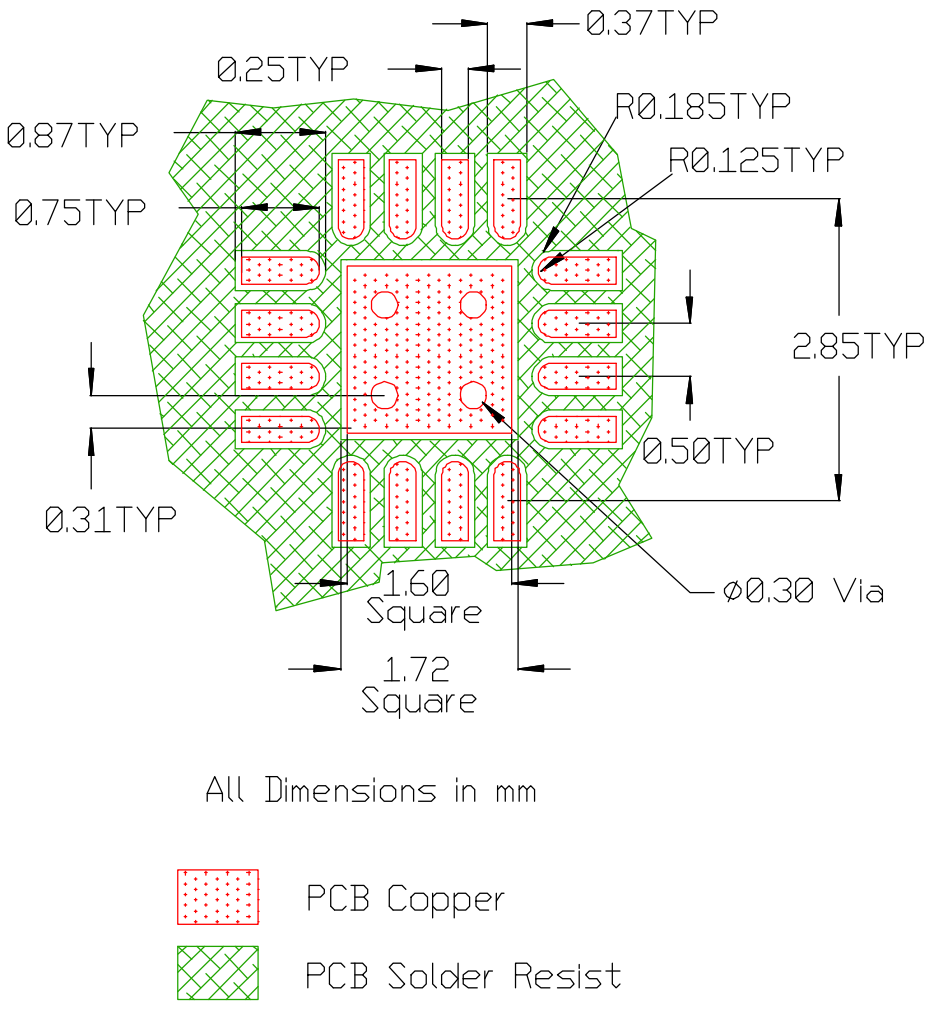

Figure 12: Solder resist

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STENCIL DESIGN

- The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.
- The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.
- The land pad aperture should be approximately 70% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.
- The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.

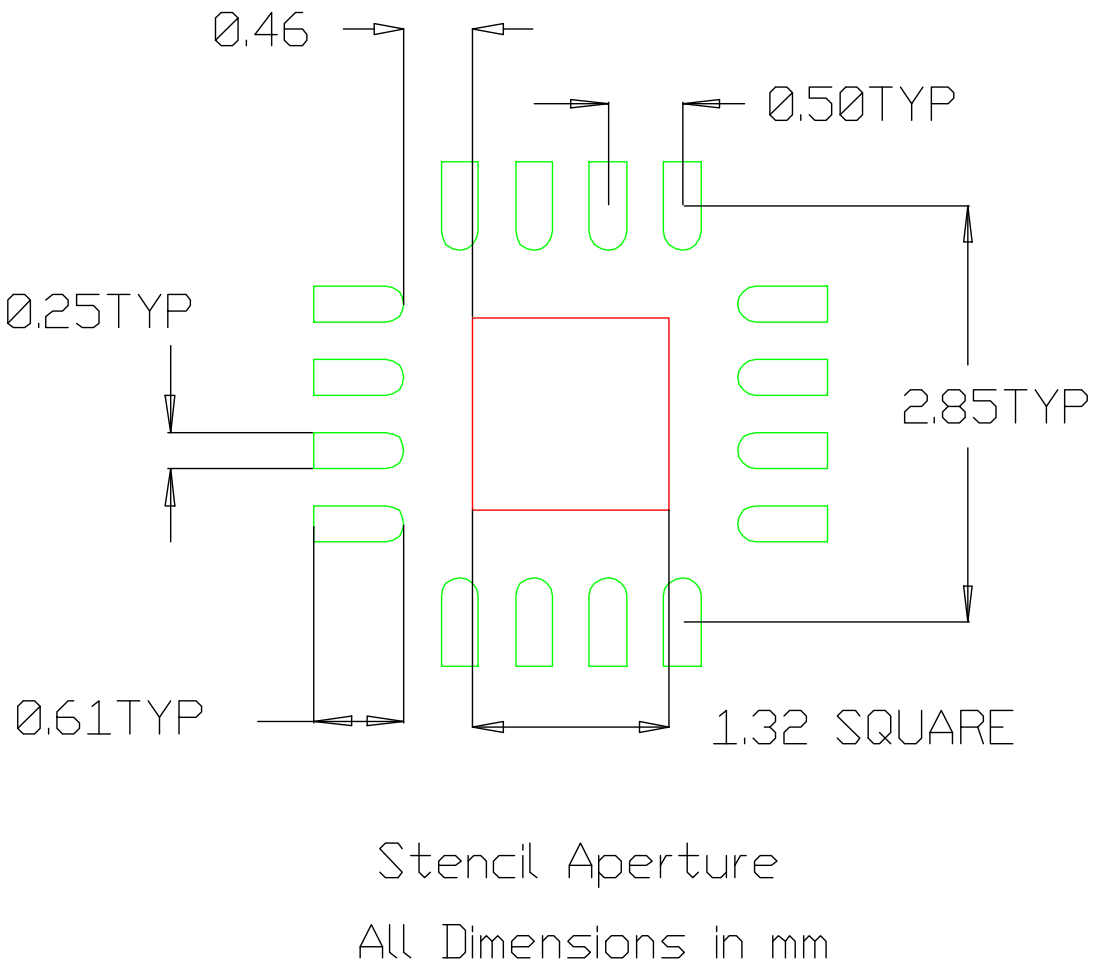

Figure 13: Stencil design

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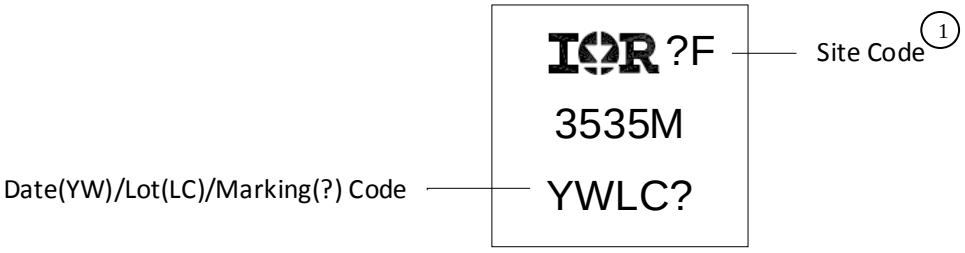
MARKING INFORMATION



NOTE (1) : Parts manufactured prior to date code 1304(YYWW) on the packing label will not have the "F" marking on line 1 of the part marking.

PACKAGE INFORMATION

16L MLPQ (3 x 3 mm Body) – θ_{JA} = 38°C/W, θ_{JC} = 3°C/W

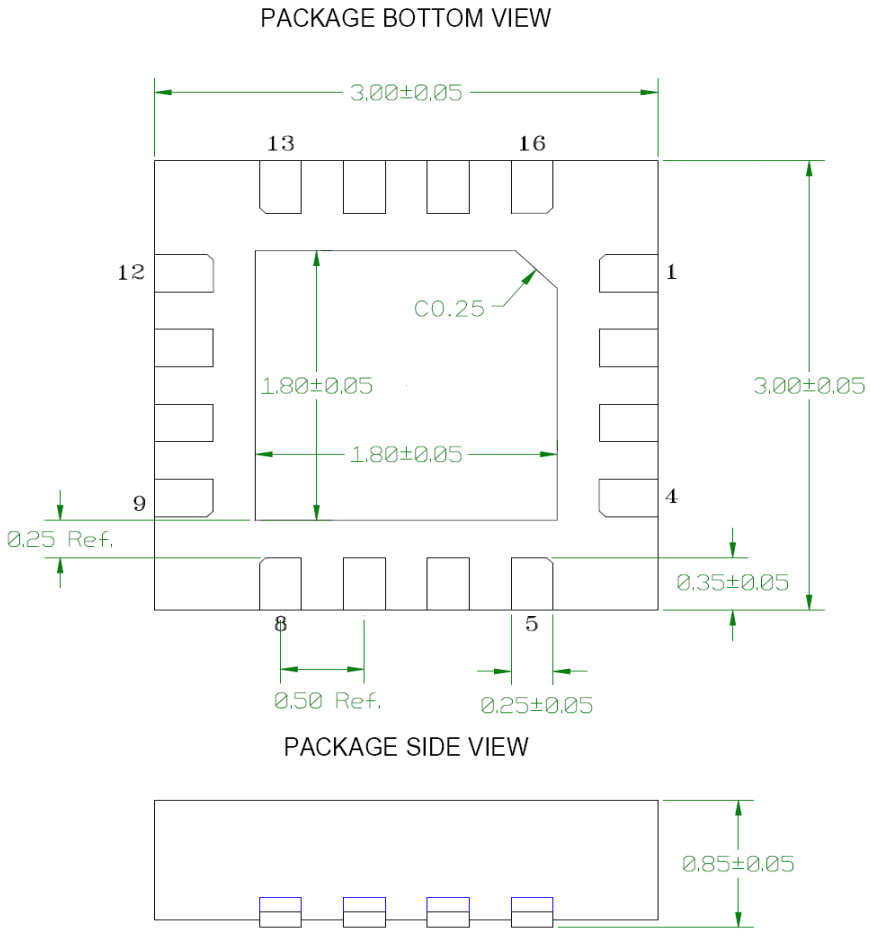


Figure 14: Package dimensions

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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