



3.3V CMOS 12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16270

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(o)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to $3.6V$, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels ($0.4\mu W$ typ. static)
- Rail-to-Rail output swing for increased noise margin
- Available in SSOP, TSSOP, and TVSOP packages

DRIVE FEATURES:

- High Output Drivers: $\pm 24mA$
- Suitable for heavy loads

APPLICATIONS:

- 3.3V high speed systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

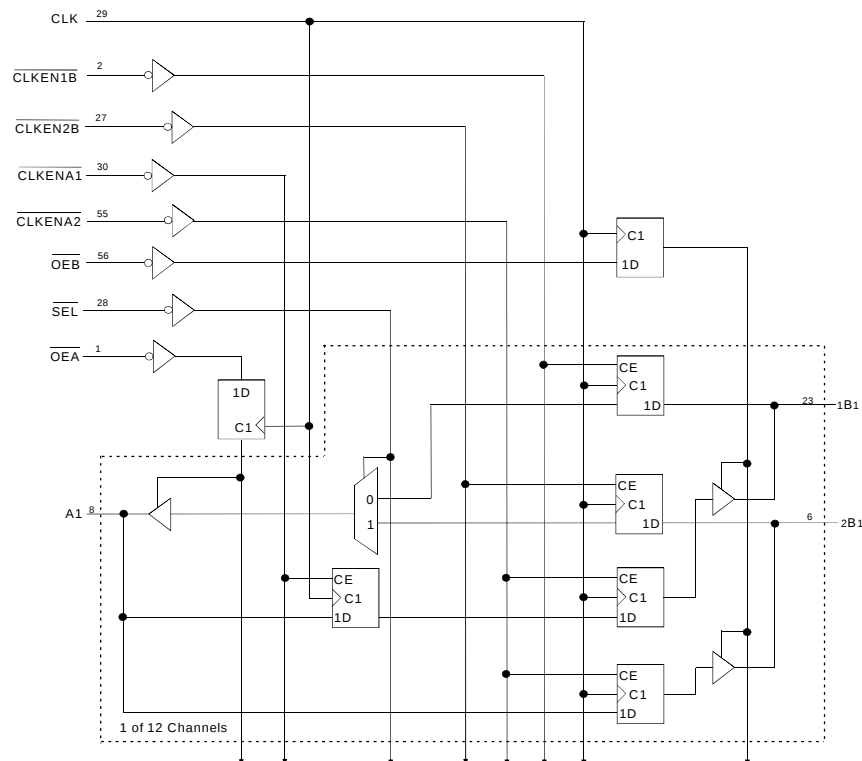
This registered bus exchanger is built using advanced dual metal CMOS technology. The ALVCH16270 is used in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

This device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{CLKEN}$) inputs are low. The select ($\overline{SEL}$) line selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the A-to-1B path, with a single storage register in the A-to-2B path. Proper control of the $\overline{CLKENA}$ input allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B-port. Data flow is controlled by the active-low output enables ($\overline{OE_A}$ and $\overline{OE_B}$). The control terminals are registered to synchronize the bus-direction changes with CLK.

The ALVCH16270 has been designed with a $\pm 24mA$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16270 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM

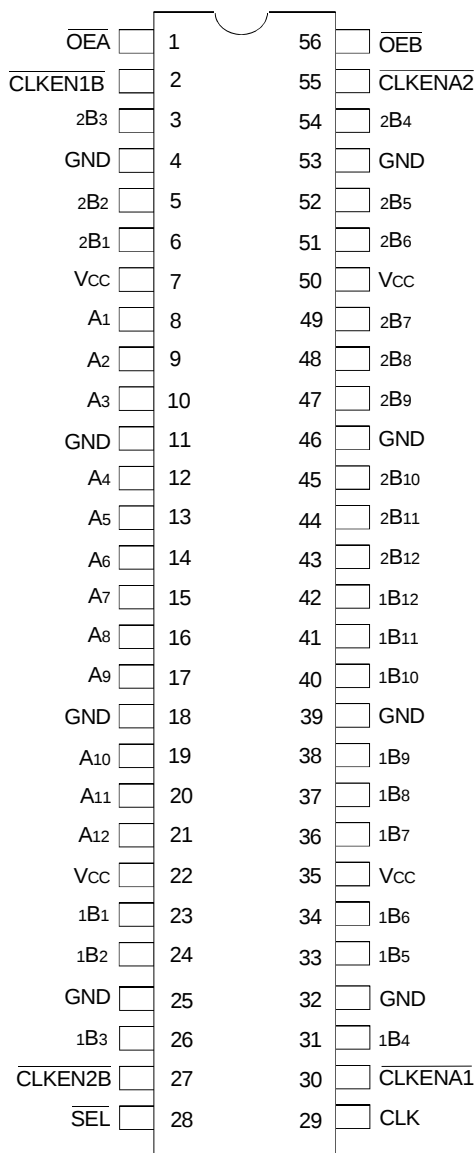


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INDUSTRIAL TEMPERATURE RANGE

AUGUST 1999

PIN CONFIGURATION



SSOP/ TSSOP/ TVSOP
TOP VIEW

A-TO-B STORAGE ($\overline{\text{OEB}} = \text{L}$ AND $\overline{\text{OEA}} = \text{H}$)

Inputs			Outputs		
CLKENA1	CLKENA2	CLK	Ax	1Bx	2Bx
L	H	↑	L	1B ₀ ⁽²⁾	2B ₀ ⁽²⁾
L	H	↑	H	1B ₀ ⁽²⁾	2B ₀ ⁽²⁾
L	L	↑	L	L ⁽³⁾	L
L	L	↑	H	H ⁽³⁾	H
H	L	↑	L	1B ₀ ⁽⁴⁾	L
H	L	↑	H	1B ₀ ⁽⁴⁾	H
H	H	X or ↑	X	1B ₀ ⁽²⁾	2B ₀ ⁽²⁾

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-50 to +50	mA
IIK	Continuous Clamp Current, Vi < 0 or Vi > Vcc	±50	mA
IOK	Continuous Clamp Current, Vo < 0	-50	mA
ICC ISS	Continuous Current through each Vcc or GND	±100	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- All terminals except Vcc.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	7	pF
COU	Output Capacitance	VOU = 0V	7	9	pF
CIO	I/O Port Capacitance	VIN = 0V	7	9	pF

NOTE:

- As applicable to the device type.

FUNCTION TABLES⁽¹⁾

OUTPUT ENABLE

Inputs			Outputs	
CLK	$\overline{\text{OEA}}$	$\overline{\text{OEB}}$	Ax	1Bx, 2Bx
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

B-TO-A STORAGE ($\overline{\text{OEA}} = \text{L}$ AND $\overline{\text{OEB}} = \text{H}$)

Inputs						Outputs
CLKENB1	CLKENB2	CLK	SEL	1Bx	2Bx	Ax
H	X	X	H	X	X	A ₀ ⁽²⁾
X	H	X	L	X	X	A ₀ ⁽²⁾
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition
- Output level before the indicated steady-state input conditions were established.
- Two CLK edges are needed to propagate data.
- Data present at the output of the first register.

PIN DESCRIPTION

Pin Names	I/O	Description
Ax(1:12)	I/O	Bidirectional Data Port A. Usually connected to the CPU's Address/Data bus. ⁽¹⁾
1Bx(1:12)	I/O	Bidirectional Data Port 1B. Usually connected to the even path or even bank of memory. ⁽¹⁾
2Bx(1:12)	I/O	Bidirectional Data Port 2B. Usually connected to the odd path or odd bank of memory. ⁽¹⁾
CLK	I	Clock Input
$\overline{\text{CLKENA1}}$	I	Clock Enable Input for the A-1B Register. If $\overline{\text{CLKENA1}}$ is LOW during the rising edge of CLK, data will be clocked into register A-1B (Active LOW).
$\overline{\text{CLKENA2}}$	I	Clock Enable Input for the A-2B Register. If $\overline{\text{CLKENA2}}$ is LOW during the rising edge of CLK, data will be clocked into register A-2B (Active LOW).
$\overline{\text{CLKEN1B}}$	I	Clock Enable Input for the 1B-A Register. If $\overline{\text{CLKEN1B}}$ is LOW during the rising edge of CLK, data will be clocked into register 1B-A (Active LOW).
$\overline{\text{CLKEN2B}}$	I	Clock Enable Input for the 2B-A Register. If $\overline{\text{CLKEN2B}}$ is LOW during the rising edge of CLK, data will be clocked into register 2B-A (Active LOW).
$\overline{\text{SEL}}$	I	1B or 2B Port Selection. When HIGH during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 1B Port to A Port. When LOW during the rising edge of CLK, $\overline{\text{SEL}}$ enables data transfer from 2B Port to A Port.
$\overline{\text{OE A}}$	I	Synchronous Output Enable for A Port (Active LOW)
$\overline{\text{OE B}}$	I	Synchronous Output Enable for B Port (Active LOW)

NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	±5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	±5	μA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	±10	μA
			V _O = GND	—	—	±10	
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CC} I _{CC} I _{CC}	Quiescent Power Supply Current	V _{CC} = 3.6V V _{IN} = GND or V _{CC}		—	0.1	40	μA
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 3V	V _I = 2V V _I = 0.8V	-75 75	— —	— —	μA
IBHH IBHL	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V V _I = 0.7V	-45 45	— —	— —	μA
IBHHO IBHLO	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	±500	μA

NOTES:

1. Pins with Bus-Hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3V		2.4	—	
		V _{CC} = 3V	I _{OH} = -24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz	87	120	pF
CPD	Power Dissipation Capacitance Outputs disabled		80.5	118	

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay CLK to xBx	1.5	5.9	—	5.8	1.1	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to Ax	1.2	5.4	—	5.4	1	4.7	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{SEL}}$ to Ax	1.4	6.2	—	6.4	1	5.5	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to xBx	1.5	7	—	6.8	1	6	ns
t _{PZH} t _{PZL}	Output Enable Time CLK to Ax	1.5	7	—	6.8	1	6	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to xBx	1.9	7.2	—	6.5	1.1	5.8	ns
t _{PHZ} t _{PLZ}	Output Disable Time CLK to Ax	1.9	7.2	—	6.5	1.1	5.8	ns
t _{SU}	Set-up Time, Ax data before CLK↑	4.1	—	3.8	—	3.1	—	ns
t _{SU}	Set-up Time, Bx data before CLK↑	0.9	—	1.2	—	0.9	—	ns
t _{SU}	Set-up Time, $\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK↑	3.5	—	3.2	—	2.7	—	ns
t _{SU}	Set-up Time, $\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ before CLK↑	3.4	—	3	—	2.6	—	ns
t _{SU}	Set-up Time, $\overline{\text{OEB}}$ or $\overline{\text{OEA}}$ before CLK↑	4.4	—	3.9	—	3.2	—	ns
t _H	Hold Time, Ax data after CLK↑	0	—	0	—	0.2	—	ns
t _H	Hold Time, Bx data after CLK↑	1.4	—	1	—	1.7	—	ns
t _H	Hold Time, $\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK↑	0	—	0.1	—	0.3	—	ns
t _H	Hold Time, $\overline{\text{CLKEN1B}}$ or $\overline{\text{CLKEN2B}}$ after CLK↑	0	—	0	—	0.6	—	ns
t _H	Hold Time, $\overline{\text{OEB}}$ or $\overline{\text{OEA}}$ after CLK↑	0	—	0	—	0.1	—	ns
t _w	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{sk(O)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

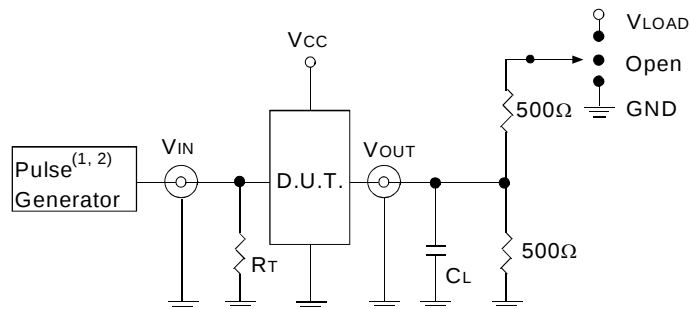
NOTES:

1. See TEST CIRCUITS AND WAVEFORMS. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} ⁽¹⁾ =3.3V±0.3V	V _{CC} ⁽¹⁾ =2.7V	V _{CC} ⁽²⁾ =2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF



Test Circuit for All Outputs

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

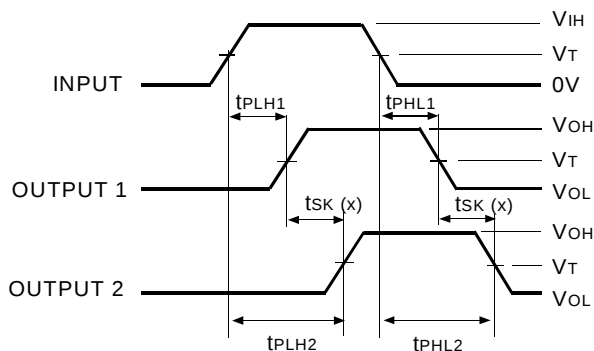
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2.5ns; t_r ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_r ≤ 2ns; t_r ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other Tests	Open

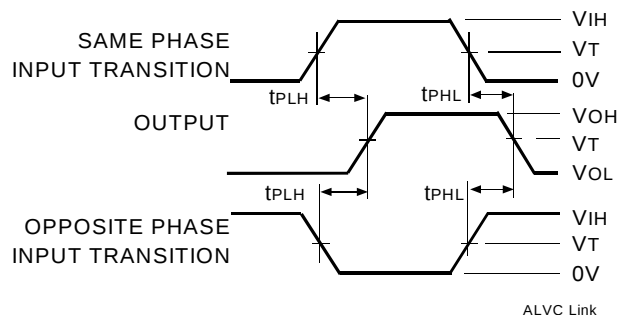


$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

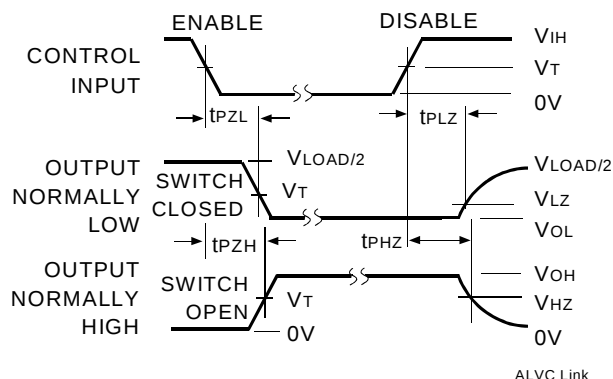
Output Skew - t_{SK}(x)

NOTES:

1. For t_{SK}(0) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.



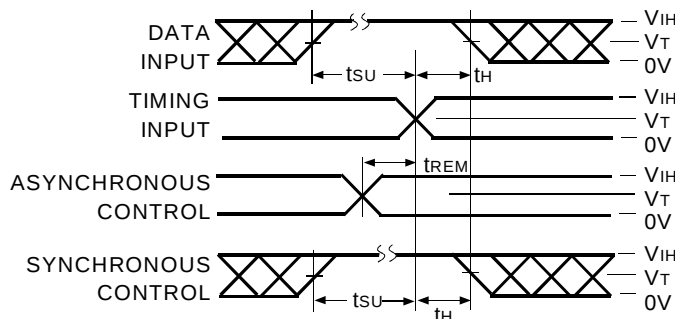
Propagation Delay



Enable and Disable Times

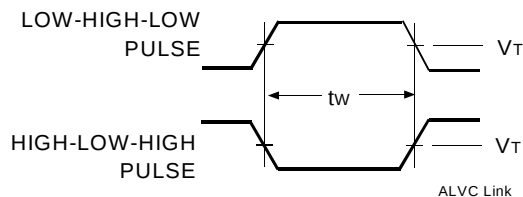
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.



ALVC Link

Set-up, Hold, and Release Times



Pulse Width

IDT	XX	ALVC	X	XX	XXX	XX
Temp. Range		Bus-Hold		Family	Device Type	Package

PV	Shrink Small Outline Package
PA	Thin Shrink Small Outline Package
PF	Thin Very Small Outline Package
270	12-Bit to 24-Bit Registered Bus Exchanger with 3-State Outputs
16	Double-Density, $\pm 24\text{mA}$
H	Bus-hold
74	-40°C to $+85^{\circ}\text{C}$



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