

## 40ns、低功耗、推挽输出比较器

 查询样品: [TLV3201](#), [TLV3202](#)

### 特性

- 低传播延迟: **40ns**
- 低静态电流  
每通道 **40 $\mu$ A**
- 输入共模扩展范围扩展到任一电源轨之上 **200mV**
- 低输入偏移电压: **1mV**
- 推挽输出
- 电源范围: **+2.7V 至 +5.5V**
- 工业温度范围:  
**-40°C 至 +125°C**
- 小型封装:  
**SC70-5**、小外形尺寸晶体管封装 (**SOT**)**23-5**、小外形尺寸集成电路封装 (**SOIC**)**-8**、微型小外形尺寸封装 (**MSOP**)**-8**

### 应用范围

- 检测设备
- 测试和测量
- 高速采样系统
- 电信
- 便携式通信

### 说明

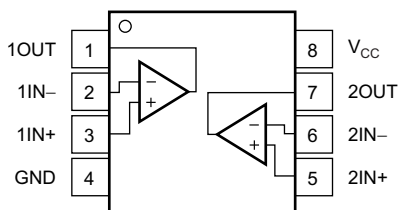
TLV3201 和 TLV3202 是单通道和双通道比较器, 此比较器能够在极小型封装内提供高速 (40ns) 和低功耗 (40 $\mu$ A) 的最终组合, 此封装具有诸如轨到轨输入、低偏移电压 (1mV)、和高输出驱动电流等特性。在对响应时间要求严格的多种应用中也可轻松执行此器件。

TLV320x 系列产品可提供单通道 (TLV3201) 和双通道 (TLV3202) 版本, 这两个版本的器件都带有推挽输出。TLV3201 采用 SOT23-5 和 SC70-5 封装。TLV3202 采用 SOIC-8 和 MSOP-8 封装。所有器件可在扩展的工业温度范围, 即 -40°C 至 +125°C, 内运行。

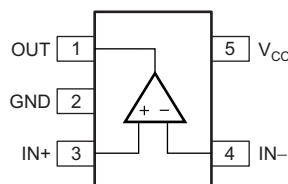
### 相关产品

器件	说明
TLV3011	1.5mm x 1.5mm 微型封装内的 5 $\mu$ A (最大值) 开漏电流、具有集成电压基准的 1.8V 至 5.5V 电压
TLV3012	微型封装内的 5 $\mu$ A (最大值) 推挽电流、具有集成电压基准的 1.8V 至 5.5V 电压
TLV3501	微型封装内的 4.5ns、轨到轨、推挽比较器
LMV7235	带有开漏输出的 75ns, 65 $\mu$ A, 2.7V 至 5.5V, 轨到轨输入比较器
REF3333	30ppm/°C 漂移、3.9 $\mu$ A、SOT23-3、SC70-3 电压基准

**D AND DGK PACKAGES  
SOIC-8 AND MSOP-8  
(TOP VIEW)**



**DCK AND DBV PACKAGES  
SC70-5 AND SOT23-5  
(TOP VIEW)**



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD <sup>(2)</sup>	PACKAGE DESIGNATOR	PACKAGE MARKING	ORDERING NUMBER
TLV3201	SOT23-5	DBV	RAI	TLV3201AIDBV
	SC70-5	DCK	SDP	TLV3201AIDCK
TLV3202	SOIC-8	D	TL3202	TLV3202AID
	MSOP-8	DGK	VUDC	TLV3202AIDGK

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and printed circuit board (PCB) design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage		7	V
Signal input terminals	Voltage <sup>(2)</sup>	-0.5 to (V <sub>CC</sub> ) + 0.5	V
	Current <sup>(2)</sup>	±10	mA
Output short circuit <sup>(3)</sup>		100	mA
Operating temperature range		-55 to +125	°C
Storage temperature range, T <sub>stg</sub>		-65 to +150	°C
Junction temperature, T <sub>J</sub>		+150	°C
Electrostatic discharge (ESD) ratings TLV3201	Human body model (HBM)	2000	V
Electrostatic discharge (ESD) ratings TLV3202	Human body model (HBM)	1000	V

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal.
- (3) Short-circuit to ground.

**ELECTRICAL CHARACTERISTICS:  $V_{CC} = 5.0\text{ V}$** 

At  $T_A = +25^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{IO}$	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			6	mV
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	10	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$ , $V_{CC} = 2.5\text{ V}$ to $5.5\text{ V}$	65	85		dB
	Input hysteresis			1.2		mV
<b>INPUT BIAS CURRENT</b>						
$I_{IB}$	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			5	nA
$I_{IO}$	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2.5	nA
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V_{EE}) - 0.2$		$(V_{CC}) + 0.2$	V
CMRR	Common-mode rejection ratio	$-0.2\text{ V} < V_{CM} < 5.2\text{ V}$	60	70		dB
<b>INPUT IMPEDANCE</b>						
	Common-mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
	Differential			$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
<b>SWITCHING CHARACTERISTICS</b>						
$t_{pd}$	Propagation delay time	Low to high	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	47	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	43	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
		High to low	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	45	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	42	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
	Propagation delay skew	Input overdrive = 20mV, $C_L = 15\text{ pF}$	2			ns
	Propagation delay matching (TLV3202)	High to low, Low to High	Input overdrive = 20 mV, $C_L = 15\text{ pF}$		5	ns
$t_r$	Rise time	10% to 90%		2.9		ns
$t_f$	Fall time	10% to 90%		3.7		ns
<b>OUTPUT</b>						
$V_{OL}$	Voltage output swing	From lower rail	$I_{SINK} = 4\text{ mA}$	175	190	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		225	mV
From upper rail		$I_{SOURCE} = 4\text{ mA}$	120	140	mV	
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		170	mV	
$I_{SC}$	Short-circuit current (per comparator)	Sinking	$I_{SC}$ sinking	40	48	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
		Sourcing	$I_{SC}$ sourcing	52	60	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
<b>POWER SUPPLY</b>						
$V_{CC}$	Specified voltage		2.7		5.5	V
$I_Q$	Quiescent current			40	50	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			65	$\mu\text{A}$
<b>TEMPERATURE</b>						
	Specified range		-40		+125	$^\circ\text{C}$
	Storage range		-65		+150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS:  $V_{CC} = 2.7\text{ V}$**

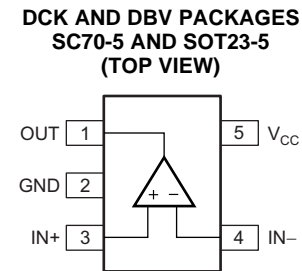
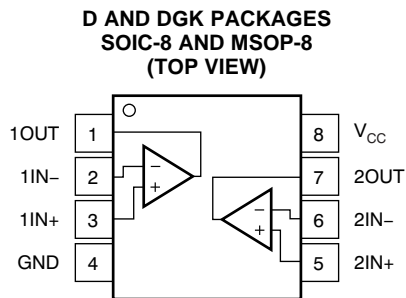
At  $T_A = +25^\circ\text{C}$  and  $V_{CC} = 2.7\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>						
$V_{IO}$	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			6	mV
$dV_{OS}/dT$	Input offset voltage drift	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		1	10	$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$ , $V_{CC} = 2.5\text{ V}$ to $5.5\text{ V}$	65	85		dB
	Input hysteresis			1.2		mV
<b>INPUT BIAS CURRENT</b>						
$I_{IB}$	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			5	nA
$I_{IO}$	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			2.5	nA
<b>INPUT VOLTAGE RANGE</b>						
$V_{CM}$	Common-mode voltage range	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	$(V_{EE}) - 0.2$		$(V_{CC}) + 0.2$	V
CMRR	Common-mode rejection ratio	$-0.2\text{ V} < V_{CM} < 2.9\text{ V}$	56	68		dB
<b>INPUT IMPEDANCE</b>						
	Common-mode			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$
	Differential			$10^{13} \parallel 4$		$\Omega \parallel \text{pF}$
<b>SWITCHING CHARACTERISTICS</b>						
$t_{pd}$	Propagation delay time	Low to high	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	47	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	42	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
		High to low	Input overdrive = 20 mV, $C_L = 15\text{ pF}$	40	50	ns
			Input overdrive = 100 mV, $C_L = 15\text{ pF}$	38	50	ns
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		55	ns
	Propagation delay skew	Input overdrive = 20mV, $C_L = 15\text{ pF}$	2			ns
	Propagation delay matching (TLV3202)	High to low, Low to High	Input overdrive = 20 mV, $C_L = 15\text{ pF}$		5	ns
$t_r$	Rise time	10% to 90%		4.8		ns
$t_f$	Fall time	10% to 90%		5.2		ns
<b>OUTPUT</b>						
$V_{OL}$	Voltage output swing	From lower rail	$I_{SINK} = 4\text{ mA}$	230	260	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			325
$V_{OH}$		From upper rail	$I_{SOURCE} = 4\text{ mA}$	210	250	mV
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			350
$I_{SC}$	Short-circuit current (per comparator)	$I_{SC}$ sinking		13	19	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
		$I_{SC}$ sourcing		15	21	mA
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		See Typical Curve	mA
<b>POWER SUPPLY</b>						
$V_{CC}$	Specified voltage		2.7		5.5	V
$I_Q$	Quiescent current			36	46	$\mu\text{A}$
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			60	$\mu\text{A}$
<b>TEMPERATURE</b>						
	Specified range		-40		+125	$^\circ\text{C}$
	Storage range		-65		+150	$^\circ\text{C}$

**THERMAL INFORMATION**

THERMAL METRIC <sup>(1)</sup>		TLV3201		TLV3202		UNITS
		DBV (SOT23)	DCK (SC70)	D (SOIC)	DGK (MSOP)	
		5 PINS	5 PINS	8 PINS	8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	237.8	281.9	146.3	201.9	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	108.7	97.6	97.2	92.5	
$\theta_{JB}$	Junction-to-board thermal resistance	64.1	68.3	84.2	123.3	
$\Psi_{JT}$	Junction-to-top characterization parameter	12.1	2.6	45.5	23.0	
$\Psi_{JB}$	Junction-to-board characterization parameter	63.3	67.3	83.7	121.6	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) 有关传统和全新热度的更多信息，请参阅 *IC 封装热量度量* 应用报告 (文献号：SPRA953)。

**PIN CONFIGURATIONS**

**PIN DESCRIPTIONS: D, DGK**

NAME	NO.	DESCRIPTION
1IN-	2	Negative input, comparator 1
1IN+	3	Positive input, comparator 1
1OUT	1	Output, comparator 1
2IN-	6	Negative input, comparator 2
2IN+	5	Positive input, comparator 2
2OUT	7	Output, comparator 2
GND	4	Negative supply, ground
V <sub>CC</sub>	8	Positive supply

**PIN DESCRIPTIONS: DCK, DBV**

NAME	NO.	DESCRIPTION
OUT	1	Output
GND	2	Negative supply, ground
IN+	3	Positive input
V <sub>CC</sub>	5	Positive supply
IN-	4	Negative input

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$ , and input overdrive ( $V_{OD}$ ) = 20 mV, unless otherwise noted.

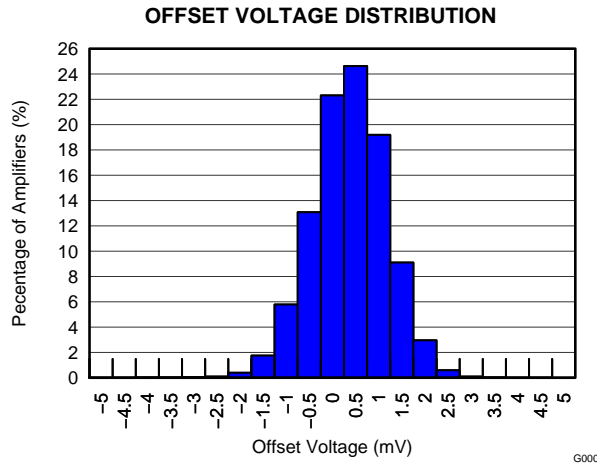


Figure 1.

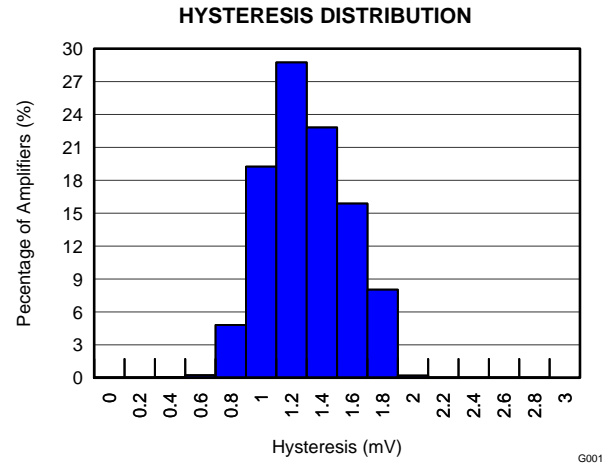


Figure 2.

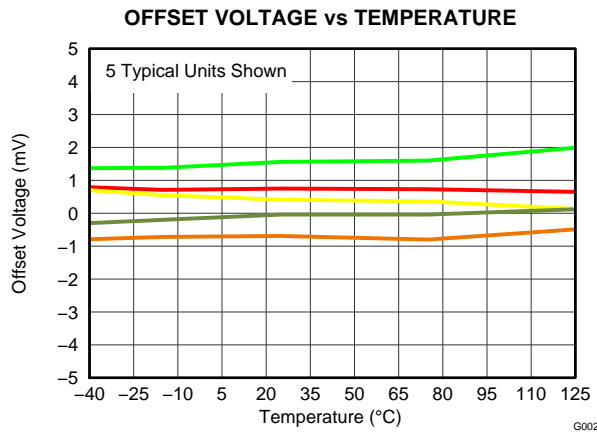


Figure 3.

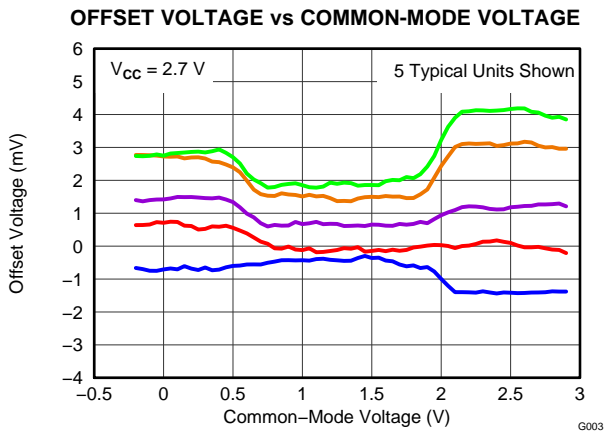


Figure 4.

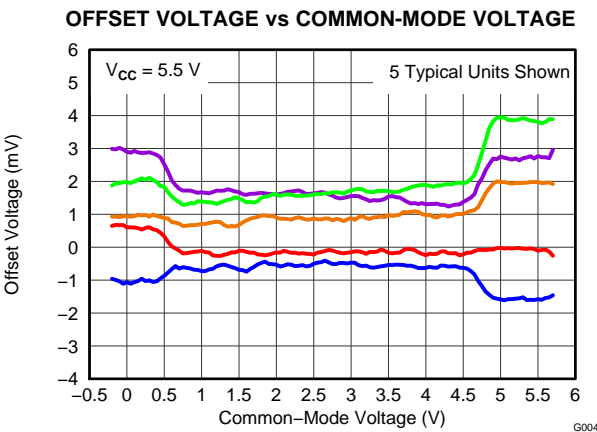


Figure 5.

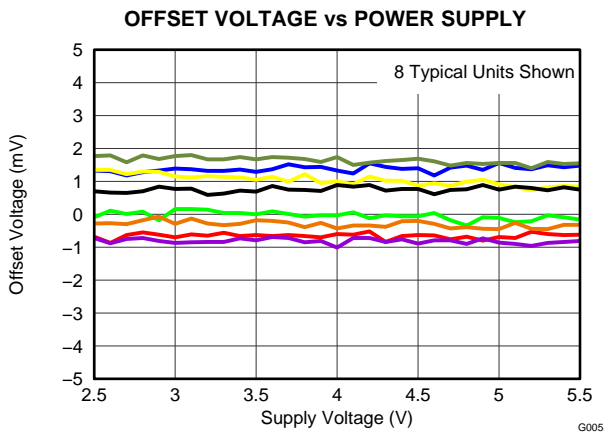


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$ , and input overdrive ( $V_{OD}$ ) = 20 mV, unless otherwise noted.

**COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE**

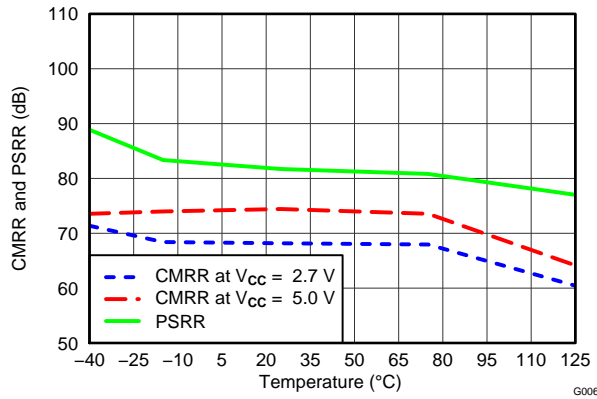


Figure 7.

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE**

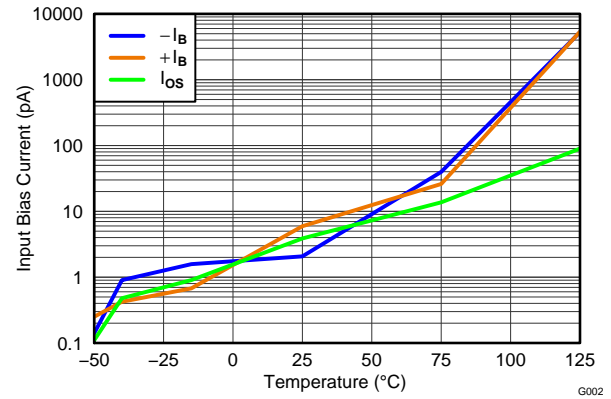


Figure 8.

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE**

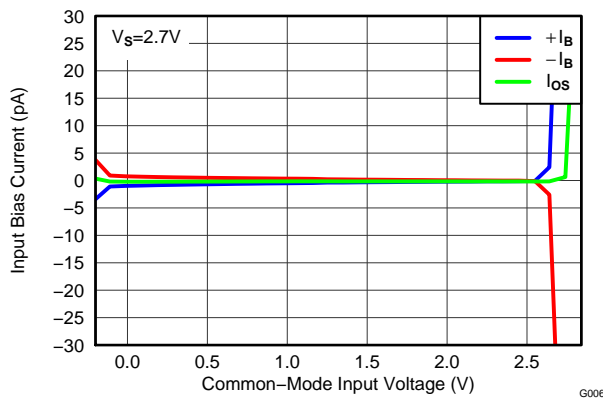


Figure 9.

**INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE INPUT VOLTAGE**

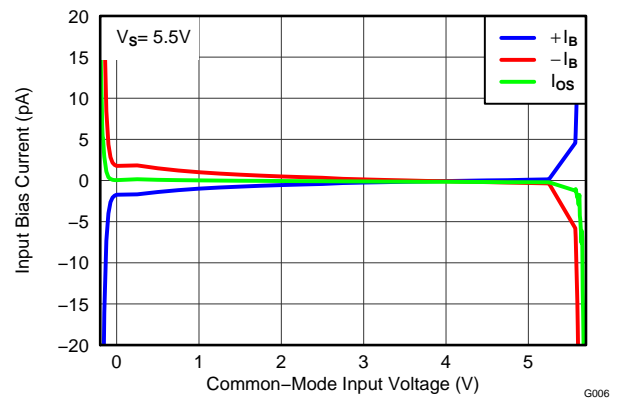


Figure 10.

**QUIESCENT CURRENT DISTRIBUTION**

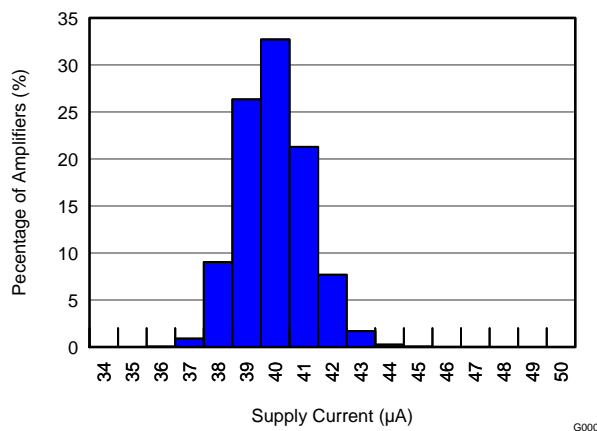


Figure 11.

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

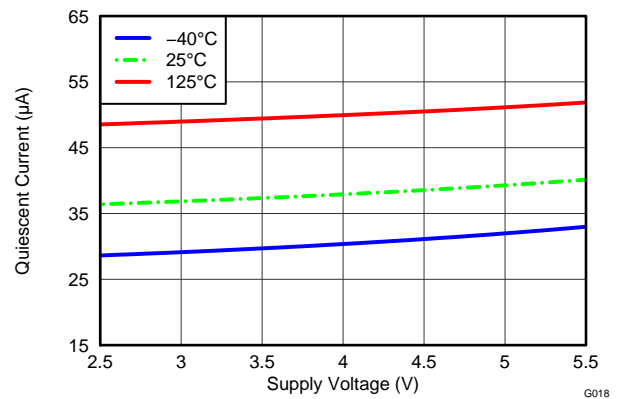


Figure 12.

### TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$ , and input overdrive ( $V_{OD}$ ) = 20 mV, unless otherwise noted.

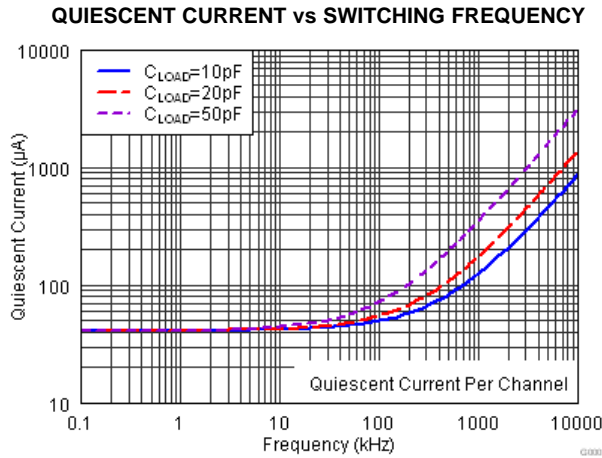


Figure 13.

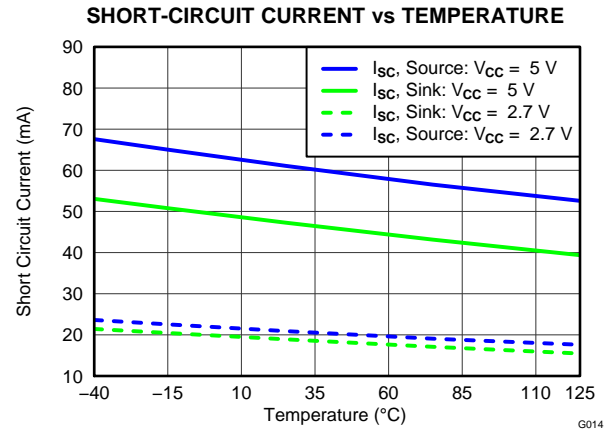


Figure 14.

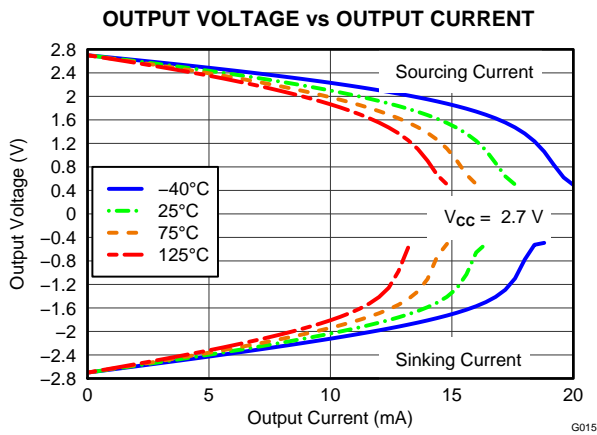


Figure 15.

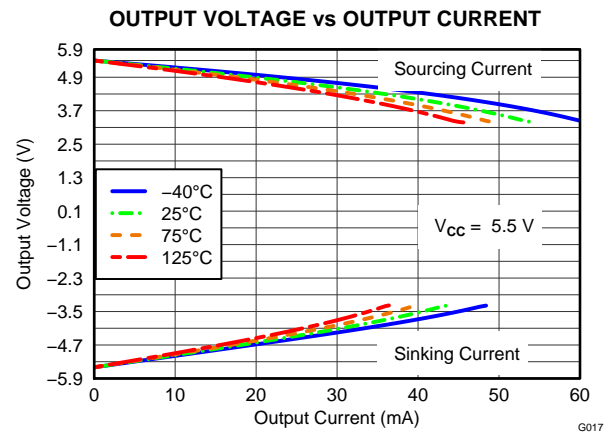


Figure 16.

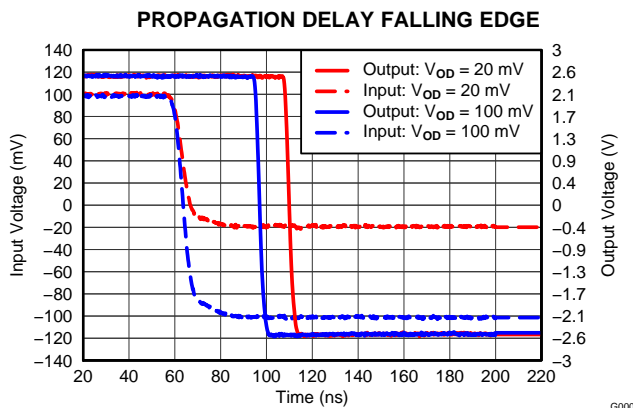


Figure 17.

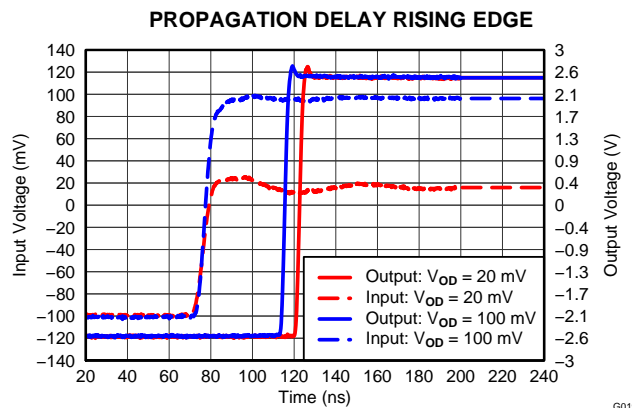


Figure 18.



### TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{ V}$ , and input overdrive ( $V_{OD}$ ) = 20 mV, unless otherwise noted.

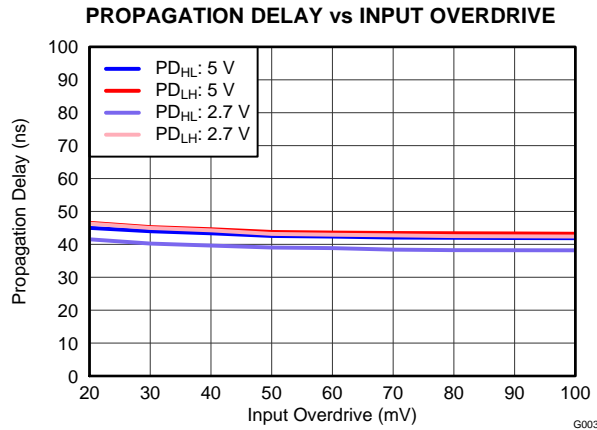


Figure 19.

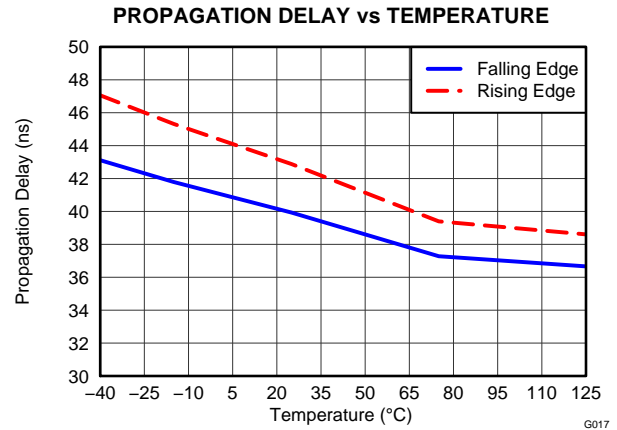


Figure 20.

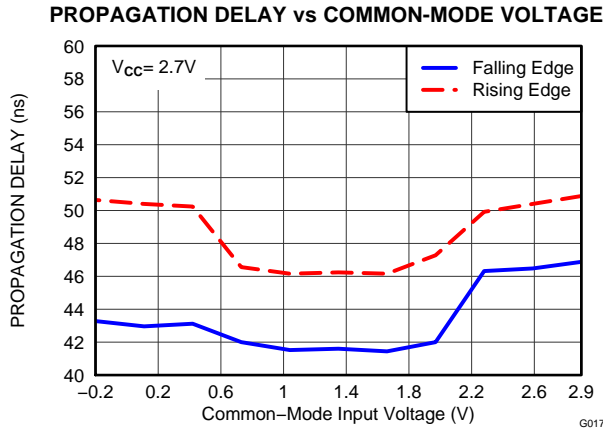


Figure 21.

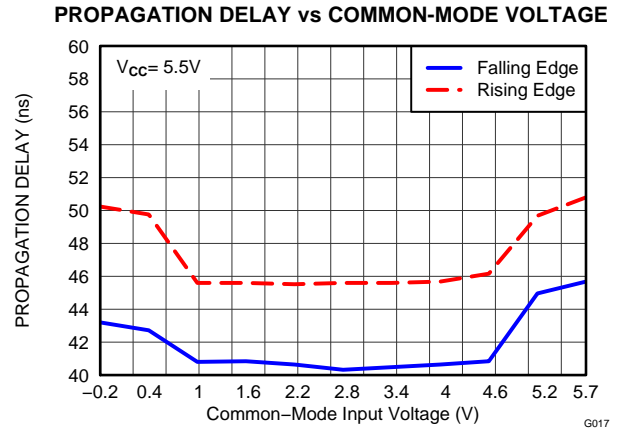


Figure 22.

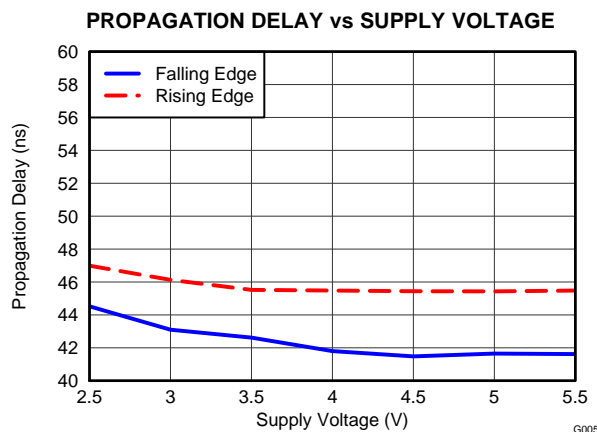


Figure 23.

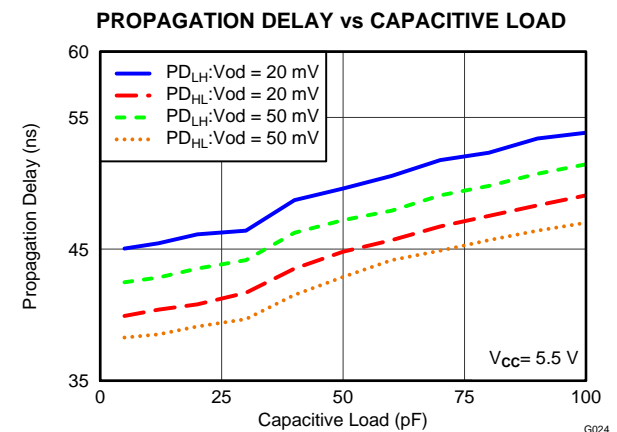


Figure 24.

## APPLICATION INFORMATION

The TLV3201 and TLV3202 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40  $\mu$ A of supply current. This combination of fast response time and minimal power consumption make the TLV3201 and TLV3202 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

### COMPARATOR INPUTS

The TLV3201 and TLV3202 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The TLV3201 and TLV3202 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the TLV320x response when input voltages exceed the supply, resulting in no phase inversion.

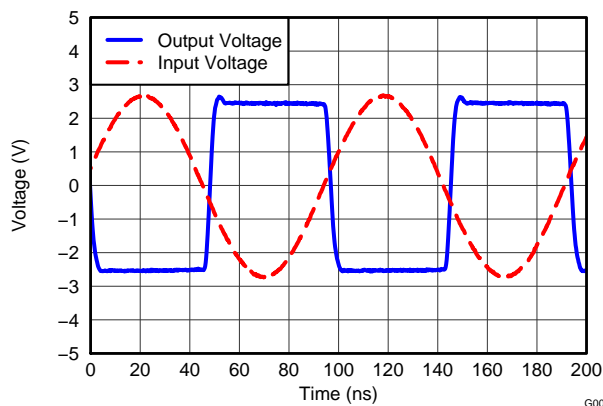


Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Prop Delay Included)

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-k $\Omega$  series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed  $V_{CC}$  beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage should be avoided to prevent damage to the input stage.

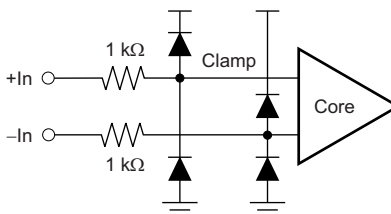
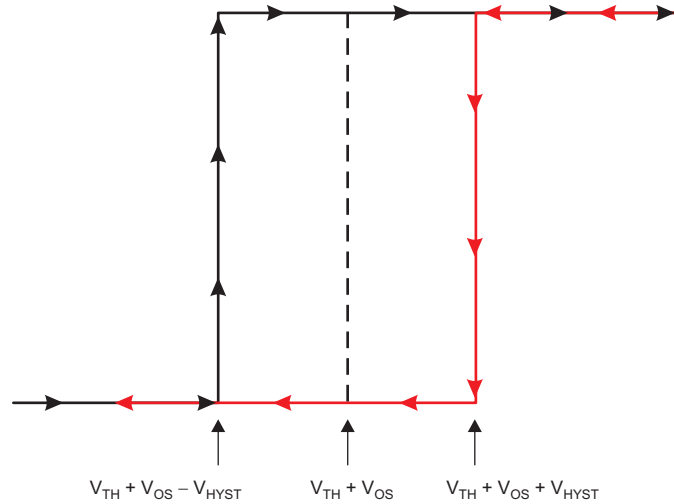


Figure 26. TLV3201 equivalent input structure

## EXTERNAL HYSTERESIS

The TLV3201 and TLV3202 have a hysteresis transfer curve (shown in [Figure 27](#)) that is a function of the following three components:

- $V_{TH}$ : the actual set voltage or threshold trip voltage
- $V_{OS}$ : the internal offset voltage between  $V_{IN+}$  and  $V_{IN-}$ . This voltage is added to  $V_{TH}$  to form the actual trip point at which the comparator must respond in order to change output states.
- $V_{HYST}$ : internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.



**Figure 27. TLV3201 Hysteresis Transfer Curve**

### Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage ( $V_{CC}$ ), as shown in [Figure 28](#). When  $V_{IN}$  at the inverting input is less than  $V_A$ , the output voltage is high (for simplicity assume  $V_O$  switches as high as  $V_{CC}$ ). The three network resistors can be represented as  $R1 \parallel R3$  in series with  $R2$ . The lower input trip voltage ( $V_{A1}$ ) is defined by [Equation 1](#):

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \quad (1)$$

When  $V_{IN}$  is greater than [ $V_A \times (V_{IN} > V_A)$ ], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as  $R2 \parallel R3$  in series with  $R1$ . The upper trip voltage ( $V_{A2}$ ) is defined by [Equation 2](#):

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \quad (2)$$

The total hysteresis provided by the network is defined by [Equation 3](#):

$$\Delta V_A = V_{A1} - V_{A2} \quad (3)$$

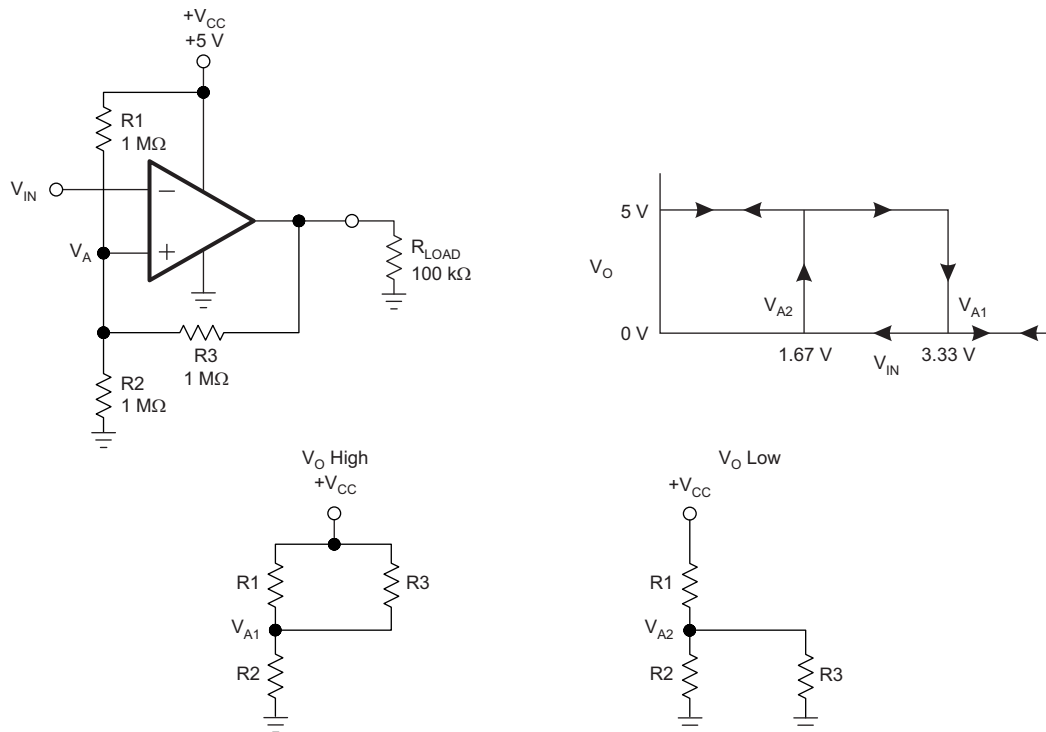


Figure 28. TLV3201 in Inverting Configuration with Hysteresis

### Noninverting Comparator with Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29, and a voltage reference ( $V_{REF}$ ) at the inverting input. When  $V_{IN}$  is low, the output is also low. For the output to switch from low to high,  $V_{IN}$  must rise up to  $V_{IN1}$ .  $V_{IN1}$  is calculated by Equation 4:

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \quad (4)$$

When  $V_{IN}$  is high, the output is also high. In order for the comparator to switch back to a low state,  $V_{IN}$  must equal  $V_{REF}$  before  $V_A$  is again equal to  $V_{REF}$ .  $V_{IN}$  can be calculated by Equation 5:

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2} \quad (5)$$

The hysteresis of this circuit is the difference between  $V_{IN1}$  and  $V_{IN2}$ , as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \quad (6)$$

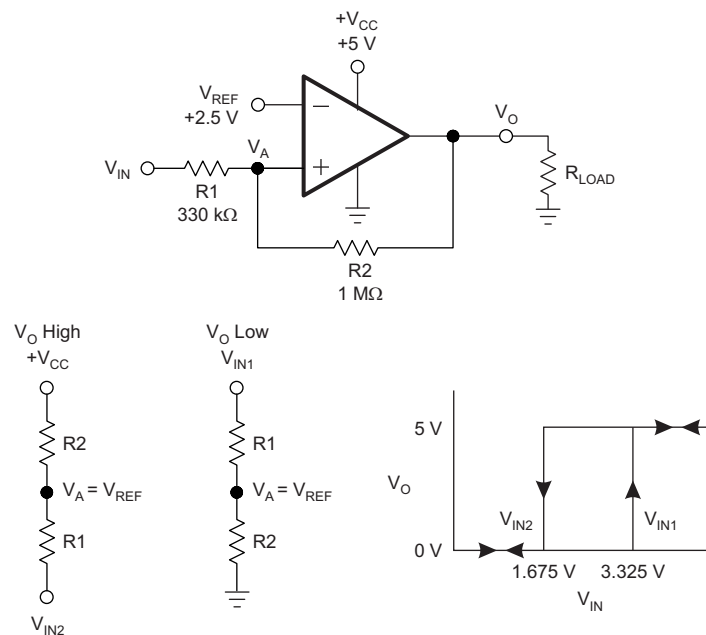


Figure 29. TLV3201 in Noninverting Configuration with Hysteresis

### CAPACITIVE LOADS

The TLV3201 and TLV3202 feature a push-pull output. When the output switches, there is a direct path between  $V_{CC}$  and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40  $\mu$ A, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201 and TLV3202 maintain specified propagation delay (see the Typical Characteristics), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

## CIRCUIT LAYOUT

The TLV3201 and TLV3202 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, the following layout guidelines should be maintained:

1. Use a printed circuit board (PCB) with a good, unbroken low-inductance ground plane.
2. Place a decoupling capacitor (0.1- $\mu\text{F}$  ceramic, surface-mount capacitor) as close as possible to  $V_{CC}$ .
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
4. Solder the device directly to the PCB rather than using a socket.
5. For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
6. The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

## APPLICATIONS CIRCUITS

One of the benefits of ac coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the TLV3201 configured as an ac-coupled comparator.

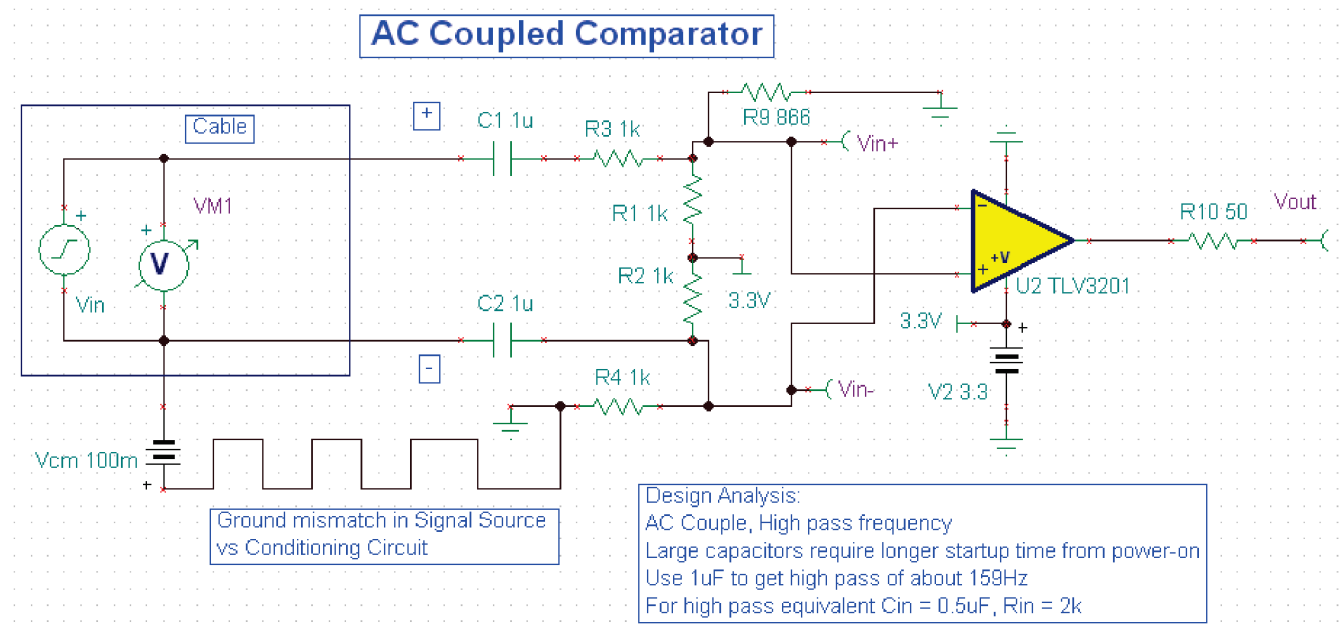


Figure 30. TLV3201 Configured as an AC-Coupled Comparator

Figure 31 shows a single-supply current monitor configured as a difference amplifier with a gain of 50. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201.

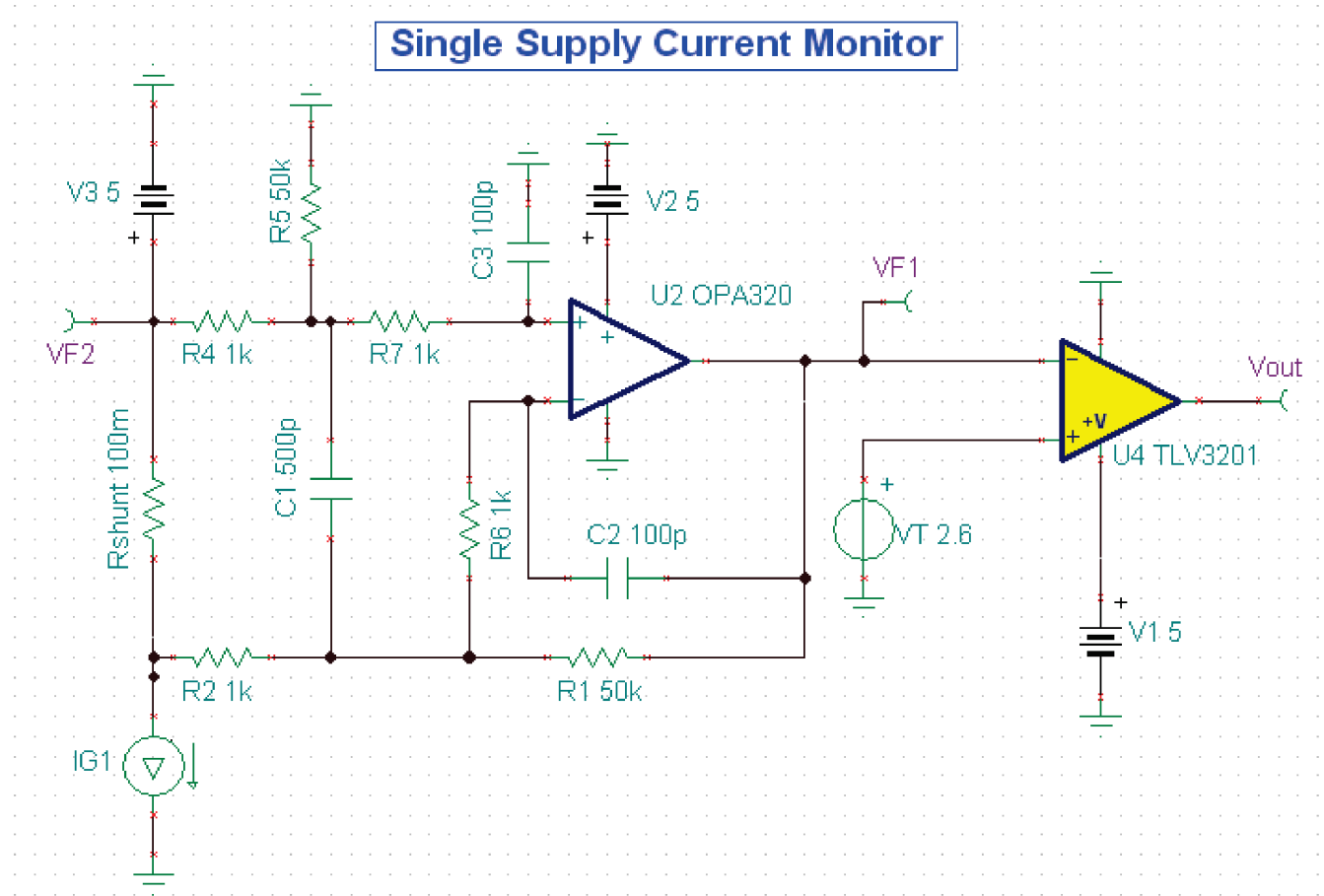


Figure 31. TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows the TMP20 and TLV3201 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

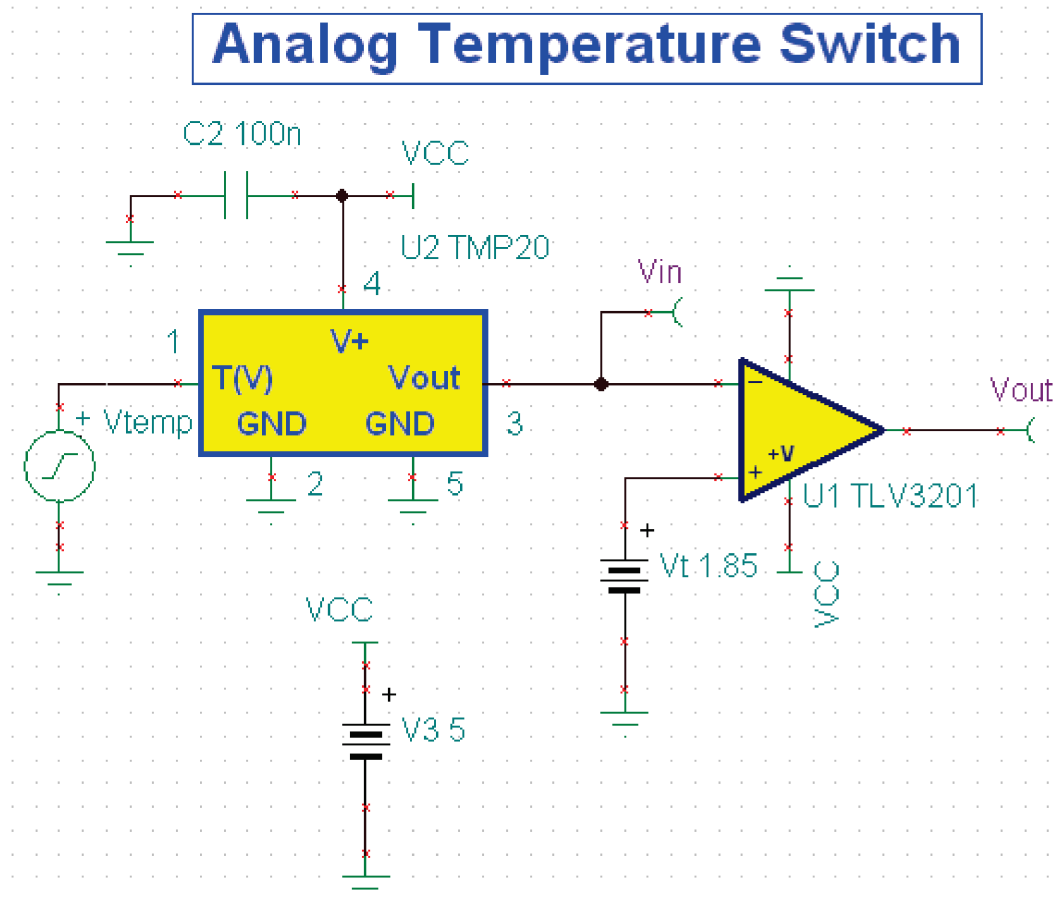


Figure 32. TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch



## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2012) to Revision A	Page
• Changed 产品状态从生产数据到混合状态 .....	1
• Added 双通道器件 .....	1

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3201AIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAI	Samples
TLV3201AIDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	RAI	Samples
TLV3201AIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3201AIDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3202AID	ACTIVE	SOIC	D	8	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples
TLV3202AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLV3201, TLV3202 :**

- Automotive : [TLV3201-Q1](#), [TLV3202-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3201AIDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3201AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3201AIDCKT	SC70	DCK	5	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
TLV3202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3202AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3201AIDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV3201AIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3201AIDCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV3202AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV3202AIDR	SOIC	D	8	2500	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV3202AID	D	SOIC	8	50	506.6	8	3940	4.32
TLV3202AIDGK	DGK	VSSOP	8	80	330	6.55	500	2.88

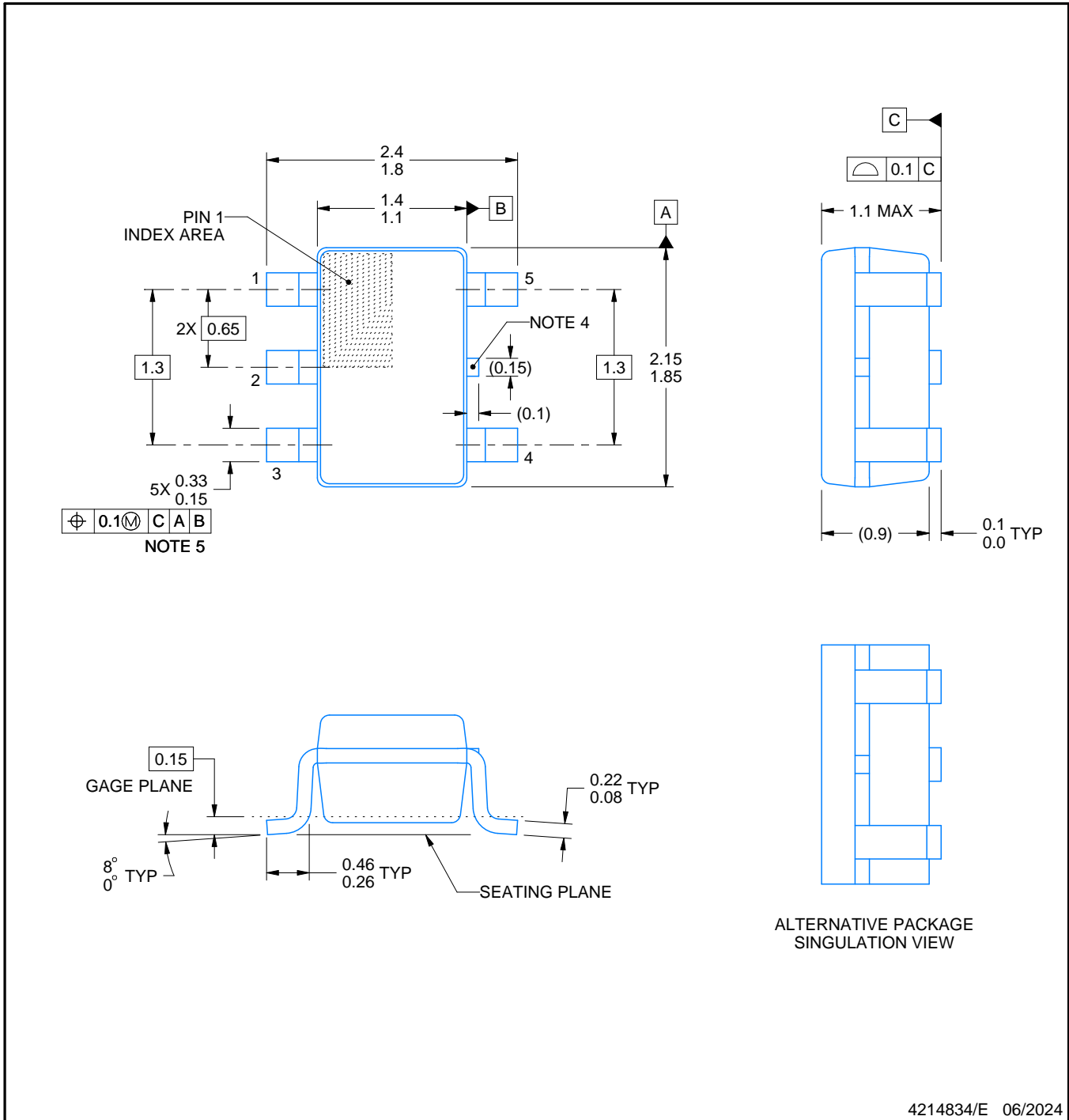
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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