



Single ATM PHY for 25.6 and 51.2 Mbps with Utopia Level 2

IDT77V107

Features List

- ◆ Performs the PHY-Transmission Convergence (TC) and Physical Media Dependent (PMD) Sublayer functions of the Physical Layer
- ◆ Compliant to ATM Forum (af-phy-040.000) and ITU-T I.432.5 specifications for 25.6 Mbps physical interface
- ◆ Also operates at 51.2Mbps
- ◆ 8-bit Utopia Level 2 Interface
- ◆ 3-Cell Transmit & Receive FIFOs
- ◆ Receiver Auto-Synchronization and Good Signal Indication
- ◆ Supports UTP Category 3 physical media
- ◆ Interfaces to standard magnetics
- ◆ Low-Power CMOS
- ◆ 3.3V supply with 5V tolerant inputs
- ◆ 100-lead TQFP Package (14 x 14 mm)
- ◆ Commercial and Industrial temperature ranges

Description

The IDT77V107 is a member of IDT's family of products supporting Asynchronous Transfer Mode (ATM) data communications and networking. The IDT77V107 implements the physical layer for 25.6 Mbps ATM, connecting a serial copper link (UTP Category 3) to an ATM

layer device such as a SAR or a switch ASIC. The IDT77V107 also operates at 51.2 Mbps and is well suited to backplane driving applications. The 77V107 has an 8-bit UTOPIA Level 2 interface on the cell side.

The IDT77V107 is fabricated using IDT's state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

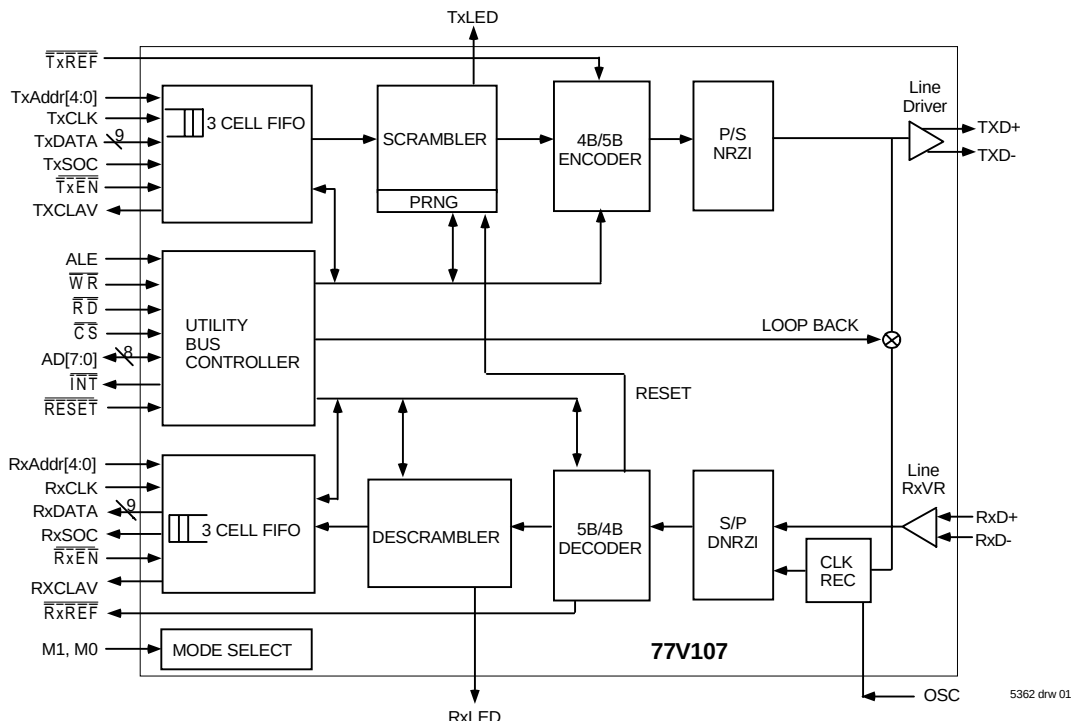
77V107 Overview

The 77V107 is a physical layer interface chip for 25.6Mbps ATM network communications as defined by ATM Forum document af-phy-040.000 and ITU-T I.432.5. The physical layer is divided into a Physical Media Dependent sub layer (PMD) and Transmission Convergence (TC) sub layer. It is based on the 77V106.

The PMD sub layer includes the functions for the transmitter, receiver and clock recovery for operation across 100 meters of category 3 unshielded twisted pair (UTP) cable. This is referred to as the Line Side Interface.

The TC sub layer defines the line coding, scrambling, data framing and synchronization. Transmitted cells are first scrambled, then pass through a 4b5b encoder and are finally NRZI encoded. In the 4b5b encoder, 4-bit nibbles are converted to 5-bit symbols via a look-up table. In addition to the 16 valid data symbols, a 17th symbol is used for a special escape (X) symbol. This symbol has the property of being

Functional Block Diagram



uniquely defined such that this bit sequence cannot be duplicated by concatenating any two other valid symbols. The escape symbol is used in combination with a second symbol to form command symbol pairs. Two command symbol pairs are defined as start-of-cell indicators, and one is used as the 8kHz timing marker.

In the absence of a cell to transmit, the TC will continue to generate valid symbols which are then transmitted across the line. When a complete cell is available for transmission, the TC transmits the appropriate start-of-cell command symbol pair followed immediately the scrambled and encoded 53-byte cell. A falling edge on the TxREF pin results in the insertion of an 8kHz timing marker in the transmit stream.

The receiver PMD performs clock and data recovery. The TC achieves symbol framing (as described below). Start-of-cell command symbol pairs and 8kHz timing symbol pair are handled appropriately, with receive cells being placed into the receive FIFO.

On the cell side, the 77V107 connects to an ATM layer device (such as a switch core or SAR) through an 8-bit Utopia Level 2 interface.

An 8-bit muxed address and data bus, controlled by a conventional asynchronous read/write handshake, provides software access to numerous internal control and status registers.

Additional pins permit insertion and extraction of an 8kHz timing marker, and provide LED indication of receive and transmit status.

Auto-Synchronization and Good Signal Indication

The 77V107 features a new receiver synchronization algorithm that allows it to achieve 4b5b symbol framing on any valid data stream. This is an improvement on earlier products which could frame only on the escape symbol, which occurs only in start-of-cell or 8kHz (X8) timing marker symbol pairs.

ATM25 transceivers always transmit valid 4b5b symbols, allowing the 77V107 receive section to achieve symbol framing and properly indicate receive signal status, even in the absence of ATM cells or 8kHz (X8) timing markers in the receive data stream. A state machine monitors the received symbols and asserts the "Good Signal" status bit when a valid signal is being received. "Good Signal" is deasserted and the receive FIFO is disabled when the signal is lost. This is sometimes referred to as Loss of Signal (LOS).

Operation at 51.2 Mbps

In addition to operation at the standard rate of 25.6 Mbps, the 77V107 is also specified to operate at 51.2 Mbps. Except for the doubled bit rate, all other aspects of operation are identical to the 25.6 Mbps mode. Other aspects of the ATM Forum Residential Broadband standard (af-rbb-phy-0101.000) at 51.2 Mbps are not supported.

Rate selection is determined by a combination of the reference clock frequency (OSC pin) and a software control bit. OSC is 32 MHz for the 25.6 Mbps line rate, and either 32 or 64 MHz for the 51.2 Mbps line rate.

See Figure 15 for recommended line magnetics. Magnetics for 51.2 Mbps operation have a higher bandwidth than magnetics optimized for 25.6 Mbps.

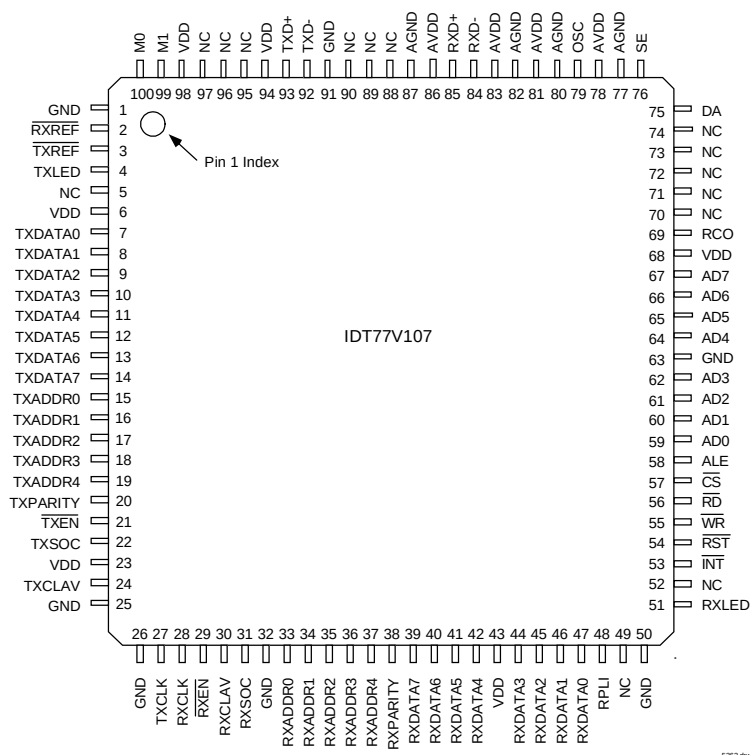


Figure 1 Pin Assignments

Line Side Signals

Signal Name	Pin Number	I/O	Signal Description
RXD+, RXD-	85, 84	In	Positive and negative receive differential input pair.
TXD+, TXD-	93, 92	Out	Positive and negative transmit differential output pair.

Utility Bus Signals

Signal Name	Pin Number	I/O	Signal Description
AD[7:0]	67, 66, 65, 64, 62, 61, 60, 59	In/Out	Utility bus address/data bus. The address input is sampled on the falling edge of ALE. Data is output on this bus when a read is performed. Input data is sampled at the completion of a write operation.
ALE	58	In	Utility bus address latch enable. Asynchronous input. An address on the AD bus is sampled on the falling edge of ALE. ALE must be low when the AD bus is being used for data.
CS	57	In	Utility bus asynchronous chip select. $\overline{CS}$ must be asserted to read or write an internal register. It may remain asserted at all times if desired.
RD	56	In	Utility bus read enable. Active low asynchronous input. After latching an address, a read is performed by deasserting $\overline{WR}$ and asserting RD and $\overline{CS}$.
WR	55	In	Utility bus write enable. Active low asynchronous input. After latching an address, a write is performed by deasserting RD, placing data on the AD bus, and asserting $\overline{WR}$ and $\overline{CS}$. Data is sampled when WR or $\overline{CS}$ is deasserted.

UTOPIA Bus Signals

Signal Name	Pin Number	I/O	Signal Description
RXADDR[4:0]	37, 36, 35, 34, 33	In	Utopia Receive Address. Address for polling and selecting a Utopia port/PHY.
RXCLAV	30	Out	Utopia Receive Cell Available. "1" indicates that the receive FIFO contains a complete received cell. "0" indicates that it does not. RXCLAV is high impedance when RXADDR[4:0] does not match the internally programmed Utopia address.
RXCLK	28	In	Utopia Receive Clock. This is a free running clock input.
RXDATA[7:0]	39, 40, 41, 42, 44, 45, 46, 47	Out	Utopia Receive Data. When one of the four ports is selected, the 77V107 transfers received cells to an ATM device across this bus. Also see RXPARITY.
$\overline{RXEN}$	29	In	Utopia Receive Enable. Driven by an ATM device to indicate its ability to receive data across the RXDATA bus.
RXPARTY	38	Out	Utopia Receive Data Parity. Odd parity over RXDATA[7:0].
RXSOC	31	Out	Utopia Receive Start of Cell. Asserted coincident with the first word of data for each cell on RXDATA.
TXADDR[4:0]	19, 18, 17, 16, 15	In	Utopia Transmit Address. Address for polling and selecting a Utopia port/PHY.
TXCLAV	24	Out	Utopia Transmit Cell Available. "1" indicates that the transmit FIFO has room available for at least one complete cell. "0" indicates that it does not. TXCLAV is high impedance when TXADDR[4:0] does not match the internally programmed Utopia address.
TXCLK	27	In	Utopia Transmit Clock. This is a free running clock input.
TXDATA[7:0]	14, 13, 12, 11, 10, 9, 8, 7	In	Utopia Transmit Data. An ATM device transfers cells across this bus to the 77V107 for transmission. Also see TXPARITY.
$\overline{TXEN}$	21	In	Utopia Transmit Enable. Driven by an ATM device to indicate it is transmitting data across the TXDATA bus.

Table 1 Signal Descriptions (Part 1 of 2)

TXPARITY	20	In	Utopia Transmit Data Parity. Odd parity across TXDATA[7:0]. Parity is checked and errors are indicated in the Interrupt Status Registers, as enabled in the Master Control Register. No other action is taken in the event of an error. Tie high or low if unused.
TXSOC	22	In	Utopia Transmit Start of Cell. Asserted coincident with the first word of data for each cell on TXDATA.
DA	75	In	Reserved signal. This input must be connected to logic low.
$\overline{\text{INT}}$	53	Out	Interrupt. $\overline{\text{INT}}$ is an open-drain output, driven low to indicate an interrupt. Once low, $\overline{\text{INT}}$ remains low until the interrupt status in the appropriate interrupt Status Register is read. Interrupt sources are programmable via the interrupt Mask Registers.
M1, M0	99, 100	In	Mode Select signals. These inputs must be connected to logic low.
OSC	79	In	TTL line rate clock source, driven by a 100 ppm oscillator. 32 MHz for 25.6 Mbps; 64 MHz for 51.2 Mbps.
RCO	69	Out	Recovered Clock Output. This is the bit clock from the receive section.
RPLI	48	Out	Reserved signal. This output should be allowed to float (unconnected).
$\overline{\text{RST}}$	54	In	Reset. Active low asynchronous input resets all control logic, counters and FIFOs. A reset must be performed after power up prior to normal operation of the part.
RXLED	51	Out	Receive LED driver. Driven low for 223 cycles of OSC, beginning with RXSOC when a good (non-null and non-errored) cell is received. Drives 8 mA both high and low.
$\overline{\text{RXREF}}$	2	Out	Receive Reference. Active low. $\overline{\text{RXREF}}$ pulses low for a programmable number of clock cycles when an x_8 command byte is received.
SE	76	In	Reserved signal. This input must be connected to logic low.
TXLED	4	Out	Transmit LED driver. Goes low for 223 cycles of OSC, beginning with TXSOC when a cell is received for transmission. 8 mA drive current both high and low
$\overline{\text{TXREF}}$	3	In	Transmit Reference. At the falling edge of $\overline{\text{TXREF}}$, an X_8 command byte is inserted into the transmit data stream. Typical application is WAN timing.

Power Supply Signals			
Signal Name	Pin Number	I/O	Signal Description
AGND	77, 80, 82, 87	—	Analog ground. AGND is ground the analog portion of the ship, which sources a more constant current than the digital portion.
AVDD	78, 81, 83, 86	—	Analog power supply. AVDD supplies power to the analog portion of the chip, which draws a more constant current than the digital portion. $3.3 \pm 0.3\text{V}$
GND	1, 25, 26, 32, 50, 63, 91	—	Digital Ground.
VDD	6, 23, 43, 68, 94, 98	—	Digital power supply. $3.3 \pm 0.3\text{V}$.

Table 1 Signal Descriptions (Part 2 of 2)

Functional Description

Transmission convergence (TC) sub layer

Introduction

The TC sub layer defines the line coding, scrambling, data framing and synchronization. Under control of a switch interface or Segmentation and Reassembly (SAR) unit, the 25.6Mbps ATM PHY accepts a 53-byte ATM cell, scrambles the data, appends a command byte to the beginning of the cell, and encodes the entire 53 bytes before transmission. These data transformations ensure that the signal is evenly distributed across the frequency spectrum. In addition, the serialized bit stream is NRZI coded. An 8kHz timing sync pulse may be used for isochronous communications.

Data Structure and Framing

Each 53-byte ATM cell is preceded with a command byte. This byte is distinguished by an escape symbol followed by one of 17 encoded symbols. Together, this byte forms one of seventeen possible command bytes. Three command bytes are defined:

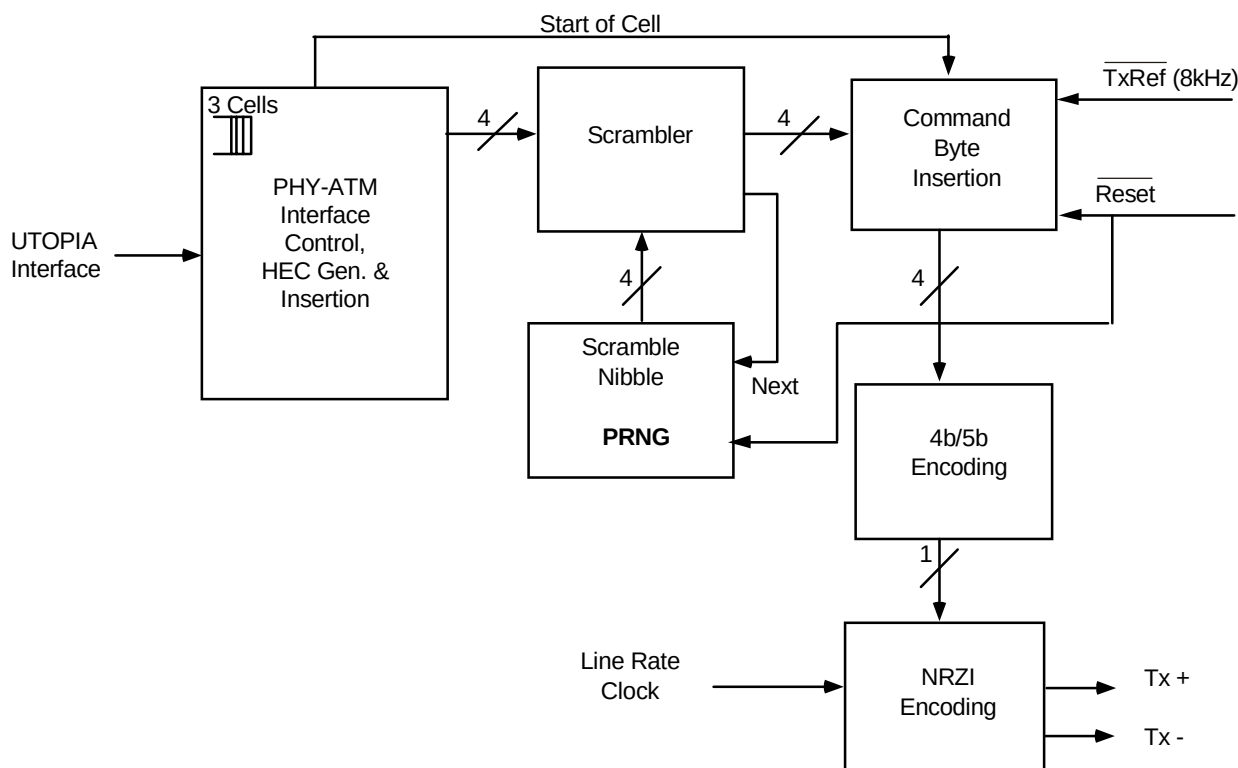
1. **X_X** (read: 'escape' symbol followed by another 'escape'): Start-of-cell with scrambler/descrambler reset.

2. **X_4** ('escape' followed by '4'): Start-of-cell without scrambler/descrambler reset.
3. **X_8** ('escape' followed by '8'): 8kHz timing marker. This command byte is generated when the 8kHz sync pulse is detected, and has priority over all line activity (data or command bytes). It is transmitted immediately when the sync pulse is detected. When this occurs during a cell transmission, the data transfer is temporarily interrupted on an octet boundary, and the X_8 command byte is inserted. This condition is the only allowed interrupt in an otherwise contiguous transfer.

Below is an illustration of the cell structure and command byte usage:

{X_X} {53-byte ATM cell} {X_4} {53-byte ATM cell} {X_8} cell} ...

In the above example, the first ATM cell is preceded by the X_X start-of-cell command byte which resets both the transmitter-scrambler and receiver-descrambler pseudo-random nibble generators (PRNG) to their initial states. The following cell illustrates the insertion of a start-of-cell command without scrambler/descrambler reset. During this cell's transmission, an 8kHz timing sync pulse triggers insertion of the X_8 8kHz timing marker command byte.



5362 drw 05

Figure 2 TC Transmit Block Diagram

Transmission Description

Refer to Figure 4 on the previous page. Cell transmission begins with the PHY-ATM Interface. An ATM layer device transfers a cell into the 77V107 across the Utopia transmit bus. This cell enters a 3-cell deep transmit FIFO. Once a complete cell is in the FIFO, transmission begins by passing the cell, four bits (MSB first) at a time to the 'Scrambler'.

The 'Scrambler' takes each nibble of data and exclusive-ORs them against the 4 high order bits ($X(t)$, $X(t-1)$, $X(t-2)$, $X(t-3)$) of a 10 bit pseudo-random nibble generator (PRNG). Its function is to provide the appropriate frequency distribution for the signal across the line.

The PRNG is clocked every time a nibble is processed, regardless of whether the processed nibble is part of a data or command byte. Note however that only data nibbles are scrambled. The entire command byte (X_C) is NOT scrambled before it's encoded (see diagram for illustration). The PRNG is based upon the following polynomial:

$$X^{10} + X^7 + 1$$

With this polynomial, the four output data bits ($D3$, $D2$, $D1$, $D0$) will be generated from the following equations:

$$D3 = d3 \text{ xor } X(t-3)$$

$$D2 = d2 \text{ xor } X(t-2)$$

$$D1 = d1 \text{ xor } X(t-1)$$

$$D0 = d0 \text{ xor } X(t)$$

The following nibble is scrambled with $X(t+4)$, $X(t+3)$, $X(t+2)$, and $X(t+1)$.

A scrambler lock between the transmitter and receiver occurs each time an X_X command is sent. An X_X command is initiated only at the beginning of a cell transfer after the PRNG has cycled through all of its states ($2^{10} - 1 = 1023$ states). The first valid ATM data cell transmitted after power on will also be accompanied with an X_X command byte. Each time an X_X command byte is sent, the first nibble after the last escape (X) nibble is XOR'd with 1111b (PRNG = 3FFx).

Because a timing marker command (X_8) may occur at any time, the possibility of a reset PRNG start-of-cell command and a timing marker command occurring consecutively does exist (e.g. $X_X_X_8$). In this case, the detection of the last two consecutive escape (X) nibbles will cause the PRNG to reset to its initial 3FFx state. Therefore, the PRNG is clocked only after the first nibble of the second consecutive escape pair.

Once the data nibbles have been scrambled using the PRNG, the nibbles are further encoded using a 4b/5b process. The 4b/5b scheme ensures that an appropriate number of signal transitions occur on the line. A total of seventeen 5-bit symbols are used to represent the sixteen 4-bit data nibbles and the one escape (X) nibble. The table below lists the 4-bit data with their corresponding 5-bit symbols:

Data	Symbol	Data	Symbol
0000	10101	0001	01001
0100	00111	0101	01101
1000	10010	1001	11001
1100	10111	1101	11101

Data	Symbol	Data	Symbol
0010	01010	0011	01011
0110	01110	0111	01111
1010	11010	1011	11011
1110	11110	1111	11111

ESC(X) = 00010

3505 drw 05a

This encode/decode implementation has several very desirable properties. Among them is the fact that the output data bits can be represented by a set of relatively simple symbols;

- ♦ Run length is limited to ≤ 5 ;
- ♦ Disparity never exceeds ± 1 .

On the receiver, the decoder determines from the received symbols whether a timing marker command (X_8) or a start-of-cell command was sent (X_X or X_4). If a start-of-cell command is detected, the next 53 bytes received are decoded and forwarded to the descrambler. (See the TC Receive Block Diagram).

The output of the 4b/5b encoder provides serial data to the NRZI encoder. The NRZI code transitions the wire voltage each time a '1' bit is sent. This, together with the previous encoding schemes guarantees that long run lengths of either '0' or '1's are prevented. Each symbol is shifted out with its most significant bit sent first.

When no cells are available to transmit, the 77V107 keeps the line active by continuing to transmit valid symbols. But it does not transmit another start-of-cell command until it has another cell for transmission. The 77V107 never creates its own idle cells for transmission.

Transmit HEC Byte Calculation/Insertion

Byte #5 of each ATM cell, the HEC (Header Error Control) is calculated automatically across the first 4 bytes of the cell header, depending upon the setting of bit 5 of the LED Driver and HEC Status/Control Register (0x03). This byte is then either inserted as a replacement of the fifth byte transferred to the PHY by the external system, or the cell is transmitted as received. A third operating mode provides for insertion of "Bad" HEC codes which may aid in communication diagnostics. These modes are controlled by the LED Driver and HEC Status/Control Registers.

Receiver Description

The receiver side of the TC sublayer operates like the transmitter, but in reverse. The data is NRZI decoded before each symbol is reassembled. The symbols are then sent to the 5b/4b decoder, followed by the Command Byte Interpreter, De-Scrambler, and finally through a FIFO to the UTOPIA interface to an ATM Layer device.

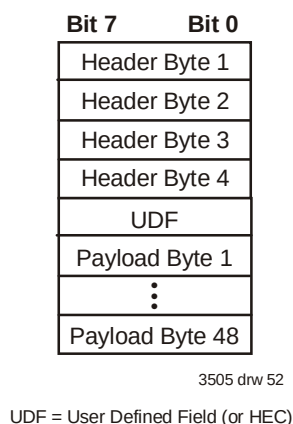


Figure 3 ATM Cell Format

Note that although the IDT77V107 can detect symbol and HEC errors, it does not attempt to correct them.

Upon resetting the device or re-establishing a serial link, logic in front of the 4b/5b decoder uses feedback from the 4b/5b decoder to determine if it is not properly “framed” on the 5-bit symbols. If not properly

framed, it will shift its framing, one bit at a time, until it achieves proper symbol framing. Receipt of an Escape (X) symbol will also force proper symbol framing.

The IDT77V107 monitors line conditions and can provide an interrupt if the line is deemed 'bad'. The Interrupt Status Register contains a Good Signal Bit (bit 6, set to 0 = Bad signal initially) which shows the status of the line per the following algorithm:

To declare 'Good Signal' (from "Bad" to "Good"):

There is an up-down counter that counts from 7 to 0 and is initially set to 7. When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and no "bad symbol" has been received, the counter decreases by one. However, if at least one "bad symbol" is detected during these 1,024 clocks, the counter is increased by one, to a maximum of 7. The Good Signal Bit is set to 1 when this counter reaches 0. The Good Signal Bit could be set to 1 as quickly as 1,433 symbols (204.8×7) if no bad symbols have been received.

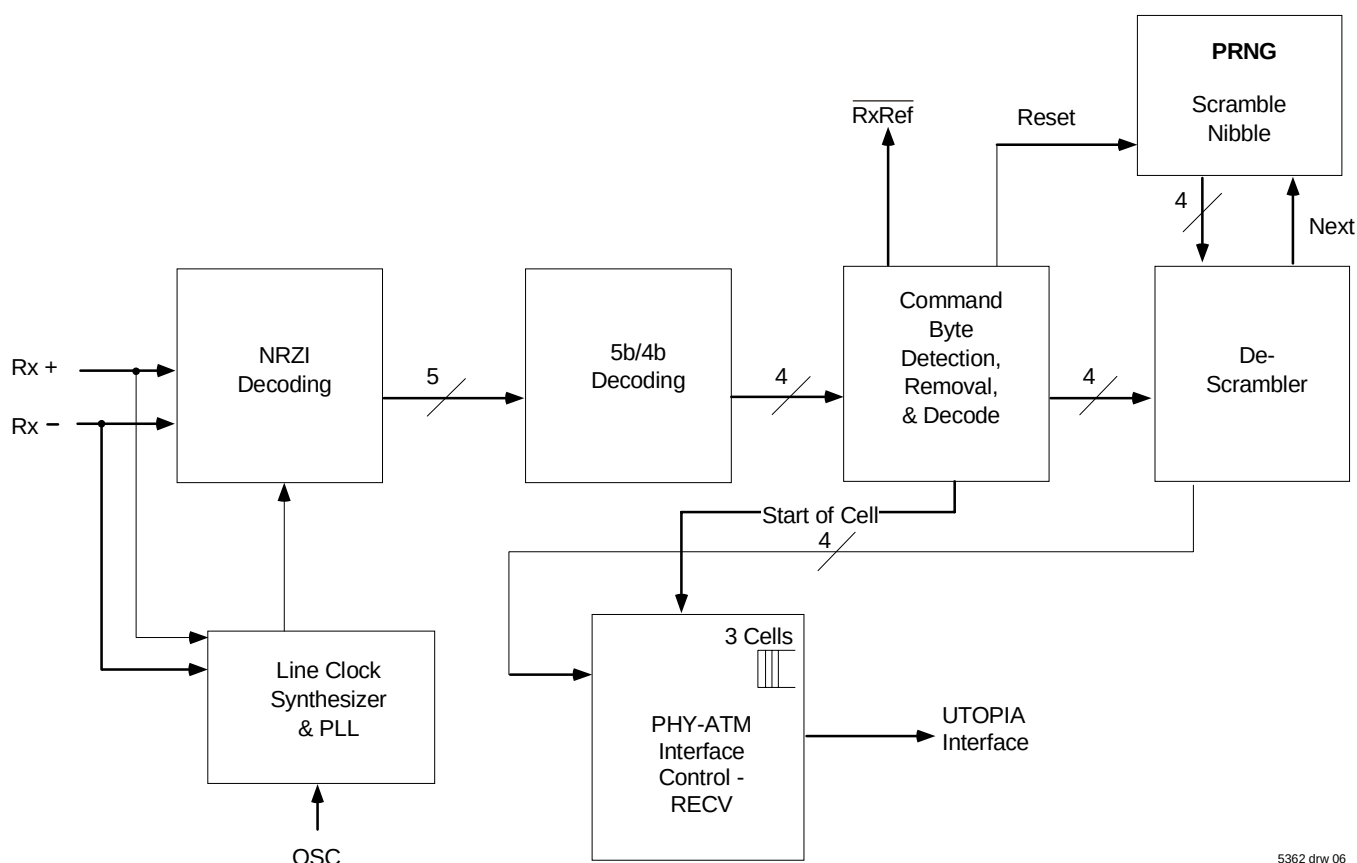


Figure 4 TC Receive Block Diagram

To declare 'Bad Signal' (from "Good" to "Bad"):

The same up-down counter counts from 0 to 7 (being at 0 to provide a "Good" status). When the clock ticks for 1,024 cycles (32MHz clock, 1,024 cycles = 204.8 symbols) and there is at least one "bad symbol", the counter increases by one. If it detects all "good symbols" and no "bad symbols" in the next time period, the counter decreases by one. The "Bad Signal" is declared when the counter reaches 7. The Good Signal Bit could be set to 0 as quickly as 1,433 symbols (204.8 x 7) if at least one "bad symbol" is detected in each of seven consecutive groups of 204.8 symbols.

8kHz Timing Marker

The 8kHz timing marker, described earlier, is a completely optional feature which is essential for some applications requiring synchronization for voice or video, and unnecessary for other applications. When unused, $\overline{\text{TXREF}}$ should be tied high. Also note that it is not limited to 8kHz, should a different frequency be desired. When looped, a received X_8 command byte causes one to be generated on the transmit side.

A received X_8 command byte causes the 77V107 to issue a negative pulse on $\overline{\text{RXREF}}$. The source channel of the marker is programmable.

Utopia Level 2 PHY-ATM Interface

UTOPIA Level 2 is a Physical Layer to ATM Layer interface standardized by the ATM Forum. It is selected using the M1 and M0 pins. It transfers ATM cells and has separate transmit and receive channels and specific handshaking protocols. UTOPIA Level 2 has dedicated address signals for both the transmit and receive directions that allow the ATM layer device to specify which PHY device it is communicating with. It is defined in ATM Forum document af-phy-0039.

Note that the 77V107 supports the standard "Operation with 1 TxClav and 1 Rx Clav" multi-phy scheme from the Utopia Level 2 standard. The optional Multiplexed Status Polling multi-phy scheme is not directly supported.

There is a single 8-bit data bus in the transmit (ATM-to-PHY) direction, and a single 8-bit data bus in the receive (PHY-to-ATM) direction. In addition to the data bus, each direction also includes a single optional parity bit, an address bus, and several handshaking signals. The UTOPIA address of the PHY is determined by bits 4 to 0 in the Enhanced Control Register. Please note that the transmit bus and the receive bus operate completely independently. The Utopia signals are summarized below:

TXDATA[7:0]	ATM to PHY
TXPARITY	ATM to PHY
TXSOC	ATM to PHY
TXADDR[4:0]	ATM to PHY
$\overline{\text{TXEN}}$	ATM to PHY
TXCLAV	PHY to ATM
TXCLK	ATM to PHY
RXDATA[7:0]	PHY to ATM
RXPARITY	PHY to ATM
RXSOC	PHY to ATM
RXADDR[4:0]	ATM to PHY
$\overline{\text{RXEN}}$	ATM to PHY
RXCLAV	PHY to ATM
RXCLK	ATM to PHY

The ATM device starts by polling the PHY ports on the Utopia bus to determine if any of them has room to accept a cell for transmission (TXCLAV), or has a receive cell available to pass on to the ATM device (RXCLAV). To poll, the ATM device drives an address (TXADDR or RXADDR) then observes TXCLAV or RXCLAV on the next cycle of TXCLK or RXCLK. The PHY will tri-state TXCLAV and RXCLAV except when it is addressed.

If TXCLAV or RXCLAV is asserted, the ATM device may select the PHY, then transfer a cell to or from it. Selection of a PHY is performed by driving the address of the desired port while $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ is high, then driving $\overline{\text{TXEN}}$ or $\overline{\text{RXEN}}$ low. When $\overline{\text{TXEN}}$ is driven low, TXSOC (start of cell) is driven high to indicate that the first byte of the cell is being driven on TXDATA. The ATM device may choose to temporarily suspend transfer of the cell by deasserting $\overline{\text{TXEN}}$. Otherwise, $\overline{\text{TXEN}}$ remains asserted as the next byte is driven onto TXDATA with each cycle of TXCLK.

In the receive direction, the ATM device selects a PHY if it wishes to receive the cell that the PHY is holding. It does this by asserting $\overline{\text{RXEN}}$. The PHY then transfers the data 8 bits each clock cycle, as determined by $\overline{\text{RXEN}}$. As in the transmit direction, the ATM device may suspend transfer by deasserting $\overline{\text{RXEN}}$ at any time. Note that the PHY asserts RXSOC coincident with the first byte of each cell.

TXPARITY and RXPARITY are parity bits for the corresponding 8-bit data fields. Odd parity is used, which means that for an all-zero data pattern, the corresponding parity bit is one.

The following figures may be referenced for Utopia Level 2 bus examples.

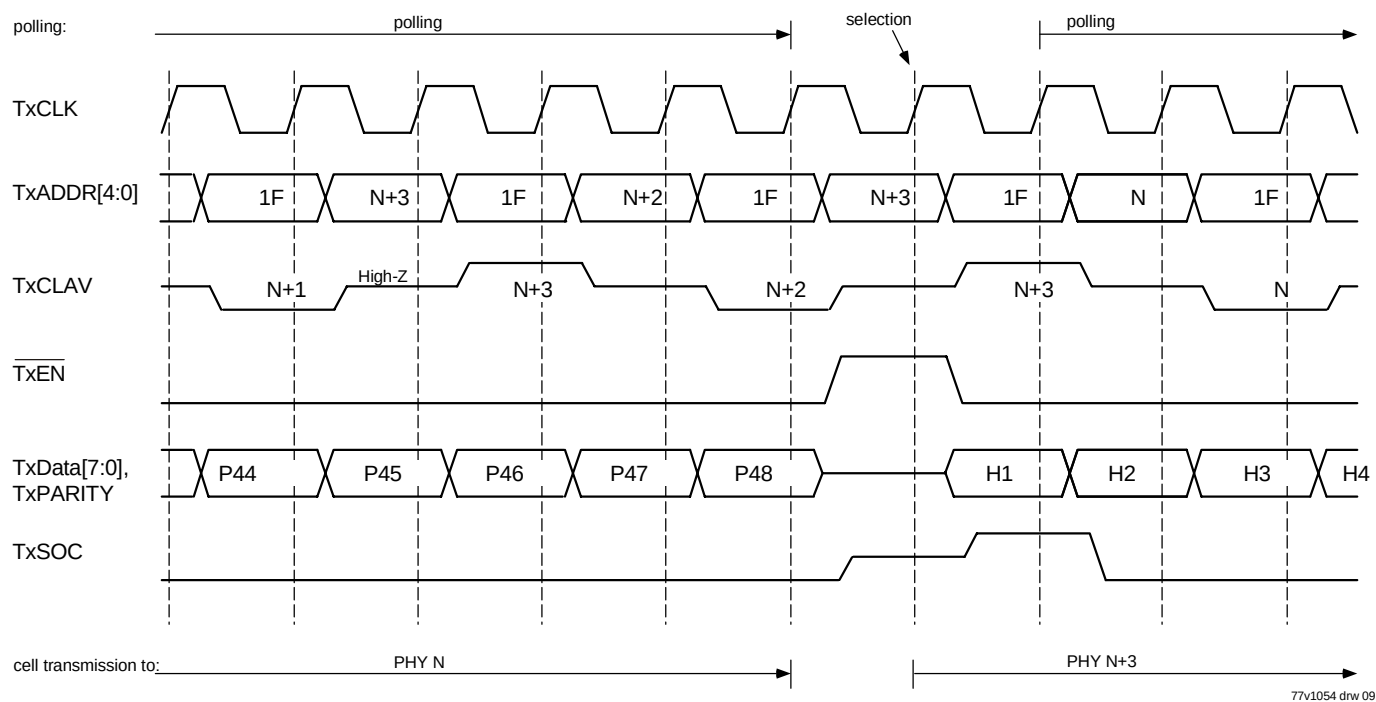


Figure 5 Utopia Transmit Handshake - Back to Back Cells

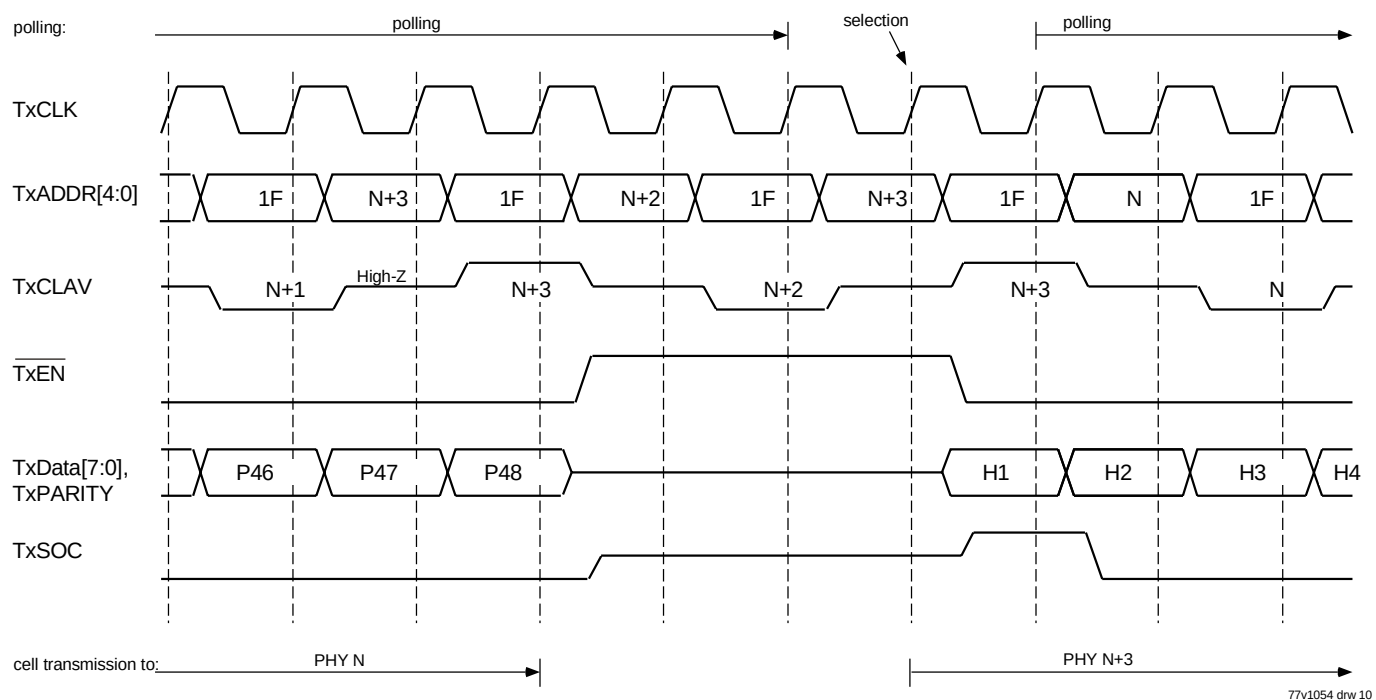


Figure 6 Utopia Transmit Handshake - Delay Between Cells

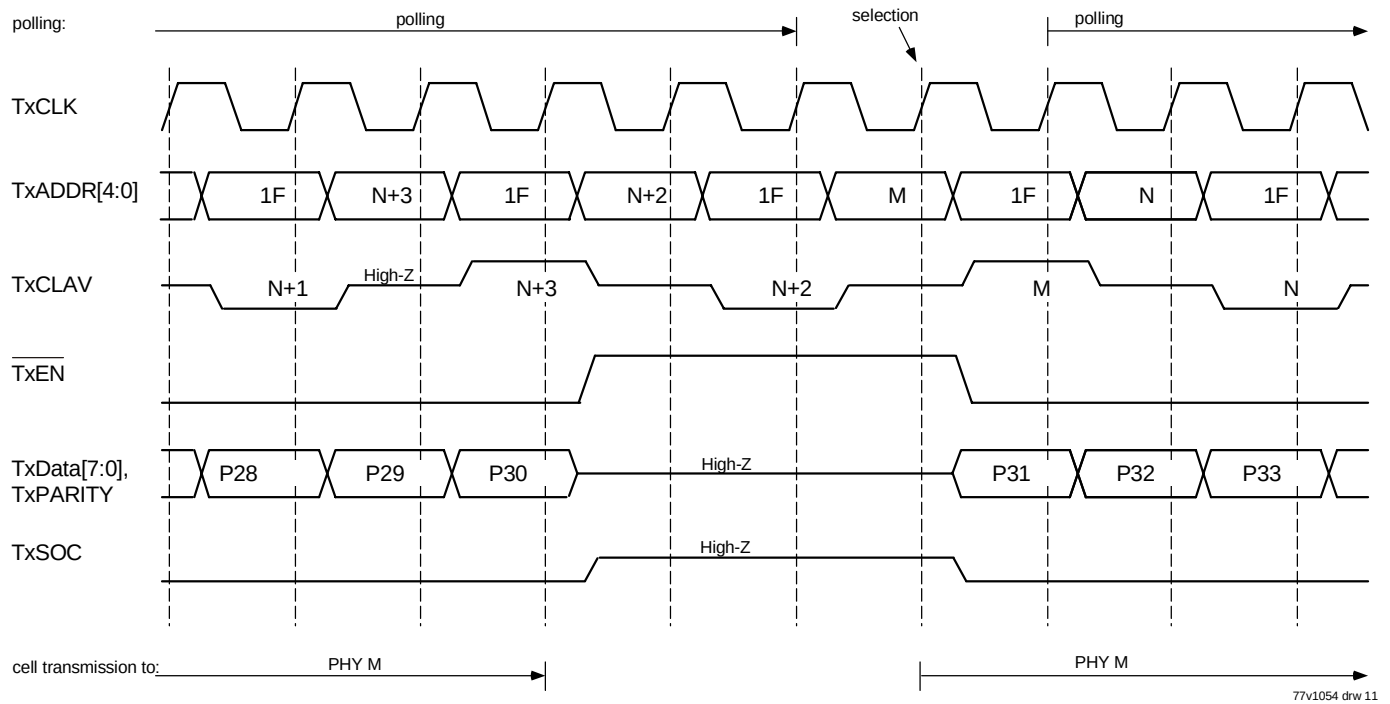


Figure 7 Utopia Transmit Handshake - Transmission Suspended

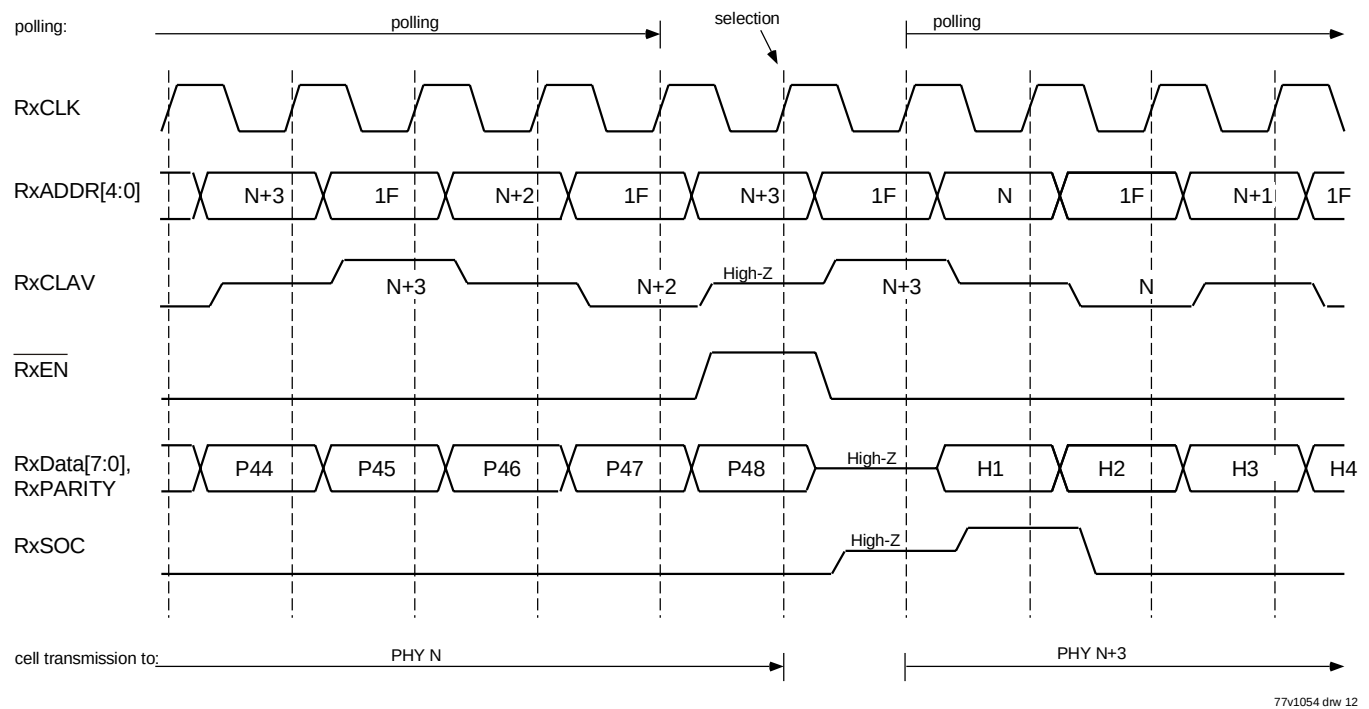


Figure 8 Utopia Receive Handshake - Back to Back Cells

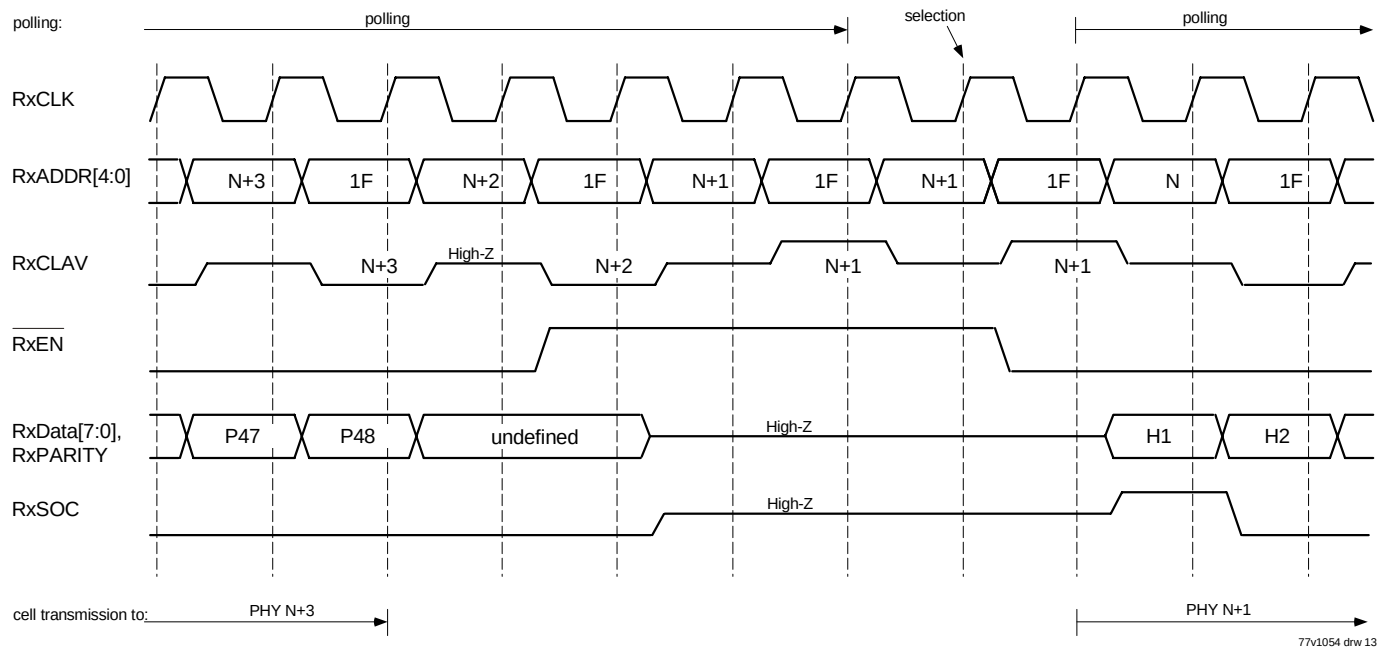


Figure 9 Utopia Receive Handshake - Delay Between Cells

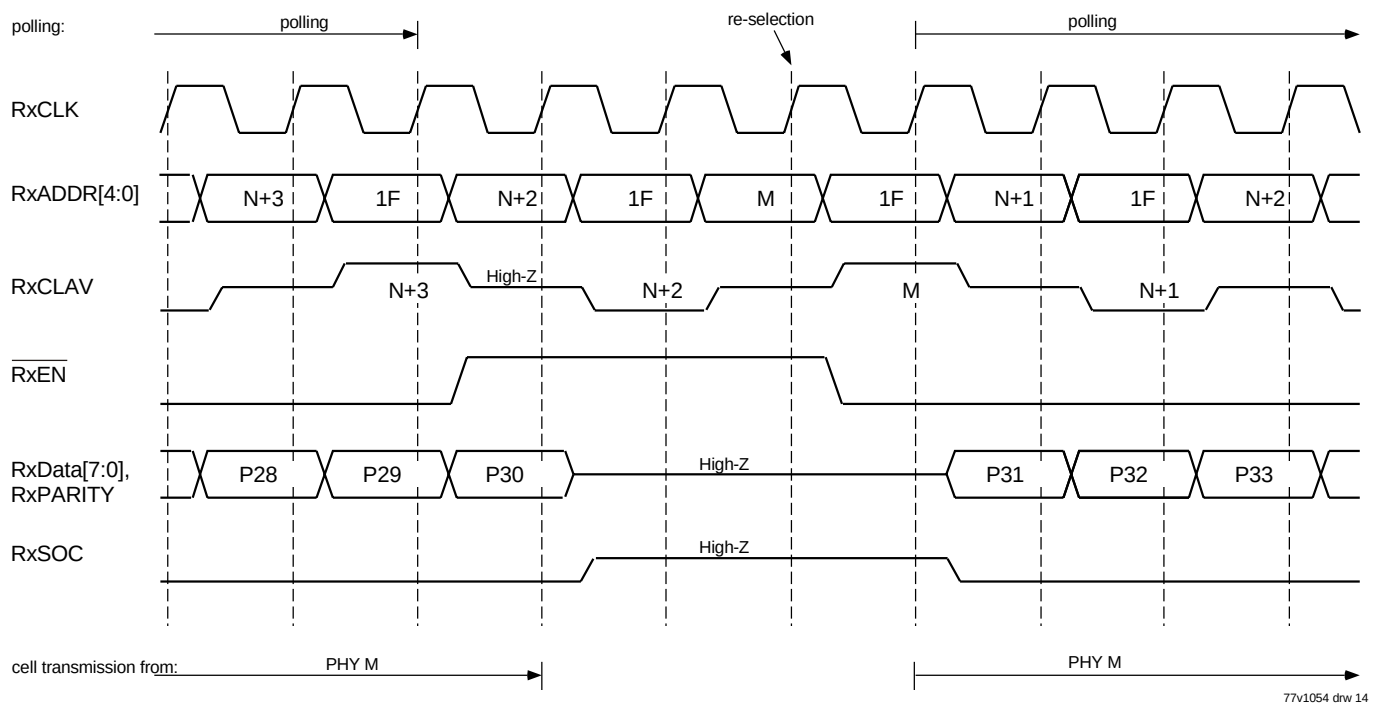


Figure 10 Utopia 2 Receive Handshake - Suspended Transfer of Data

Control and Status Interface

Utility Bus

The Utility Bus is a byte-wide interface that provides access to the registers within the IDT77V107. These registers are used to select desired operating characteristics and functions, and to communicate status to external systems.

The Utility Bus is implemented using a multiplexed address and data bus (AD[7:0]) where the register address is latched via the Address Latch Enable (ALE) signal.

The Utility Bus interface is comprised of the following pins:

AD[7:0], ALE, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$

Read Operation

Refer to the Utility Bus timing waveforms. A register read is performed as follows:

1. Initial condition:
 - $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$ not asserted (logic 1)
 - ALE not asserted (logic 0)
2. Set up register address:
 - place desired register address on AD[7:0]
 - set ALE to logic 1;
 - latch this address by setting ALE to logic 0.
3. Read register data:
 - Remove register address data from AD[7:0]
 - assert $\overline{\text{CS}}$ by setting to logic 0;
 - assert $\overline{\text{RD}}$ by setting to logic 0
 - wait minimum pulse width time (see AC specifications)

Write Operation

A register write is performed as described below:

1. Initial condition:
 - $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{CS}}$ not asserted (logic 1)
 - ALE not asserted (logic 0)
2. Set up register address:
 - place desired register address on AD[7:0]
 - set ALE to logic 1;
 - latch this address by setting ALE to logic 0.
3. Write data:
 - place data on AD[7:0]
 - assert $\overline{\text{CS}}$ by setting to logic 0;
 - assert $\overline{\text{WR}}$ (logic 0) for minimum time (according to timing specification); reset $\overline{\text{WR}}$ or $\overline{\text{CS}}$ to logic 1 to complete register write cycle.

Interrupt Operations

A variety of selectable interrupt and signalling conditions are provided. They are useful both during 'normal' operation, and as diagnostic aids. Refer to the Status and Control Register List section.

Overall interrupt control is provided via bit 0 of the Master Control Register. When this bit is cleared (set to 0), interrupt signalling is prevented on the respective port. The Interrupt Mask Register allows individual masking of different interrupt sources. Additional interrupt

signal control is provided by bit 5 of the Master Control Register. When this bit is set (=1), receive cell errors will be flagged via interrupt signalling and all other interrupt conditions are masked. These errors include:

- Bad receive HEC
- Short (fewer than 53 bytes) cells
- Received cell symbol error

Normal interrupt operations are performed by setting bit 0 and clearing bit 5 in the Master Control Register. $\overline{\text{INT}}$ (pin 34) will go to a low state when an interrupt condition is detected. The external system should then interrogate the 77V107 to determine which one (or more) conditions caused this flag, and reset the interrupt for further occurrences. This is accomplished by reading the Interrupt Status Register. Decoding the bits in this byte will tell which error condition caused the interrupt. Reading these registers also:

- clears the (sticky) interrupt status bits in the registers that are read
- resets $\overline{\text{INT}}$

This leaves the interrupt system ready to signal an alarm for further problems.

LED Control and Signalling

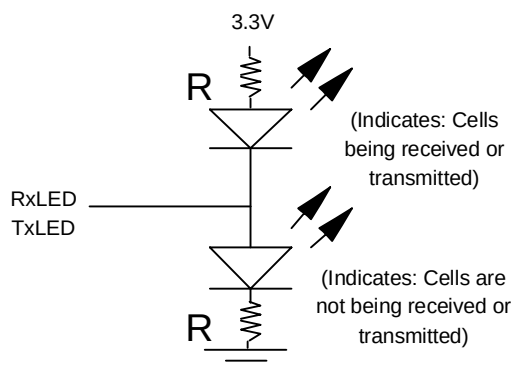
The LED outputs provide bi-directional LED drive capability of 8 mA. As an example, the RxLED outputs are described in the truth table:

State	Pin Voltage
Cells being transmitted	Low
Cells not being received	High

As illustrated in the following figure, this could be connected to provide for a two-LED condition indicator. These could also be different colors to provide simple status indication at a glance. (The minimum value for R should be 330 Ω).

TxLED Truth Table

State	Pin Voltage
Cells being transmitted	Low
Cells not being received	High



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Figure 11

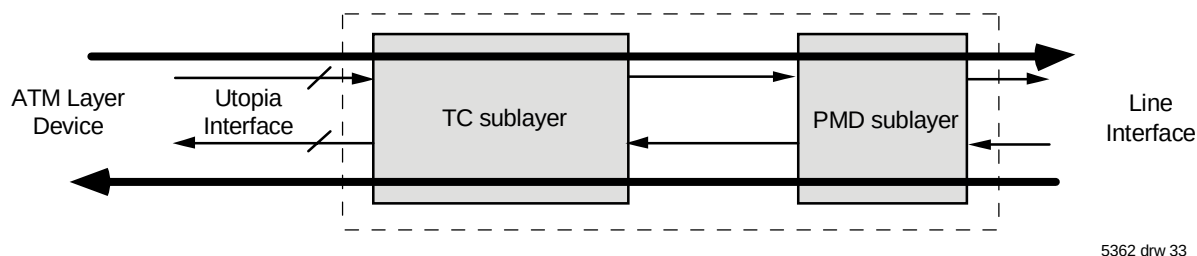
Diagnostic Functions

1. Loopback

There are two loopback modes supported by the 77V107. The loopback mode is controlled via bits 1 and 0 of the Diagnostic Control Registers:

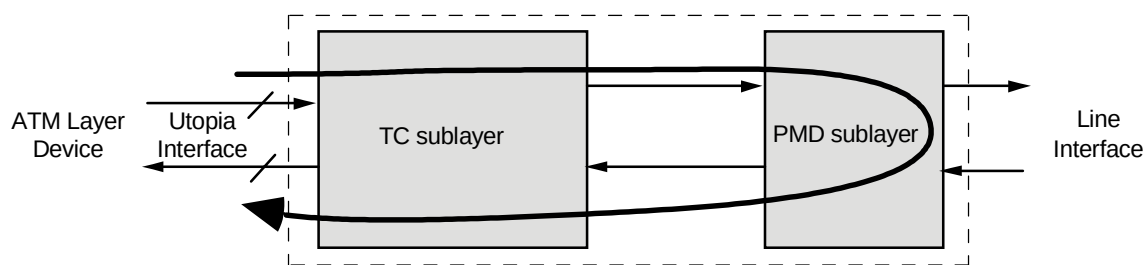
Normal Mode

Figure 12 shows normal operating conditions: data to be transmitted is transferred to the TC, where it is queued and formatted for transmission by the PMD. Receive data from the PMD is decoded along with its clock for transfer to the receiving "upstream system".



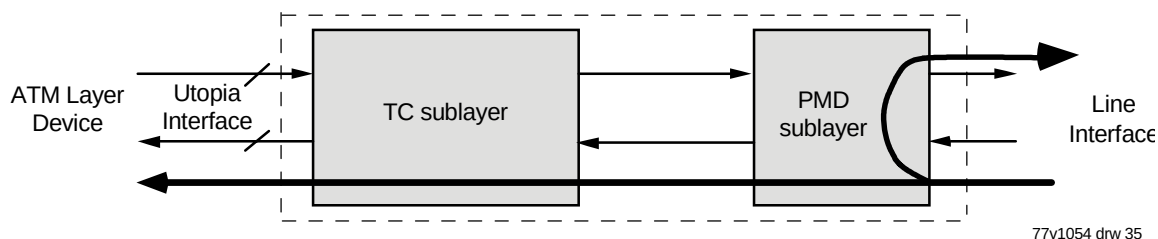
5362 drw 33

Figure 12 Normal Mode



77v1054 drw 34

Figure 13 PHY Loopback



77v1054 drw 35

Figure 14 Line Loopback

PHY Loopback

As Figure 13 illustrates below, this loopback mode provides a connection within the PHY from the transmit PHY-ATM interface to the PHY-ATM receive interface. Note that while this mode is operating, no data is forwarded to or received from the line interface.

Line Loopback

Figure 14 might also be called "remote loopback" since it provides for a means to test the overall system, including the line. Since this mode will probably be entered under direction from another system (at a remote location), receive data is also decoded and transferred to the upstream system to allow it to listen for commands. A common example would be a command asking the upstream system to direct the TC to leave this loopback state, and resume normal operations.

2. Counters

Several condition counters are provided to assist external systems (e.g. software drivers) in evaluating communications conditions. It is anticipated that these counters will be polled from time to time (user selectable) to evaluate performance.

- ◆ Symbol Error Counters
 - 8 bits
 - counts all invalid 5-bit symbols received
- ◆ Transmit Cell Counters
 - 16 bits
 - counts all transmitted cells
- ◆ Receive Cell Counters
 - 16 bits
 - counts all received cells, excluding idle cells and HEC errored cells
- ◆ Receive HEC Error Counters
 - 5 bits
 - counts all HEC errors received

The TxCell and RxCell counters are sized (16 bits) to provide a full cell count (without roll over) if the counter is read once/second. The Symbol Error counter and HEC Error counter were given sufficient size to indicate exact counts for low error-rate conditions. If these counters overflow, a gross condition is occurring, where additional counter resolution does not provide additional diagnostic benefit.

Reading Counters

1. Decide which counter value is desired. Write to the Counter Select Register to the bit location corresponding to the desired counter. This loads the High and Low Byte Counter Registers with the selected counter's value, and resets this counter to zero.

NOTE: Only one counter may be enabled at any time in the Counter Select Register.

2. Read the Counter Registers (low byte and high byte) to get the value.

Further reads may be accomplished in the same manner by writing to the Counter Select Registers.

Line Side (Serial) Interface

PHY to Magnetics Interface

A standard connection to 100Ω and 120Ω unshielded twisted pair cabling is shown in the figure below. Note that the transmit signal is somewhat attenuated in order to meet the launch amplitude specified by the standards. The receive circuitry is designed to attenuate low frequencies in order to compensate for the high frequency attenuation of the cable.

Also, the receive circuitry biases the positive and negative RX inputs to slightly different voltages. This is done so that the receiver does not receive false signals in the absence of a real signal. This can be important because the 77V107 does not disable error detection or interrupts when an input signal is not present.

When connecting to UTP at 51.2 Mbps, it is necessary to use magnetics with sufficient bandwidth. Such a device can also operate satisfactorily at 25.6 Mbps.

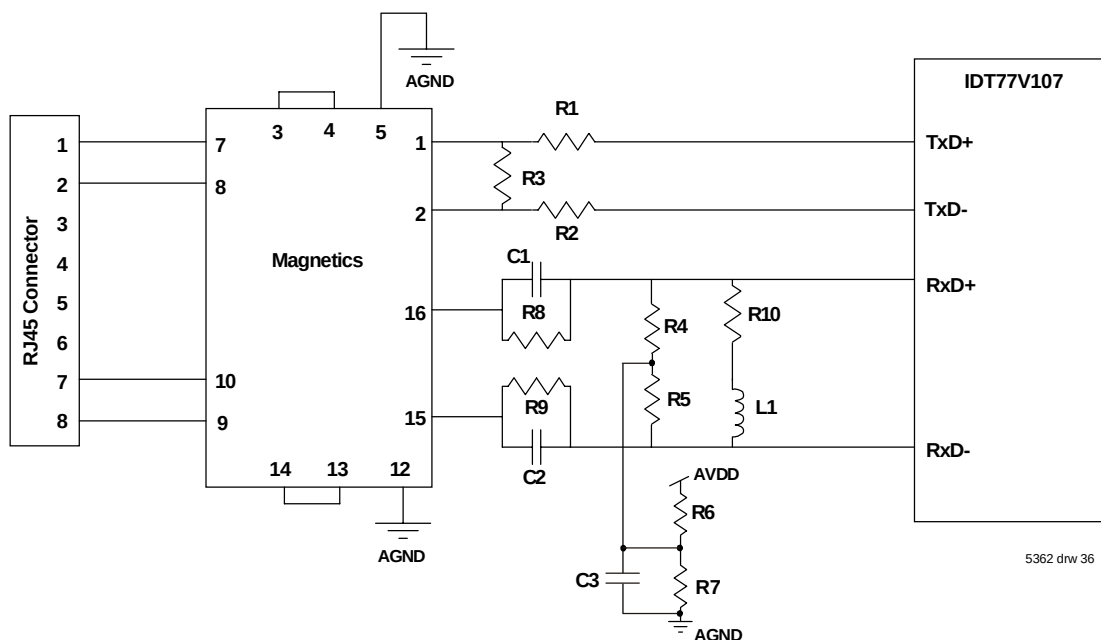


Figure 15 Recommended Connection to Magnetics

Component	Value	Tolerance
R1	47Ω	±5%
R2	47Ω	±5%
R3	620Ω	±5%
R4	62Ω	±5%
R5	62Ω	±5%
R6	10kΩ	±5%
R7	10kΩ	±5%
R8	33Ω	±5%
R9	33Ω	±5%
R10	82Ω	±5%
C1	470pF	±20%
C2	470pF	±20%
C3	0.1μF	±20%
L1	3.3μH	±20%

Table 2 Analog Component Values

Magnetics Modules for 25.6 Mbps

Pulse PE-67583 or R4005 (619) 674-8100

TDK TLA-6M103 (847) 803-6100

Magnetics Modules for 51.2 Mbps

Pulse R4005 (619) 674-8100

Status and Control Register List

Nomenclature

"Reserved" register bits, if written, should always be written "0"

R/W = register may be read and written via the utility bus

R-only or W-only = register is read-only or write-only

sticky = register bit is cleared after the register containing it is read;
all sticky bits are read-only

"0" = 'cleared' or 'not set'

"1" = 'set'

Master Control Register

Address: 0x00

Bit	Type	Initial State	Function
7	R/W	0 = OSC multiplied by one	Clock Multiplier Controls whether or not the OSC reference clock input is multiplied by two to generate the line clock. Cleared (0) = OSC is multiplied by 1 to generate line clock Set (1) = OSC is multiplied by 2 to generate line clock
6	R/W	1 = discard errored cells	Discard Receive Error Cells On receipt of any cell with an error (e.g. short cell, invalid command mnemonic, receive HEC error (if enabled)), this cell will be discarded and will not enter the receive FIFO.
5	R/W	0 = all interrupts	Enable Cell Error Interrupts Only If Bit 0 in this register is set (Interrupts Enabled), setting of this bit enables only "Received Cell Error" (as defined in bit 6) to trigger interrupt line.
4	R/W	0 = disabled	Transmit Data Parity Check Directs TC to check parity of TxDATA against parity bit located in TXPARITY.
3	R/W	1 = discard idle cells	Discard Received Idle Cells Directs TC to discard received idle (VPI/VCI = 0 and GFC = 0) cells from PMD without signalling external systems.
2	R/W	0 = not halted	Halt Tx Halts transmission of data from TC to PMD and forces the TxD outputs to the "0" state.
1	R/W	0	Reserved
0	R/W	1 = enable interrupts	Enable Interrupt Pin (Interrupt Mask Bit) Enables the INT output pin. If cleared, pin is always high and interrupt is masked. If set, an interrupt will be signaled by setting the interrupt pin to "0". It doesn't affect the Interrupt Status Registers.

Interrupt Status Register

Address:0x01

Bit	Type	Initial State	Function
7		0	Reserved
6	R	0 = Bad Signal	Good Signal Bit See definitions earlier in this data sheet. 1 - Good Signal 0 - Bad Signal
5	sticky	0	HEC error cell received Set when a HEC error is detected on received cell.
4	sticky	0	"Short Cell" Received Interrupt signal which flags received cells with fewer than 53 bytes. This condition is detected when receiving Start-of-Cell command bytes with fewer than 53 bytes between them.
3	sticky	0	Transmit Parity Error If Bit 4 of the Master Control Register (Transmit Data Parity Check) is set, this interrupt flags a transmit data parity error condition. Odd parity is used.
2	sticky	0	Receive Signal Condition change This interrupt is set when the received 'signal' changes either from 'bad to good' or from 'good to bad'.
1	sticky	0	Received Symbol Error Set when an undefined 5-bit symbol is received.
0	sticky	0	Receive FIFO Overflow Interrupt which indicates when the receive FIFO has filled and cannot accept additional data.

Diagnostic Control Register

Address:0x02

Bit	Type	Initial State	Function
7	R/W	0 = normal	Force TxCLAV Deassert This feature can be used during line loopback mode to prevent cells from being passed across the Utopia bus for transmission.
6	R/W	0	Reserved
5	R/W	1	Reserved
4	R/W	0 = normal	RFLUSH = Clear Receive FIFO This signal is used to tell the TC to flush (clear) all data in the receive FIFO. The TC signals this completion by clearing this bit.
3	R/W	0 = normal	Insert Transmit Payload Error Tells TC to insert cell payload errors in transmitted cells. This can be used to test error detection and recovery systems at destination station, or, under loopback control, at the local receiving station. This payload error is accomplished by flipping bit 0 of the last cell payload byte.
2	R/W	0 = normal	Insert Transmit HEC Error Tells TC to insert HEC error in Byte 5 of transmitted cells. This can be used to test error detection and recovery systems in downstream switches, or, under loopback control, the local receiving station. The HEC error is accomplished by flipping bit 0 of the HEC byte.
1, 0	R/W	00 = normal	Loopback Control bit # 1 0 0 0 Normal mode (receive from network) 1 0 PHY Loopback 1 1 Line Loopback

LED Driver and HEC Status/Control Registers

Address: 0x03

Bit	Type	Initial State	Function																				
7	R	0	Reserved																				
6	R/W	0 = enable checking	Disable Receive HEC Checking (HEC Enable) When not set, the HEC is calculated on first 4 bytes of received cell, and compared against the 5th byte. When set (= 1), the HEC byte is not checked.																				
5	R/W	0 = enable calculate & replace	Disable Transmit HEC Calculate & Replace When set, the 5th header byte of cells queued for transmit is not replaced with the HEC calculated across the first four bytes of that cell.																				
4,3	R/W	00 = 1 cycle	RxREF Pulse Width Select <table> <tr> <th>bit #</th><th>4</th><th>3</th><th></th></tr> <tr> <td>0</td><td>0</td><td>0</td><td>RxREF active for 1 cycle of the recovered clock</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>RxREF active for 2 cycles of the recovered clock</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>RxREF active for 4 cycles of the recovered clock</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>RxREF active for 8 cycles of the recovered clock</td></tr> </table>	bit #	4	3		0	0	0	RxREF active for 1 cycle of the recovered clock	0	1	1	RxREF active for 2 cycles of the recovered clock	1	0	0	RxREF active for 4 cycles of the recovered clock	1	1	1	RxREF active for 8 cycles of the recovered clock
bit #	4	3																					
0	0	0	RxREF active for 1 cycle of the recovered clock																				
0	1	1	RxREF active for 2 cycles of the recovered clock																				
1	0	0	RxREF active for 4 cycles of the recovered clock																				
1	1	1	RxREF active for 8 cycles of the recovered clock																				
2	R	1 = empty	Transmit FIFO Status 1 = TxFIFO empty 0 = TxFIFO not empty																				
1	R	1	TxLED Status 0 = Cell Transmitted 1 = Cell Not Transmitted																				
0	R	1	RxLED Status 0 = Cell Received 1 = Cell Not Received																				

Low Byte Counter Register [7:0]

Address: 0x04

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides low-byte of counter value selected via the Counter Select Register.

High Byte Counter Register [15:8]

Address: 0x05

Bit	Type	Initial State	Function
[7:0]	R	0x00	Provides high-byte of counter value selected via the Counter Select Register.

Counter Select Register

Address: 0x06

Bit	Type	Initial State	Function
7	—	0	Reserved
6	—	0	Reserved
5	—	0	Reserved
4	—	0	Reserved
3	W	0	Symbol Error Counter
2	W	0	TxCell Counter
1	W	0	RxCell Counter Does not count HEC errored cells, even when bit 6 of the Master Control Register is cleared.
0	W	0	Receive HEC Error Counter

Note: For proper operation, only one bit may be set in the Counter Select Register at any time.

Interrupt Mask Register

Address: 0x07

Bit	Type	Initial State	Function
7		0	Reserved
6		0	Reserved
5	R/W	0 = interrupt enabled	HEC Error Cell.
4	R/W	0 = interrupt enabled	Short Cell Error.
3	R/W	0 = interrupt enabled	Transmit Parity Error.
2	R/W	0 = interrupt enabled	Receive Signal Condition Change.
1	R/W	0 = interrupt enabled	Received Cell Symbol Error.
0	R/W	0 = interrupt enabled	Receive FIFO Overflow.

Note: When set to "1", these bits mask the corresponding interrupts going to the interrupt pin (INT). When set to "0", the interrupts are unmasked. These interrupts correspond to the interrupt status bits in the Interrupt Status Registers.

Enhanced Control Register

Address: 0x08

Bit	Type	Initial State	Function
7	W	0 = not reset	Software Reset 1 = Reset. This bit is self-clearing; it isn't necessary to write ""0"" to exit reset.
6	R/W	0 = OSC	Transmit Line Clock (or Loop Timing Mode) When set to 0, the OSC input is used as the transmit line clock. When set to 1, the recovered receive clock is used as the transmit line clock.
5	R/W	0	Reserved
4-0	R/W	00000	Utopia Port Address These bits determine the 5-bit address of the Utopia port for both receive and transmit.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +5.5	V
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +120	°C
IOUT	DC Output Current	50	mA

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Digital Supply Voltage	3.0	3.3	3.6	V
GND	Digital Ground Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	5.25	V
VIL	Input Low Voltage	-0.3	—	0.8	V
AVDD	Analog Supply Voltage	3.0	3.3	3.6	V
AGND	Analog Ground Voltage	0	0	0	V
VDIF	VDD - AVDD	-0.5	0	0.5	V

Recommended Operating Temperature and Supply Voltage

Grade	Ambiant Temperature	GND, AGND	VDD, AVDD
Commercial	0°C to +70°C	0V	3.3V ± 0.3V
Industrial	-40°C to +85°C	0V	3.3V ± 0.3V

Capacitance (TA = +25°C, f = 1MHz)

Symbol	Parameter	Conditions	Max	Unit
C _{IN} ¹	Input Capacitance	V _{IN} = 0V	10	pF
C _{IO} ¹	I/O Capacitance	V _{OUT} = 0V	10	pF

¹ Characterized values, not currently tested.

DC Electrical Characteristics (All Pins except TXD+/- and RXD+/-)

Symbol	Parameter	Test Conditions	Min	Max	Unit
I _{LI}	Input Leakage Current (TxADDR, RxADDR, M0, DA)	Gnd ≤ V _{IN} ≤ VDD	-60	60	μA
	Input Leakage Current (all other input signals)	Gnd ≤ V _{IN} ≤ VDD	-5	5	μA
V _{OH} ¹	Output Logic "1" Voltage	I _{OH} = -2mA, VDD = min.	2.4	—	V
V _{OH} ²	Output Logic "1" Voltage	I _{OH} = -8mA, VDD = min.	2.4	—	V
V _{OL} ³	Output Logic "0" Voltage	I _{OL} = 8mA, VDD = min.	—	0.4	V
I _{DD} ^{4, 5}	Digital Power Supply Current (VDD pins)	OSC = 32 MHz, all outputs unloaded	—	45	mA
		OSC = 64 MHz, all outputs unloaded	—	80	mA
I _{DD} ⁵	Analog Power Supply Current (AVDD pins)	OSC = 32 MHz, all outputs unloaded	—	40	mA
		OSC = 64 MHz, all outputs unloaded	—	55	mA

¹ For AD[7:0] pins only.

² For all output pins except AD[7:0], INT and TXD+/-.

³ For all output pins except TXD+/-.

⁴ Add 15mA when TXD+/- are driving a load

⁵ Total supply current is the sum of I_{DD}1 and I_{DD}2

DC Electrical Characteristics (TXD+/- Output Pins Only)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V _{OH}	Output Logic High Voltage	I _{OH} = -20mA	VDD - 0.5V	—	V
V _{OL}	Output Logic Low Voltage	I _{OL} = 20mA	—	0.5	V

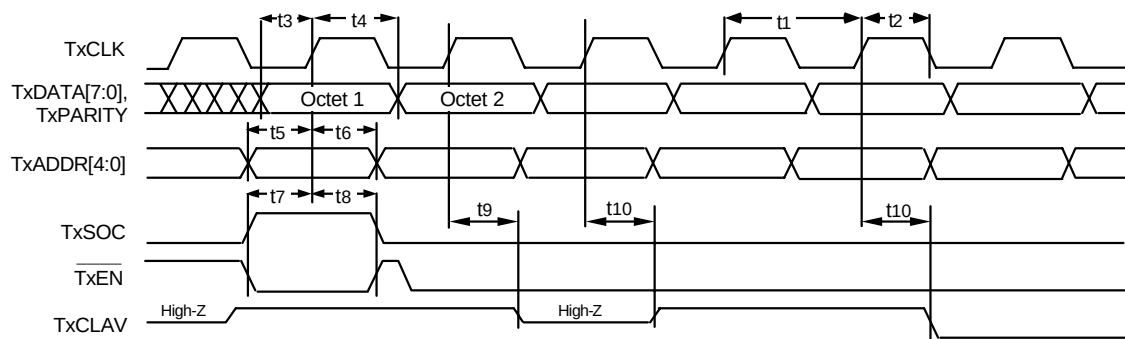
DC Electrical Characteristics (RXD+/- Input Pins Only)

Symbol	Parameter	Min	Typ	Max	Unit
V _{IR}	RXD+/- input voltage range	0	—	VDD	V
V _{IP}	RXD+/- input peak-to-peak differential voltage	0.6	—	2*VDD	V
V _{ICM}	RXD+/- input common mode voltage	1.0	VDD/2	VDD-0.5	V

UTOPIA Bus Timing Parameters

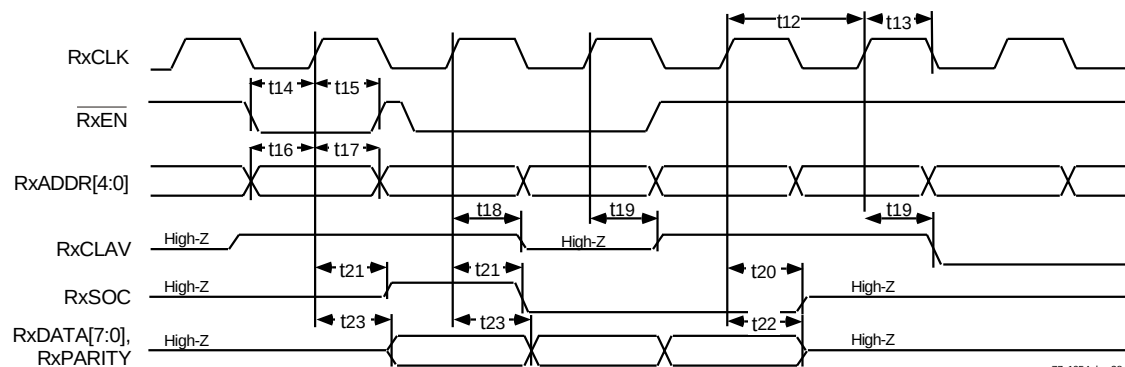
Symbol	Parameter	Min	Max	Unit
t ₁	TxCLK Frequency	0.2	50	MHz
t ₂	TxCLK Duty Cycle (% of t ₁)	40	60	%
t ₃	TxDATA[7:0], TxPARITY Setup Time to TxCLK	4	—	ns

Symbol	Parameter	Min	Max	Unit
t4	TxDATA[7:0], TxPARITY Hold Time to TxCLK	1.5	—	ns
t5	TxADDR[4:0], Setup Time to TxCLK	4	—	ns
t6	TxADDR[4:0], Hold Time to TxCLK	1.5	—	ns
t7	TxSOC, TxEN Setup Time to TxCLK	4	—	ns
t8	TxSOC, TxEN Hold Time to TxCLK	1.5	—	ns
t9	TxCLK to TxCLAV High-Z	2	10	ns
t10	TxCLK to TxCLAV Low-Z (min) and Valid (max)	2	10	ns
t12	RxCLK Frequency	0.2	50	MHz
t13	RxCLK Duty Cycle (% of t12)	40	60	ns
t14	RxEN Setup Time to RxCLK	4	—	ns
t15	RxEN Hold Time to RxCLK	1.5	—	ns
t16	RxADDR[4:0] Setup Time to RxCLK	4	—	ns
t17	RxADDR[4:0] Hold Time to RxCLK	1.5	—	ns
t18	RxCLK to RxCLAV High-Z	2	10	ns
t19	RxCLK to RxCLAV Low-Z (min) and Valid (max)	2	10	ns
t20	RxCLK to RxSOC High-Z	2	10	ns
t21	RxCLK to RxSOC Low-Z (min) and Valid (max)	2	10	ns
t22	RxCLK to RxDATA, RxPARITY High-Z	2	10	ns
t23	RxCLK to RxDATA, RxPARITY Low-Z (min) and Valid (max)	2	10	ns



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Figure 16 UTOPIA Transmit Timing Waveforms



77v1054 drw 38

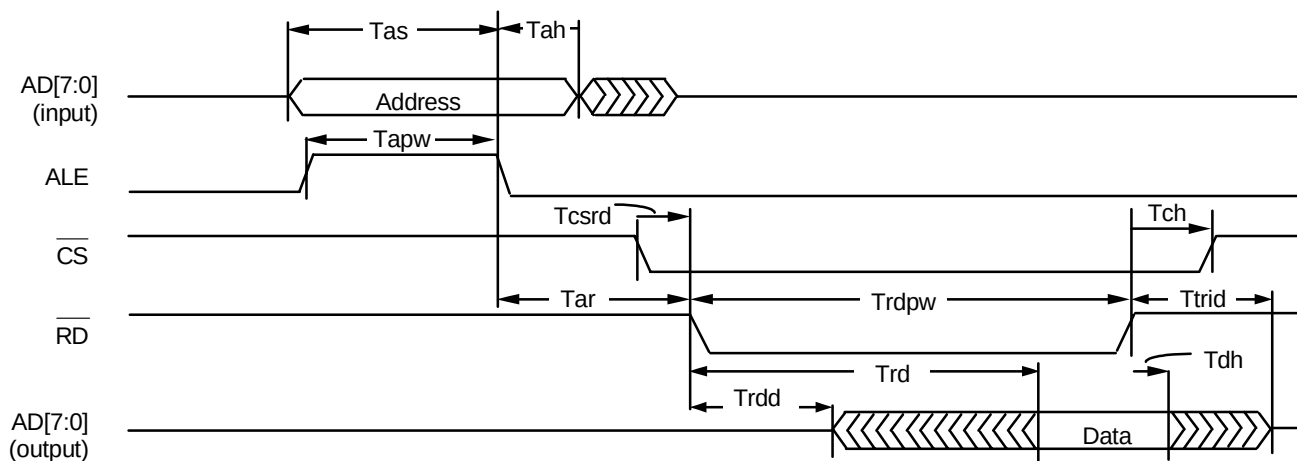
Figure 17 UTOPIA Receive Timing Waveform

Utility Bus Read Cycle

Name	Min	Max	Unit	Description
Tas	10	—	ns	Address setup to ALE
Tcsrd	0	—	ns	Chip select to read enable
Tah	5	—	ns	Address hold to ALE
Tapw	10	—	ns	ALE min pulse width
Ttria	—	0	ns	Address tri-state to $\overline{\text{RD}}$ assert
Trdpw	20	—	ns	Min. $\overline{\text{RD}}$ pulse width
Tdh	0	—	ns	Data Valid hold time
Tch	0	—	ns	$\overline{\text{RD}}$ deassert to $\overline{\text{CS}}$ deassert
Ttrid	—	10	ns	$\overline{\text{RD}}$ deassert to data tri-state
Trd	—	18	ns	Read Data access
Tar	5	—	ns	ALE low to start of read
Trdd	0	—	ns	Start of read to Data low-Z

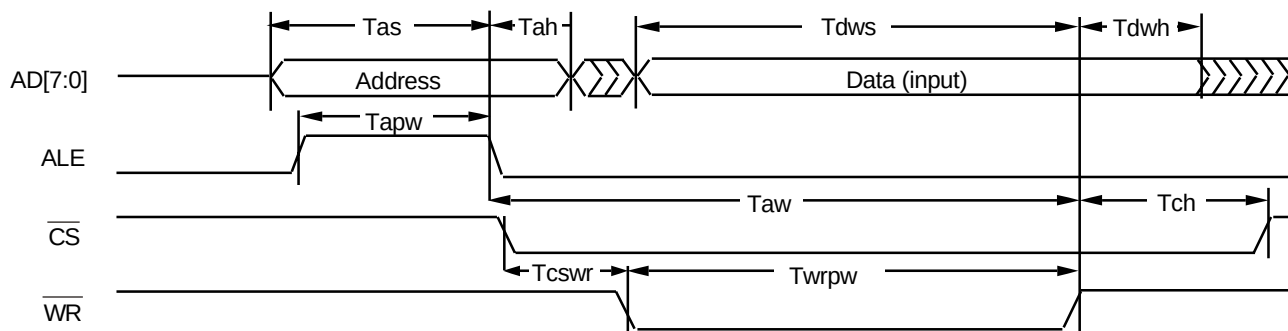
Utility Bus Write Cycle

Name	Min	Max	Unit	Description
Tapw	10	—	ns	ALE min pulse width
Tas	10	—	ns	Address set up to ALE
Tah	5	—	ns	Address hold time to ALE
Tacswr	0	—	ns	$\overline{\text{CS}}$ Assert to $\overline{\text{WR}}$
Twrpw	20	—	ns	Min. $\overline{\text{WR}}$ pulse width
Tdws	20	—	ns	Write Data set up
Tdwh	10	—	ns	Write Data hold time
Tch	0	—	ns	$\overline{\text{WR}}$ deassert to $\overline{\text{CS}}$ deassert
Taw	20	—	ns	ALE low to end of write



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Figure 18 Utility Bus Read Cycle

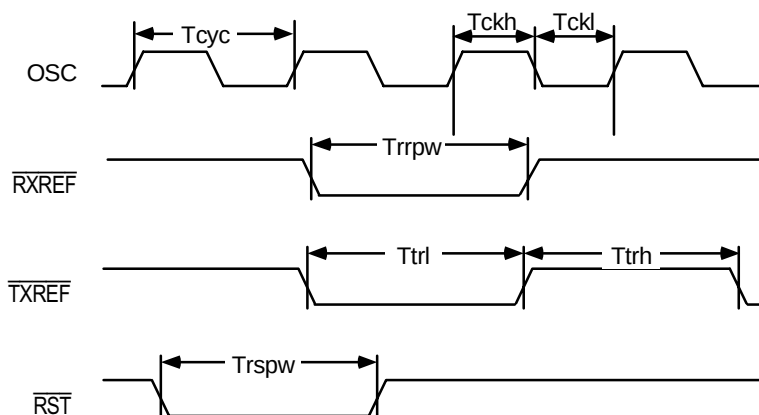


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Figure 19 Utility Bus Write Cycle

OSC, TXREF and Reset Timing

Symbol	Parameter	Min	Typ	Max	Unit
Tcyc	OSC cycle period (25.6 Mbps) (51.2 Mbps)	30 15	31.25 15.625	33 16.5	ns ns
Tckh	OSC high time	40	—	60	%
Tckl	OSC low time	40	—	60	%
Tcc	OSC cycle to cycle period variation	—	—	1	%
Ttrh	TXREF High Time	35	—	—	ns
Ttrl	TXREF Low Time	35	—	—	ns
Trspw	Minimum RST Pulse Width	two OSC cycles	—	—	—
Trrpw	TXREF Pulse Width (For default setting in register 0x03 and 25.6 mbps. Can be programmed for multiples of this amount.)	0.9	1 (31.25ns)	1.1	Receive Data Bit Period

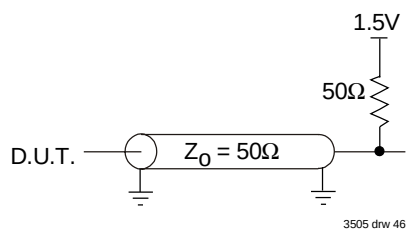


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Figure 20 OSC, TXREF and Reset Timing

AC Test Conditions

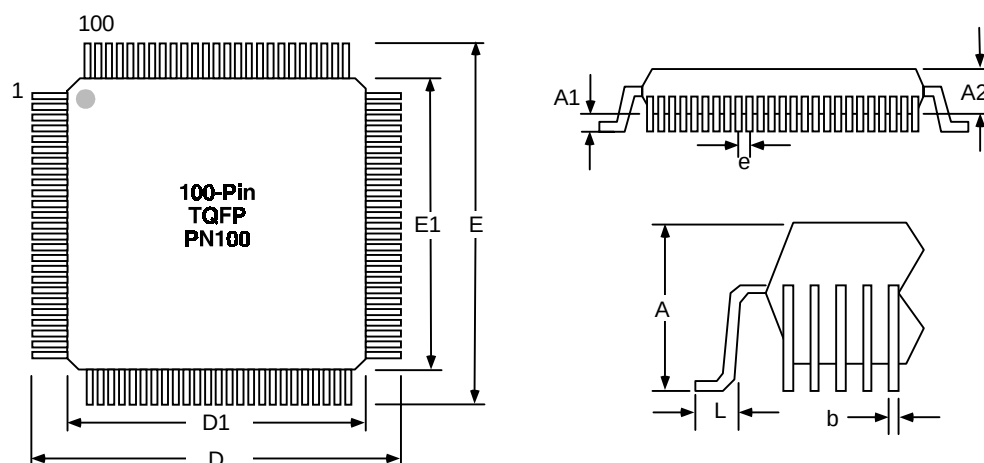
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 21



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Figure 21 Output Test Load

Package Drawing



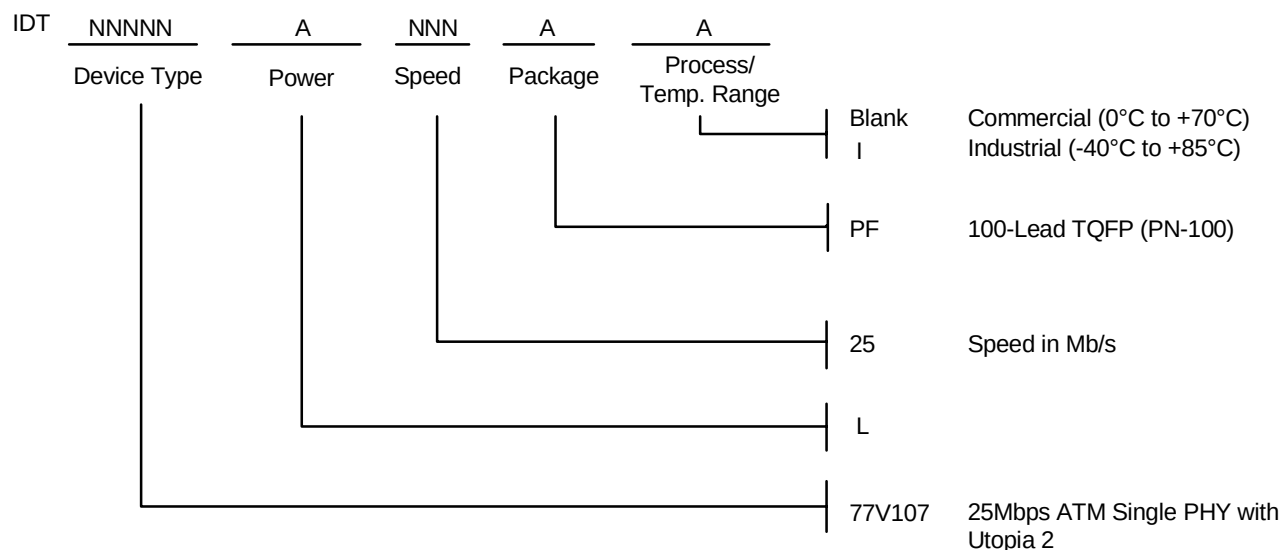
SYMBOL	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	-	16.00	-
D1	-	14.00	-
E	-	16.00	-
E1	-	14.00	-
L	0.45	-	0.75
e	-	0.50	-
b	0.17	0.22	0.27

Dimensions are in millimeters

For the complete package drawing, see PSC4036.pdf in the packaging section of the IDT web site.

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Ordering Information



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Revision History

1/20/2000:	ADVANCE INFORMATION. Initial release.
2/18/2000	PRELIMINARY. Initial release.
1/4/2001	FINAL. DPI interface option removed, package drawing added, power consumption and Utopia timing limits improved. Corrections to Diagnostic Control Register. Description added of symbol framing hunt logic. Corrections to resistor values on "Recommended Connection to Magnetics" on pages 14 and 15.
4/19/01	Added RXREF waveform and pulse width information in Figure 20.
7/03/01	Corrected 0x03 address register name on page 17 to read "LED Driver and HEC Status/Control Registers."


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