72Mb M-die DDRII SRAM Specification

165 FBGA with Pb & Pb-Free

(RoHS compliant)

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Document Title

2Mx36-bit, 4Mx18-bit DDRII CIO b2 SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	1. Initial document.	Mar. 9, 2003	Advance
0.1	1. Correct the JTAG ID register definition 2. Correct the AC timing parameter (delete the tKHK̄H Max value)	Mar. 20, 2003	Preliminary
0.2	1. Add the Power-on Sequence specification	Aug. 16, 2004	Preliminary
0.3	1. Correct the pin name table	Oct. 18, 2004	Preliminary
0.4	1. Update the power consumption (Icc & Isb)	May. 17, 2005	Preliminary
1.0	1. Finalize the datasheet	Aug. 2, 2005	Final

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2Mx36-bit, 4Mx18-bit DDRII CIO b2 SRAM

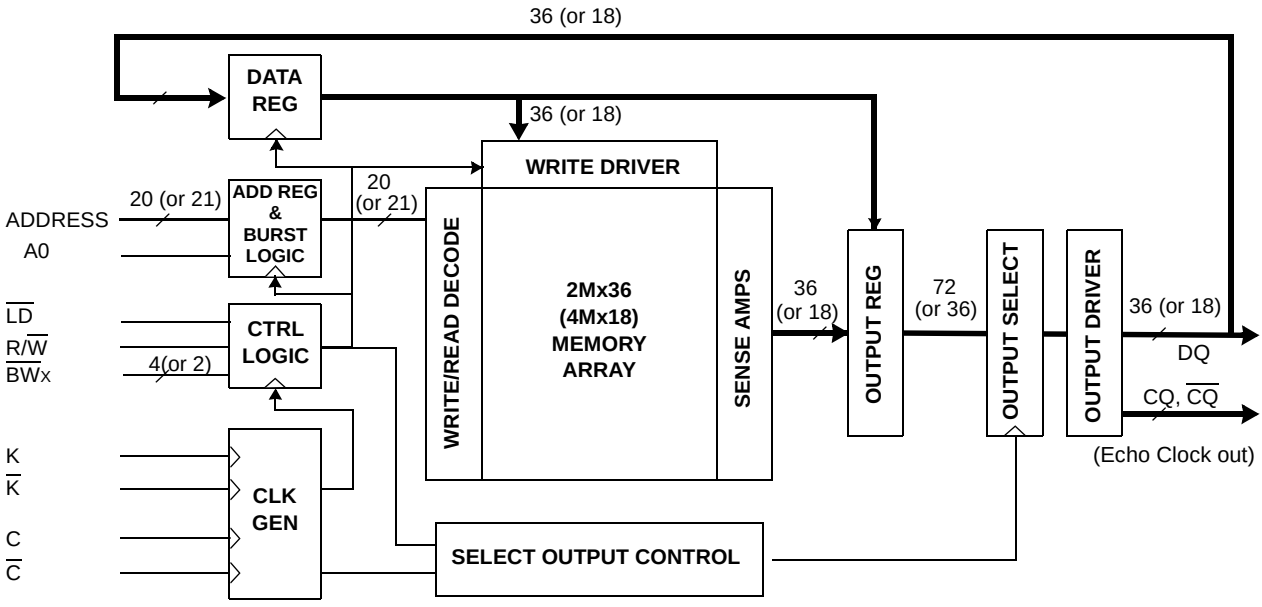
FEATURES

- 1.8V+0.1V/-0.1V Power Supply.
- DLL circuitry for wide output data valid window and future freguency scaling.
- I/O Supply Voltage 1.5V+0.1V/-0.1V for 1.5V I/O, 1.8V+0.1V/-0.1V for 1.8V I/O.
- Pipelined, double-data rate operation.
- Common data input/output bus .
- HSTL I/O
- Full data coherency, providing most current data.
- Synchronous pipeline read with self timed late write.
- Registered address, control and data input/output.
- DDR(Double Data Rate) Interface on read and write ports.
- Fixed 2-bit burst for both read and write operation.
- Clock-stop supports to reduce current.
- Two input clocks(K and $\overline{K}$) for accurate DDR timing at clock rising edges only.
- Two input clocks for output data(C and $\overline{C}$) to minimize clock-skew and flight-time mismatches.
- Two echo clocks (CQ and $\overline{CQ}$) to enhance output data traceability.
- Single address bus.
- Byte write function.
- Simple depth expansion with no data contention.
- Programmable output impedance.
- JTAG 1149.1 compatible test access port.
- 165FBGA(11x15 ball aray FBGA) with body size of 15x17mm & Lead Free

Org.	Part Number	Cycle Time	Access Time	Unit
X36	K7I643682M-F(E)C(I)30	3.3	0.45	ns
	K7I643682M-F(E)C(I)25	4.0	0.45	ns
	K7I643682M-F(E)C(I)20	5.0	0.45	ns
	K7I643682M-F(E)C(I)16	6.0	0.50	ns
X18	K7I641882M-F(E)C(I)30	3.3	0.45	ns
	K7I641882M-F(E)C(I)25	4.0	0.45	ns
	K7I641882M-F(E)C(I)20	5.0	0.45	ns
	K7I641882M-F(E)C(I)16	6.0	0.50	ns

* E : Lead Free Package
* I : Industrial Temperature

FUNCTIONAL BLOCK DIAGRAM



Notes: 1. Numbers in ( ) are for x18 device.

PIN CONFIGURATIONS(TOP VIEW) K7I643682M(2Mx36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}/SA*	SA	R/$\overline{W}$	$\overline{BW_2}$	$\overline{K}$	$\overline{BW_1}$	$\overline{LD}$	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{BW_3}$	K	$\overline{BW_0}$	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes : 1. * Checked No Connect(NC) pins are reserved for higher density address, i.e. 2A for 144Mb .
2. $\overline{BW_0}$ controls write to DQ0:DQ8, $\overline{BW_1}$ controls write to DQ9:DQ17, $\overline{BW_2}$ controls write to DQ18:DQ26 and $\overline{BW_3}$ controls write to DQ27:DQ35.

PIN NAME

SYMBOL	PIN NUMBERS	DESCRIPTION	NOTE
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA0	6C	Burst Count Address Inputs	
SA	3A,9A,10A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
DQ0-35	2B,3B,11B,3C,10C,11C,2D,3D,11D,3E,10E,11E,2F,3F 11F,2G,3G,11G,3J,10J,11J,3K,10K,11K,2L,3L,11L 3M,10M,11M,2N,3N,11N,3P,10P,11P	Data Inputs Outputs	
R/$\overline{W}$	4A	Read, Write Control Pin, Read active when high	
$\overline{LD}$	8A	Synchronous Load Pin, bus Cycle sequence is to be defined when low	
$\overline{BW_0}$, $\overline{BW_1}$,$\overline{BW_2}$, $\overline{BW_3}$	7B,7A,5A,5B	Block Write Control Pin,active when low	
V_{REF}	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V_{DD}	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
V_{SS}	2A,4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L, 4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	1B,9B,10B,1C,2C,9C,1D,9D,10D,1E,2E,9E, 1F,9F,10F,1G,9G,10G,1J,2J,9J,1K,2K,9K 1L,9L,10L,1M,2M,9M,1N,9N,10N,1P,2P,9P	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DD} output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

PIN CONFIGURATIONS(TOP VIEW) K7I641882M(4Mx18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW_1}$	$\overline{K}$	NC	$\overline{LD}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC	K	$\overline{BW_0}$	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

Notes: 1. $\overline{BW_0}$ controls write to DQ0:DQ8 and $\overline{BW_1}$ controls write to DQ9:DQ17.

PIN NAME

SYMBOL	PIN NUMBERS	DESCRIPTION	NOTE
K, $\overline{K}$	6B, 6A	Input Clock	
C, $\overline{C}$	6P, 6R	Input Clock for Output Data	1
CQ, $\overline{CQ}$	11A, 1A	Output Echo Clock	
$\overline{Doff}$	1H	DLL Disable when low	
SA0	6C	Burst Count Address Inputs	
SA	2A,3A,9A,10A,4B,8B,5C,7C,5N-7N,4P,5P,7P,8P,3R-5R,7R-9R	Address Inputs	
DQ0-17	2B,11B,10C,3D,3E,11E,2F,11F,3G,10J,3K,11K,2L,11L 10M,3N,3P,11P	Data Inputs Outputs	
R/$\overline{W}$	4A	Read, Write Control Pin, Read active when high	
$\overline{LD}$	8A	Synchronous Load Pin, bus Cycle sequence is to be defined when low	
$\overline{BW_0}$, $\overline{BW_1}$	7B, 5A	Block Write Control Pin,active when low	
V_{REF}	2H,10H	Input Reference Voltage	
ZQ	11H	Output Driver Impedance Control Input	2
V_{DD}	5F,7F,5G,7G,5H,7H,5J,7J,5K,7K	Power Supply (1.8 V)	
V_{DDQ}	4E,8E,4F,8F,4G,8G,3H,4H,8H,9H,4J,8J,4K,8K,4L,8L	Output Power Supply (1.5V or 1.8V)	
V_{SS}	4C,8C,4D-8D,5E-7E,6F,6G,6H,6J,6K,5L-7L,4M-8M,4N,8N	Ground	
TMS	10R	JTAG Test Mode Select	
TDI	11R	JTAG Test Data Input	
TCK	2R	JTAG Test Clock	
TDO	1R	JTAG Test Data Output	
NC	7A,1B,3B,5B,9B,10B,1C,2C,3C,9C,11C,1D,2D,9D,10D,11D 1E,2E,9E,10E,1F,3F,9F,10F,1G,2G,9G,10G,11G 1J,2J,3J,9J,11J,1K,2K,9K,10K,1L,3L,9L,10L 1M,2M,3M,9M,11M,1N,2N,9N,10N,11N,1P,2P,9P,10P	No Connect	3

Notes: 1. C, $\overline{C}$, K or $\overline{K}$ cannot be set to V_{REF} voltage.
2. When ZQ pin is directly connected to V_{DD} output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. Not connected to chip pad internally.

GENERAL DESCRIPTION

The K7I643682M and K7I641882M are 75,497,472-bits DDR Common I/O Synchronous Pipelined Burst SRAMs.
They are organized as 2,097,152 words by 36bits for K7I643682M and 4,194,304 words by 18 bits for K7I641882M.
Address, data inputs, and all control signals are synchronized to the input clock (K or $\overline{K}$).
Normally data outputs are synchronized to output clocks (C and $\overline{C}$), but when C and $\overline{C}$ are tied high,
the data outputs are synchronized to the input clocks (K and $\overline{K}$).
Read data are referenced to echo clock (CQ or $\overline{CQ}$) outputs.
Read address and write address are registered on rising edges of the input K clocks.
Common address bus is used to access address both for read and write operations.
The internal burst counter is fiexd to 2-bit sequential for both read and write operations.
Synchronous pipeline read and late write enable high speed operations.
Simple depth expansion is accomplished by using $\overline{LD}$ for port selection.
Byte write operation is supported with $\overline{BW_0}$ and $\overline{BW_1}$ ($\overline{BW_2}$ and $\overline{BW_3}$) pins for x18 (x36) device.
IEEE 1149.1 serial boundary scan (JTAG) simplifies monitoriing package pads attachment status with system.
The K7I643682M and K7I641882M are implemented with SAMSUNG's high performance 6T CMOS technology
and is available in 165pin FBGA packages. Multiple power and ground pins minimize ground bounce.

Read Operations

Read cycles are initiated by initiating R/$\overline{W}$ as high at the rising edge of the positive input clock K.
Address is presented and stored in the read address register synchronized with K clock.
For 2-bit burst DDR operation, it will access two 36-bit or 18-bit data words with each read command.
The first pipelined data is transfered out of the device triggered by $\overline{C}$ clock following next $\overline{K}$ clock rising edge.
Next burst data is triggered by the rising edge of following C clock rising edge.
Continuous read operations are initated with K clock rising edge.
And pipelined data are transferred out of device on every rising edge of both C and $\overline{C}$ clocks.
In case C and $\overline{C}$ tied to high, output data are triggered by K and $\overline{K}$ insted of C and $\overline{C}$.
When the $\overline{LD}$ is disabled after a read operation, the K7I643682M and K7I641882M will first complete
burst read operation before entering into deselect mode at the next K clock rising edge.
Then output drivers disabled automatically to high impedance state.

Write Operations

Write cycles are initiated by activating R/$\overline{W}$ as low at the rising edge of the positive input clock K.
Address is presented and stored in the write address register synchronized with next K clock.
For 2-bit burst DDR operation, it will write two 36-bit or 18-bit data words with each write command.
The first "late writed" data is transfered and registered in to the device synchronous with next K clock rising edge.
Next burst data is transfered and registered synchronous with following $\overline{K}$ clock rising edge.
Continuous write operations are initated with K rising edge.
And "late writed" data is presented to the device on every rising edge of both K and $\overline{K}$ clocks.
When the $\overline{LD}$ is disabled, the K7I643682M and K7I641882M will enter into deselect mode.
The device disregards input data presented on the same cycle $\overline{W}$ disabled.
The K7I643682M and K7I641882M support byte write operations.
With activating $\overline{BW_0}$ or $\overline{BW_1}$ ($\overline{BW_2}$ or $\overline{BW_3}$) in write cycle, only one byte of input data is presented.
In K7I641882M, $\overline{BW_0}$ controls write operation to D0:D8, $\overline{BW_1}$ controls write operation to D9:D17.
And in K7I643682M $\overline{BW_2}$ controls write operation to D18:D26, $\overline{BW_3}$ controls write operation to D27:D35.

Single Clock Mode

K7I643682M and K7I641882M can be operated with the single clock pair K and $\overline{K}$, insted of C or $\overline{C}$ for output clocks.
To operate these devices in single clock mode, C and $\overline{C}$ must be tied high during power up
and must be maintained high during operation.
After power up, this device can't change to or from single clock mode.
System flight time and clock skew could not be compensated in this mode.

Depth Expansion

Separate input and output ports enables easy depth expansion.
Each port can be selected and deselected independently and read and write operation do not affect each other.
Before chip deselected, all read and write pending operations are completed.

Programmable Impedance Output Buffer Operation

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to V_{SS} through a precision resistor(RQ).
The value of RQ (within 15%) is five times the output impedance desired.
For example, 250Ω resistor will give an output impedance of 50Ω.
Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles.
In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM.
There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

Echo clock operation

To assure the output tracibility, the SRAM provides the output Echo clock, pair of compliment clock CQ and $\overline{CQ}$,
which are synchronized with internal data output.
Echo clocks run free during normal operation.
The Echo clock is triggered by internal output clock signal, and transfered to external through same structures as output driver.

Clock Consideration

K7I643682M and K7I641882M utlizes internal DLL(Delay-Locked Loops) for maximum output data valid window.
It can be placed into a stopped-clock state to minimize power with a modest restart time of 1024 clock cycles.
Circuitry automatically resets the DLL when absence of input clock is detected.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

K	$\overline{LD}$	R/$\overline{W}$	Q		OPERATION
			Q(A0)	Q(A1)	
Stopped	X	X	Previous state	Previous state	Clock Stop
↑	H	X	High-Z	High-Z	No Operation
↑	L	H	Q_{OUT} at $\overline{C}$(t+1)	Q_{OUT} at C(t+2)	Read
↑	L	L	Din at K(t+1)	Din at $\overline{K}$(t+1)	Write

Notes: 1. X means "Don't Care".

2. The rising edge of clock is symbolized by (↑).

3. Before enter into clock stop status, all pending read and write operations will be completed.

WRITE TRUTH TABLE(x18)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	OPERATION
↑		L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	WRITE BYTE 0 (K↑)
	↑	L	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	WRITE BYTE 1 (K↑)
	↑	H	L	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	WRITE NOTHING (K↑)
	↑	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).

3. Assumes a WRITE cycle was initiated.

4. This table illustates operation for x18 devices.

WRITE TRUTH TABLE(x36)

K	$\overline{K}$	$\overline{BW_0}$	$\overline{BW_1}$	$\overline{BW_2}$	$\overline{BW_3}$	OPERATION
↑		L	L	L	L	WRITE ALL BYTEs (K↑)
	↑	L	L	L	L	WRITE ALL BYTEs ($\overline{K}$↑)
↑		L	H	H	H	WRITE BYTE 0 (K↑)
	↑	L	H	H	H	WRITE BYTE 0 ($\overline{K}$↑)
↑		H	L	H	H	WRITE BYTE 1 (K↑)
	↑	H	L	H	H	WRITE BYTE 1 ($\overline{K}$↑)
↑		H	H	L	L	WRITE BYTE 2 and BYTE 3 (K↑)
	↑	H	H	L	L	WRITE BYTE 2 and BYTE 3 ($\overline{K}$↑)
↑		H	H	H	H	WRITE NOTHING (K↑)
	↑	H	H	H	H	WRITE NOTHING ($\overline{K}$↑)

Notes: 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of input clock K or $\overline{K}$ (↑).

3. Assumes a WRITE cycle was initiated.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to 2.9	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	-0.5 to V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.5 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature (Commercial / Industrial)	T_{OPR}	0 to 70 / -40 to 85	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note:** 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{DDQ} must not exceed V_{DD} during normal operation.

OPERATING CONDITIONS ($0°C \le T_A \le 70°C$)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{DD}	1.7	1.9	V
	V_{DDQ}	1.4	1.9	V
Reference Voltage	V_{REF}	0.68	0.95	V

DC ELECTRICAL CHARACTERISTICS(V_{DD}=1.8V ±0.1V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT	NOTES
Input Leakage Current	I_{IL}	V_{DD}=Max ; V_{IN}=V_{SS} to V_{DDQ}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled,		-2	+2	µA	
Operating Current (x36): QDR mode	I_{CC}	V_{DD}=Max , I_{OUT}=0mA Cycle Time ≥ t_{KHKH} Min	-30	-	900	mA	1,4
			-25	-	800		
			-20	-	700		
			-16		650		
Operating Current (x18): QDR mode	I_{CC}	V_{DD}=Max , I_{OUT}=0mA Cycle Time ≥ t_{KHKH} Min	-30	-	850	mA	1,4
			-25	-	750		
			-20	-	650		
			-16	-	600		
Standby Current(NOP): QDR mode	I_{SB1}	Device deselected, I_{OUT}=0mA, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-30	-	400	mA	1,5
			-25	-	380		
			-20	-	360		
			-16	-	340		
Output High Voltage	V_{OH1}			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	2,6
Output Low Voltage	V_{OL1}			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	2,6
Output High Voltage	V_{OH2}	I_{OH}=-1.0mA		V_{DDQ}-0.2	V_{DDQ}	V	3
Output Low Voltage	V_{OL2}	I_{OL}=1.0mA		V_{SS}	0.2	V	3
Input Low Voltage	V_{IL}			-0.3	V_{REF}-0.1	V	7,8
Input High Voltage	V_{IH}			V_{REF}+0.1	V_{DDQ}+0.3	V	7,9

Notes: 1. Minimum cycle. I_{OUT}=0mA.

2. $|I_{OH}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ for $175\Omega \le RQ \le 350\Omega$. $|I_{OL}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ for $175\Omega \le RQ \le 350\Omega$.
3. Minimum Impedance Mode when ZQ pin is connected to V_{DDQ}.
4. Operating current is calculated with 50% read cycles and 50% write cycles.
5. Standby Current is only after all pending read and write burst opeactions are completed.
6. Programmable Impedance Mode.
7. These are DC test criteria. DC design criteria is V_{REF}±50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
8. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.5V(pulse width ≤ 3ns).
9. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=V_{DDQ}+0.85V(pulse width ≤ 3ns).

AC ELECTRICAL CHARACTERISTICS (V_{DD}=1.8V ±0.1V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input High Voltage	V_{IH} (AC)	V_{REF} + 0.2	-	V	1,2
Input Low Voltage	V_{IL} (AC)	-	V_{REF} - 0.2	V	1,2

Notes: 1. This condition is for AC function test only, not for AC parameter test.
2. To maintain a valid level, the transitioning edge of the input must :
a) Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$
b) Reach at least the target AC level
c) After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$

AC TIMING CHARACTERISTICS(V_{DD}=1.8V±0.1V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	-30		-25		-20		-16		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock Cycle Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKH}	3.30	5.25	4.00	6.30	5.00	7.88	6.00	8.40	ns	
Clock Phase Jitter (K, $\overline{K}$, C, $\overline{C}$)	$t_{KC\ var}$		0.20		0.20		0.20		0.20	ns	5
Clock High Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKL}	1.32		1.60		2.00		2.40		ns	
Clock Low Time (K, $\overline{K}$, C, $\overline{C}$)	t_{KLKH}	1.32		1.60		2.00		2.40		ns	
Clock to $\overline{Clock}$ ($K\uparrow \rightarrow \overline{K}\uparrow, C\uparrow \rightarrow \overline{C}\uparrow$)	$t_{KH\overline{K}H}$	1.49		1.80		2.20		2.70		ns	
Clock to data clock ($K\uparrow \rightarrow C\uparrow, \overline{K}\uparrow \rightarrow \overline{C}\uparrow$)	t_{KHCH}	0.00	1.45	0.00	1.80	0.00	2.30	0.00	2.80	ns	
DLL Lock Time (K, C)	$t_{KC\ lock}$	1024		1024		1024		1024		cycle	6
K Static to DLL reset	$t_{KC\ reset}$	30		30		30		30		ns	
Output Times											
C, $\overline{C}$ High to Output Valid	t_{CHQV}		0.45		0.45		0.45		0.50	ns	3
C, $\overline{C}$ High to Output Hold	t_{CHQX}	-0.45		-0.45		-0.45		-0.50		ns	3
C, $\overline{C}$ High to Echo Clock Valid	t_{CHCQV}		0.45		0.45		0.45		0.50	ns	
C, $\overline{C}$ High to Echo Clock Hold	t_{CHCQX}	-0.45		-0.45		-0.45		-0.50		ns	
CQ, $\overline{CQ}$ High to Output Valid	t_{CQHQV}		0.27		0.30		0.35		0.40	ns	7
CQ, $\overline{CQ}$ High to Output Hold	t_{CQHQX}	-0.27		-0.30		-0.35		-0.40		ns	7
$\overline{C}$, High to Output High-Z	t_{CHQZ}		0.45		0.45		0.45		0.50	ns	3
$\overline{C}$, High to Output Low-Z	t_{CHQX1}	-0.45		-0.45		-0.45		-0.50		ns	3
Setup Times											
Address valid to K rising edge	t_{AVKH}	0.40		0.50		0.60		0.70		ns	
Control inputs valid to K rising edge	t_{IVKH}	0.40		0.50		0.60		0.70		ns	2
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.30		0.35		0.40		0.50		ns	
Hold Times											
K rising edge to address hold	t_{KHAX}	0.40		0.50		0.60		0.70		ns	
K rising edge to control inputs hold	t_{KHIX}	0.40		0.50		0.60		0.70		ns	
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.30		0.35		0.40		0.50		ns	

Notes: 1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control singles are R, W, BW_0, BW_1 and BW_2, BW_3, also for x36
3. If C,$\overline{C}$ are tied high, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature $tCHQX_1$ is bigger than tCHQZ.
The specs as shown do not imply bus contention because $tCHQX_1$ is a MIN parameter that is worst case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter(worst case at 70°C, 1.7V)
It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. Vdd slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
7. Echo clock is very tightly controlled to data valid/data hold. By design, there is a ± 0.1 ns variation from echo clock to data.
The data sheet parameters reflect tester guardbands and test setup variations.

THERMAL RESISTANCE

PRMETER	SYMBOL	Typ	Unit	NOTES
Junction to Ambient	θ_{JA}	21	°C/W	
Junction to Case	θ_{JC}	2.48	°C/W	

Note: Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J = T_A + P_D \times \theta_{JA}$

PIN CAPACITANCE

PRMETER	SYMBOL	TESTCONDITION	TYP	MAX	Unit	NOTES
Address Control Input Capacitance	C_{IN}	V_{IN}=0V	3.5	4	pF	
Input and Output Capacitance	C_{OUT}	V_{OUT}=0V	4	5	pF	
Clock Capacitance	C_{CLK}	-	3	4	pF	

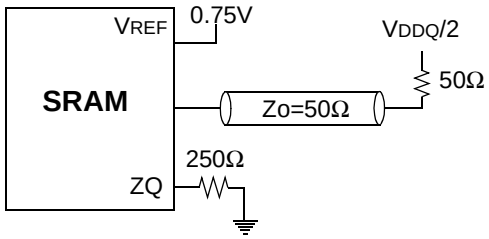
Note: 1. Parameters are tested with RQ=250Ω and V_{DDQ}=1.5V.
2. Periodically sampled and not 100% tested.

AC TEST CONDITIONS

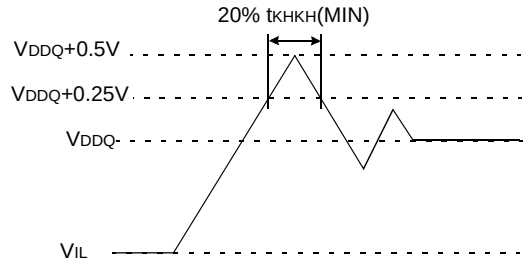
Parameter	Sym-	Value	Unit
Core Power Supply Voltage	V_{DD}	1.7~1.9	V
Output Power Supply Voltage	V_{DDQ}	1.4~1.9	V
Input High/Low Level	V_{IH}/	1.25/0.25	V
Input Reference Level	V_{REF}	0.75	V
Input Rise/Fall Time	T_R/T_F	0.3/0.3	ns
Output Timing Reference Level		V_{DDQ}/2	V

Note: Parameters are tested with RQ=250Ω

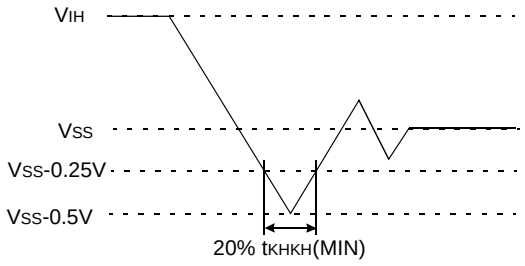
AC TEST OUTPUT LOAD



Overershoot Timing

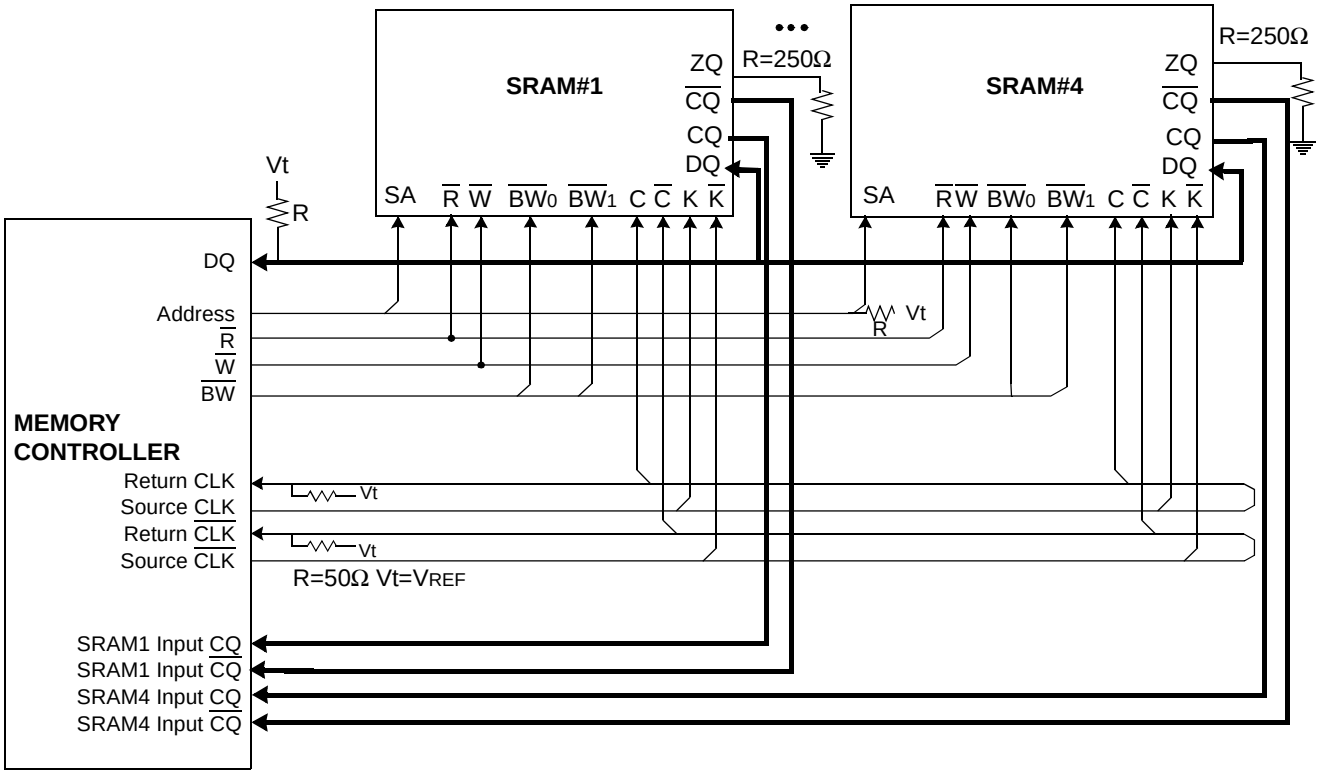


Undershoot Timing

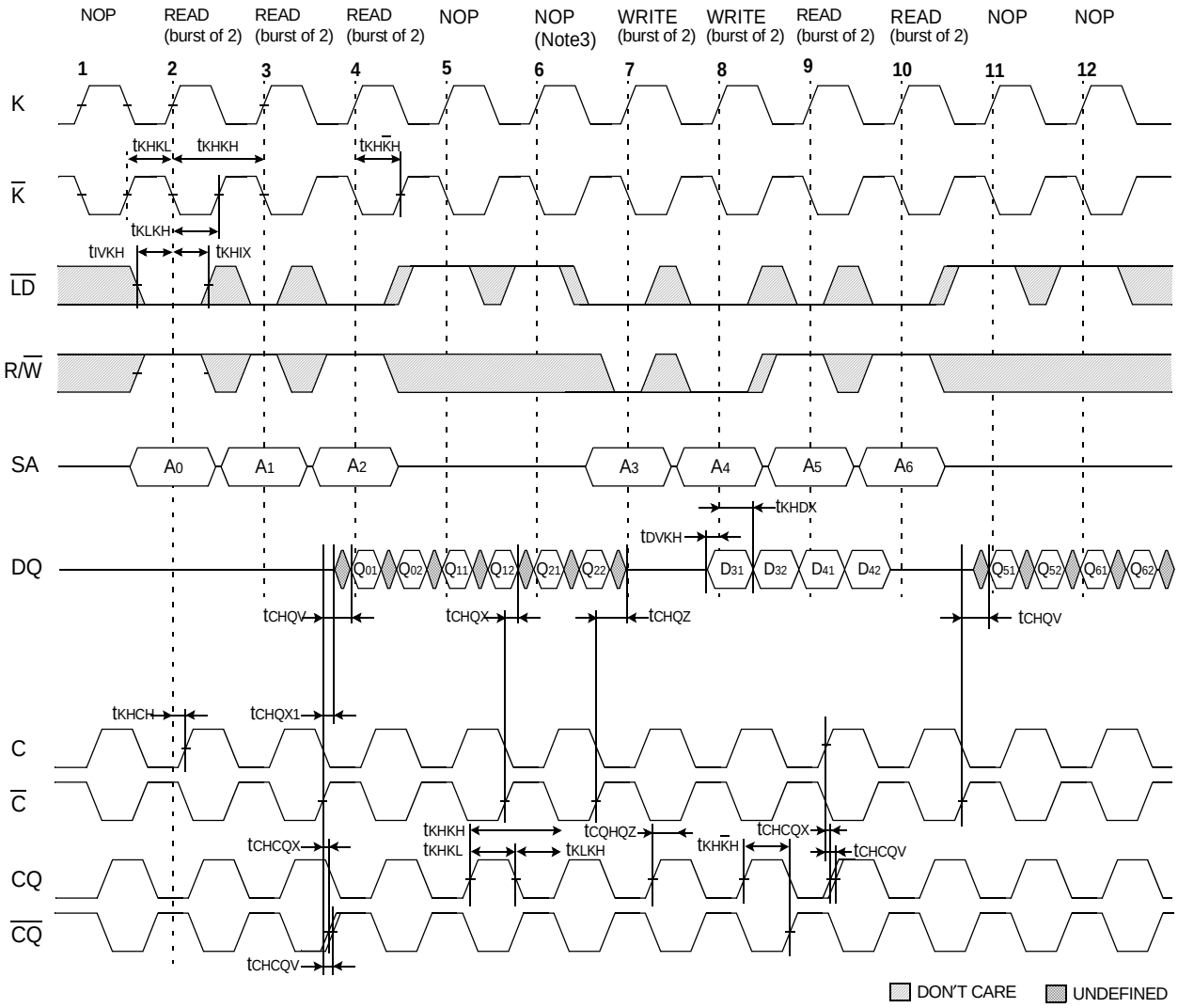


Note: For power-up, $V_{IH} \le V_{DDQ}$+0.3V and $V_{DD} \le$ 1.7V and $V_{DDQ} \le$ 1.4V t ≤ 200ms

APPLICATION INRORMATION



TIMING WAVE FORMS OF READ, WRITE AND NOP



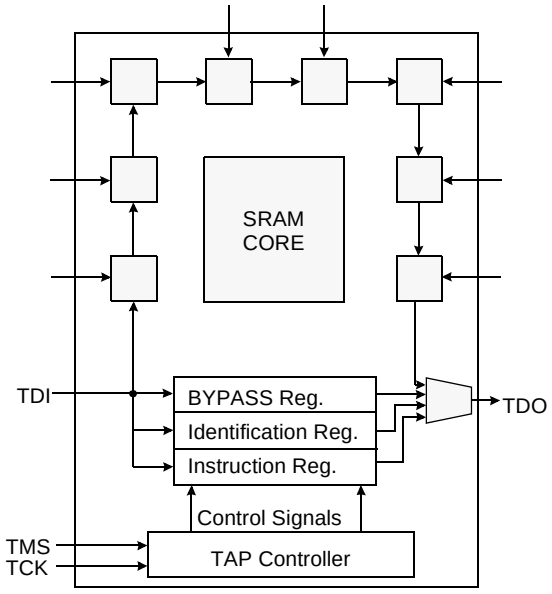
NOTE

1. Q_{01} refers to output from address A. Q_{02} refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after a NOP .
3. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies, it may be required to prevent bus contention.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



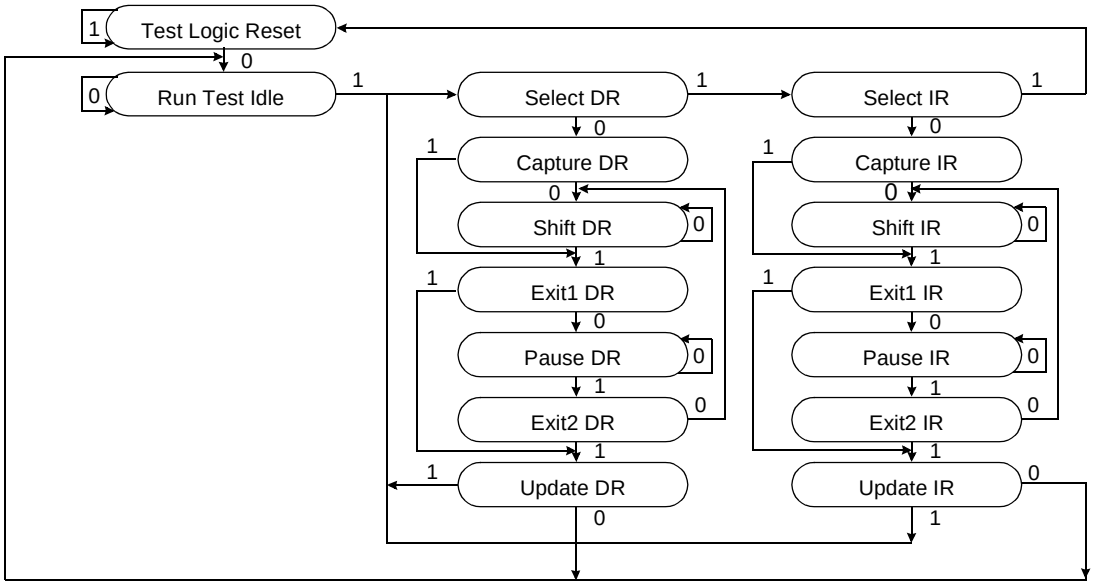
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	RESERVED	Do Not Use	6
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	RESERVED	Do Not Use	6
1	1	1	BYPASS	Bypass Register	4

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
2Mx36	3 bits	1 bit	32 bits	109 bits
4Mx18	3 bits	1 bit	32 bits	109 bits

ID REGISTER DEFINITION

Part	Revision Number (31:29)	Part Configuration (28:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
2Mx36	000	00def0wx0t0q0b0s0	00001001110	1
4Mx18	000	00def0wx0t0q0b0s0	00001001110	1

Note : Part Configuration
/def=011 for 72Mb, /wx=11 for x36, 10 for x18.
/t=1 for DLL Ver., 0 for non-DLL Ver. /q=1 for QDR, 0 for DDR /b=1 for 4Bit Burst, 0 for 2Bit Burst /s=1 for Separate I/O, 0 for Common I/O

BOUNDARY SCAN EXIT ORDER

ORDER	PIN ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

ORDER	PIN ID
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

ORDER	PIN ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Note: 1. NC pins are read as "X" (i.e. don't care.)

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	1.4	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.4	V	

Note: 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

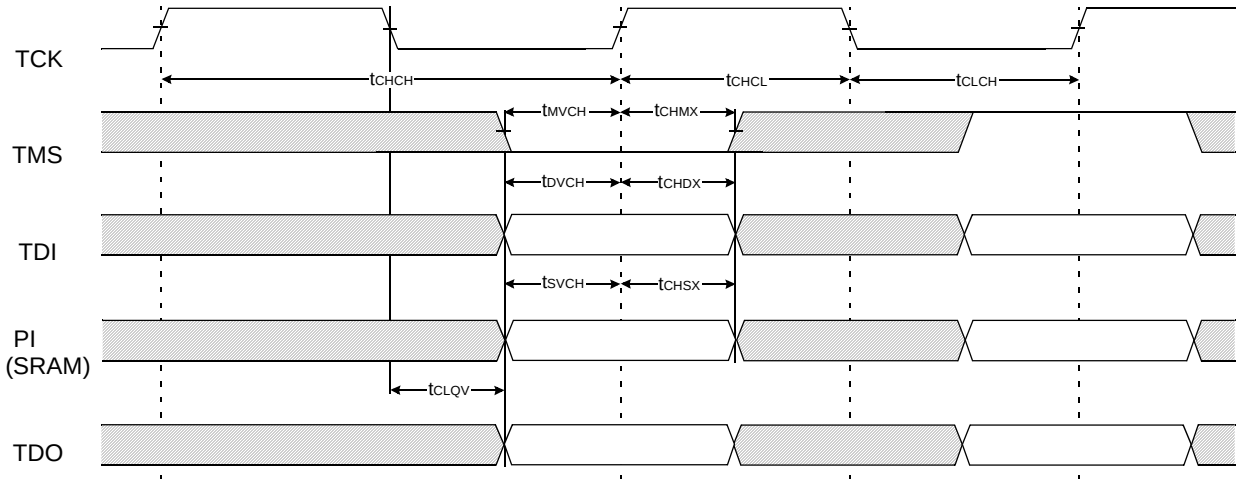
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.3/0.5	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

Note: 1. See SRAM AC test output load on page 11.

JTAG AC Characteristics

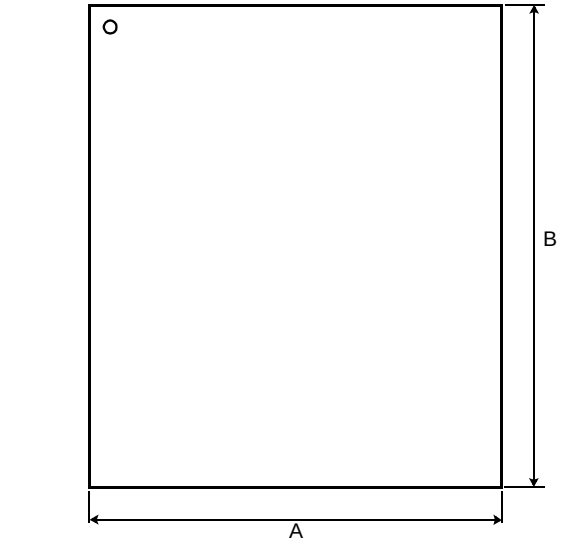
Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM

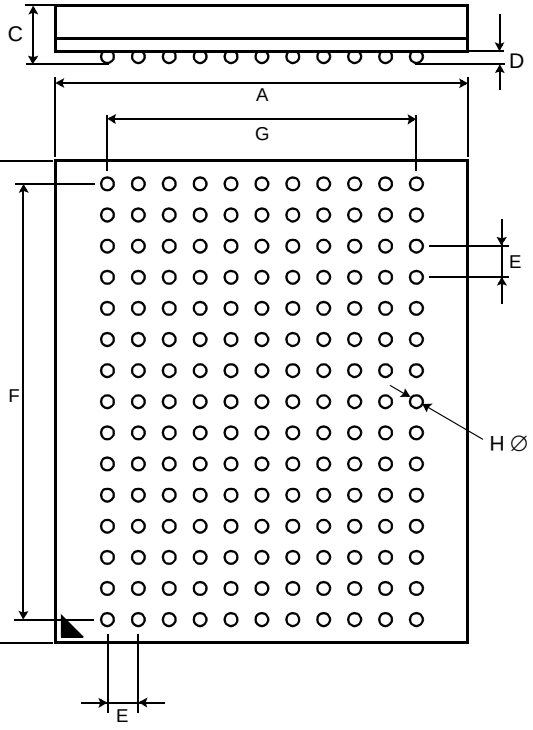


165 FBGA PACKAGE DIMENSIONS

15mm x 17mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Top View



Side View

Bottom View

Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	15 ± 0.1	mm		**E**	1.0	mm	
B	17 ± 0.1	mm		**F**	14.0	mm	
C	1.3 ± 0.1	mm		**G**	10.0	mm	
D	0.35 ± 0.05	mm		**H**	0.5 ± 0.05	mm	