

512 x 8 Registered PROM

Features

- CMOS for optimum speed/power
- High speed
 - 25 ns address set-up
 - 12 ns clock to output
- Low power
 - 495 mW (Commercial)
 - 660 mW (Military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- EPROM technology, 100% programmable
- Slim 300-mil, 24-pin plastic or hermetic DIP, 28-pin LCC, or 28-pin PLCC
- $5V \pm 10\% V_{CC}$, commercial and military
- TTL-compatible I/O

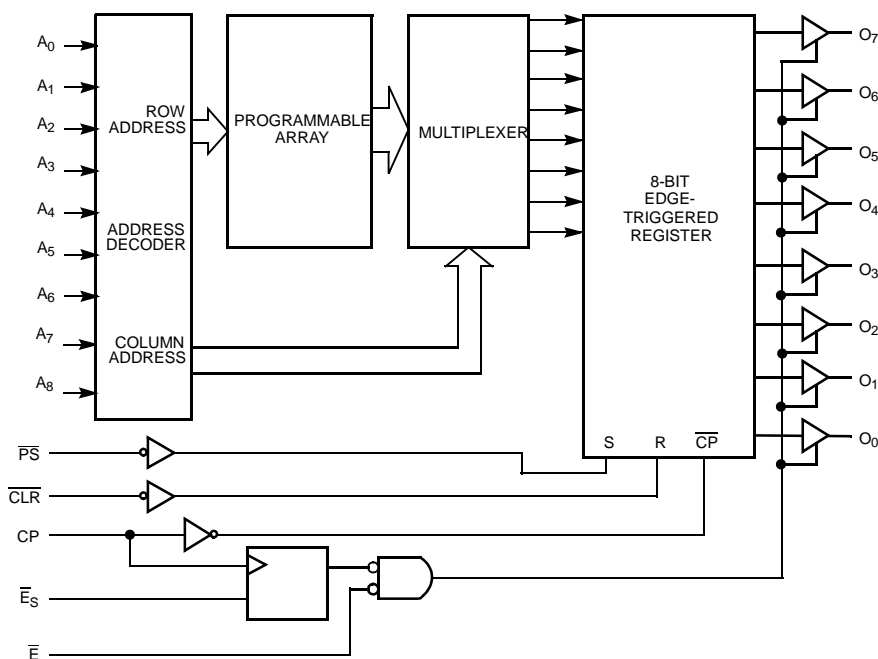
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2001V static discharge

Functional Description

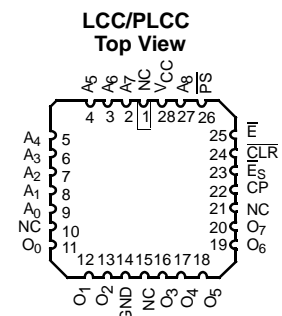
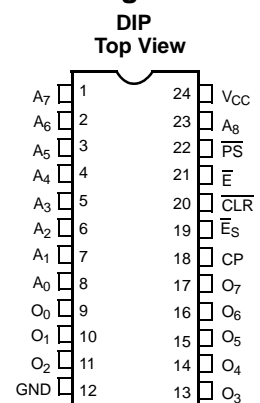
The CY7C225A is a high-performance 512-word by 8-bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, and 28-pin PLCC. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225A replaces bipolar devices and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C225A-25	7C225A-30	7C225A-40	Unit
Minimum Address Set-Up Time		25	30	40	ns
Maximum Clock to Output		12	15	25	ns
Maximum Operating Current	Commercial	90	90		mA
	Military			120	mA

Maximum Ratings^[1]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State -0.5V to +7.0V

DC Input Voltage -3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3,4]

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA V _{IN} = V _{IH} or V _{IL}	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}		0.4	V
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs	2.0		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _{IN} ≤ V _{CC}	-10	+10	μA
V _{CD}	Input Clamp Diode Voltage	Note 4			
I _{OZ}	Output Leakage Current	GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled ^[5]	-10	+10	μA
I _{OS}	Output Short Circuit Current	V _{CC} = Max., V _{OUT} = 0.0V ^[6]	-20	-90	mA
I _{CC}	Power Supply Current	I _{OUT} = 0 mA V _{CC} = Max.		90	mA
		Commercial		120	
V _{PP}	Programming Supply Voltage		12	13	V
I _{PP}	Programming Supply Current			50	mA
V _{IHP}	Input HIGH Programming Voltage		3.0		V
V _{ILP}	Input LOW Programming Voltage			0.4	V

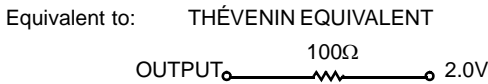
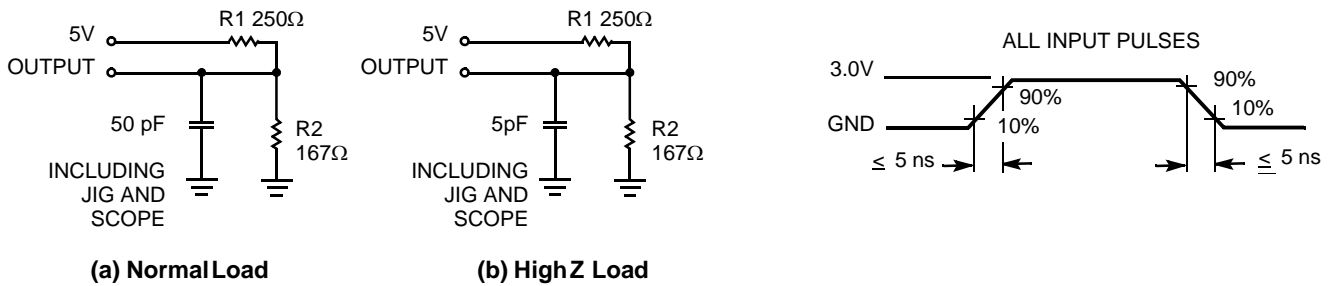
Notes

1. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. See the "Introduction to CMOS PROMs" section of the Cypress Data Book for general information on testing.
5. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
6. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms^[4]



Operating Modes

The CY7C225A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous (\overline{E}_S) and asynchronous (\overline{E}) output enables and \overline{CLEAR} and \overline{PRESET} inputs.

Upon power-up, the synchronous enable (\overline{E}_S) flip-flop will be in the set condition causing the outputs (O_0 – O_7) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address inputs (A_0 – A_8) and a logic LOW to the enable (\overline{E}_S) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0 – O_7) provided the asynchronous enable (\overline{E}) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable (\overline{E}) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of \overline{E} , the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable (\overline{E}_S) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW,

the subsequent positive clock edge will return the output to the active state if \overline{E} is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C225A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

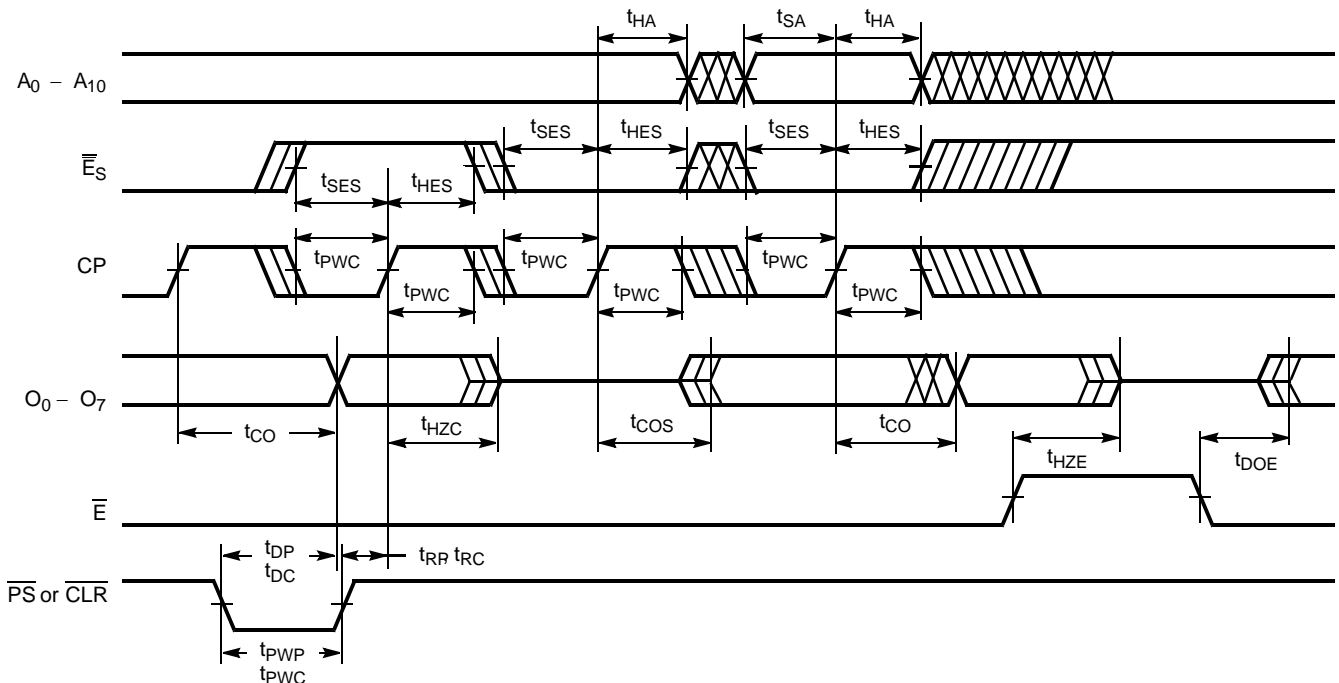
The CY7C225A has buffered asynchronous \overline{CLEAR} and \overline{PRESET} inputs. Applying a LOW to the \overline{PRESET} input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the \overline{CLEAR} input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable (\overline{E}) LOW.

When power is applied, the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the \overline{E}_S input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The \overline{E} input may then be used to enable the outputs.

Switching Characteristics Over the Operating Range^[3,4]

Parameter	Description	7C225A-25		7C225A-30		7C225A-40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Set-Up to Clock HIGH	25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		ns
t_{SES}	\bar{E}_S Set-Up to Clock HIGH	10		10		10		ns
t_{HES}	\bar{E}_S Hold from Clock HIGH	0		5		5		ns
t_{DP}, t_{DC}	Delay from \overline{PRESET} or \overline{CLEAR} to Valid Output		20		20		20	ns
t_{RP}, t_{RC}	\overline{PRESET} or \overline{CLEAR} Recovery to Clock HIGH	15		20		20		ns
t_{PWP}, t_{PWC}	\overline{PRESET} or \overline{CLEAR} Pulse Width	15		20		20		ns
t_{COS}	Valid Output from Clock HIGH ^[7]		20		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH ^[7]		20		20		30	ns
t_{DOE}	Valid Output from \bar{E} LOW		20		20		30	ns
t_{HZE}	Inactive Output from \bar{E} HIGH		20		20		30	ns

Switching Waveforms^[4]



Note

7. Applies only when the synchronous (\bar{E}_S) function is used.

Programming Information

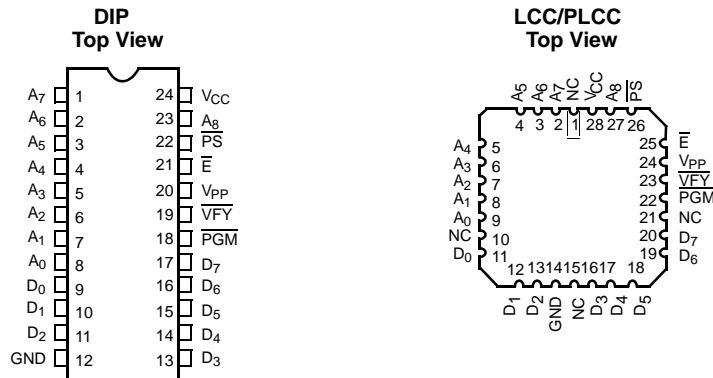
Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed

programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Mode Selection

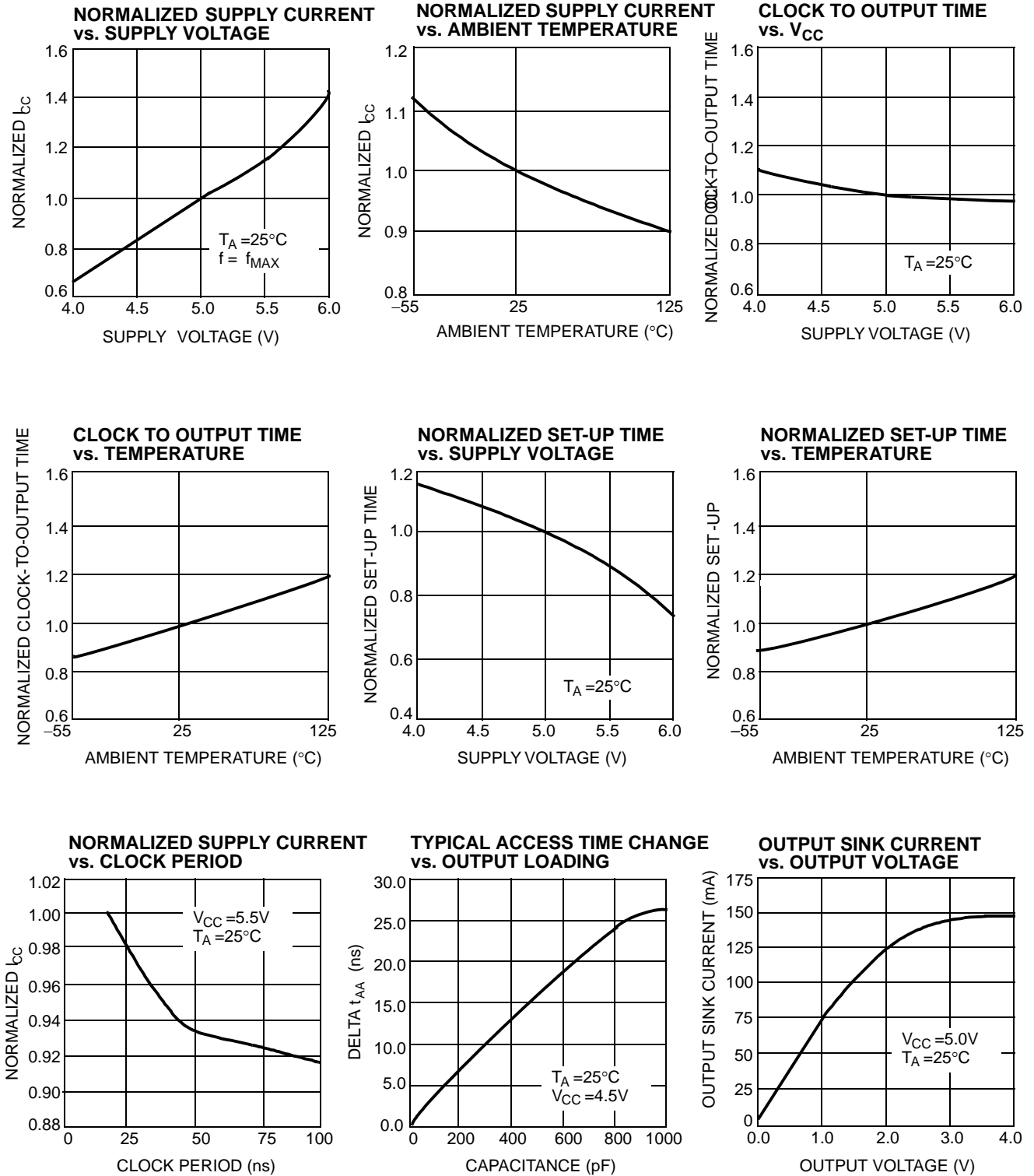
Mode	Pin Function ^[8]							
	Read or Output Disable	A ₈ -A ₀	CP	E _S	CLR	E	PS	O ₇ -O ₀
	Other	A ₈ -A ₀	PGM	VFY	V _{PP}	E	PS	D ₇ -D ₀
Read		A ₈ -A ₀	X	V _{IL}	V _{IH}	V _{IL}	V _{IH}	O ₇ -O ₀
Output Disable		A ₈ -A ₀	X	V _{IH}	V _{IH}	X	V _{IH}	High Z
Output Disable		A ₈ -A ₀	X	X	V _{IH}	V _{IH}	V _{IH}	High Z
Clear		A ₈ -A ₀	X	V _{IL}	V _{IL}	V _{IL}	V _{IH}	Zeros
Preset		A ₈ -A ₀	X	V _{IL}	V _{IH}	V _{IL}	V _{IL}	Ones
Program		A ₈ -A ₀	V _{ILP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	D ₇ -D ₀
Program Verify		A ₈ -A ₀	V _{IHP}	V _{ILP}	V _{PP}	V _{IHP}	V _{IHP}	O ₇ -O ₀
Program Inhibit		A-A ₀	V _{IHP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	High Z
Intelligent Program		A ₈ -A ₀	V _{ILP}	V _{IHP}	V _{PP}	V _{IHP}	V _{IHP}	D ₇ -D ₀
Blank Check		A ₈ -A ₀	V _{IHP}	V _{ILP}	V _{PP}	V _{IHP}	V _{IHP}	Zeros

Figure 1. Programming Pinouts



Note
8. X = "don't care" but not to exceed V_{CC} ±5%.

Typical DC and AC Characteristics



Ordering Information

Speed (ns)		Ordering Code	Package Type	Package Type	Operating Range
t _{SA}	t _{CO}				
25	12	CY7C225A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial

**MILITARY SPECIFICATIONS
Group A Subgroup Testing**

DC Characteristics

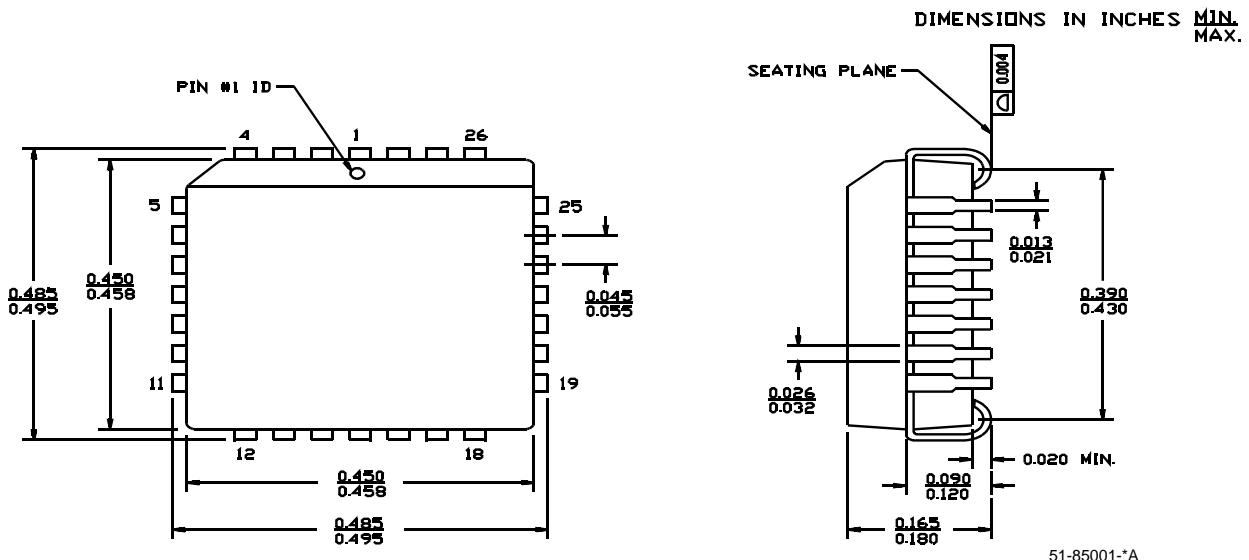
Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11
t _{DP}	7, 8, 9, 10, 11
t _{RP}	7, 8, 9, 10, 11

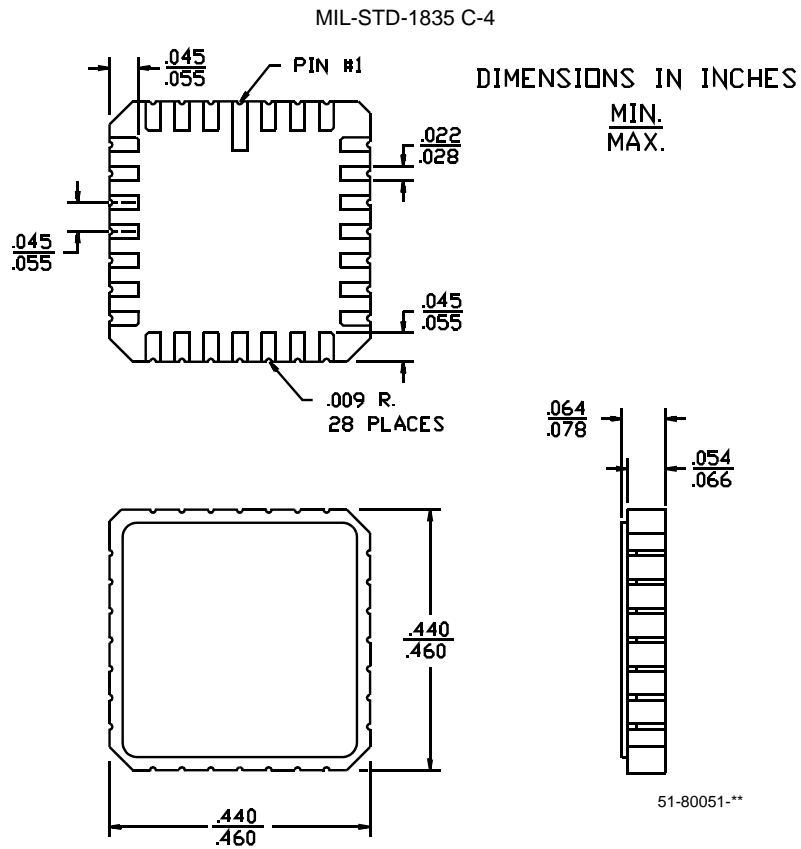
Package Diagrams

Figure 2. 28-Lead Plastic Leaded Chip Carrier J64



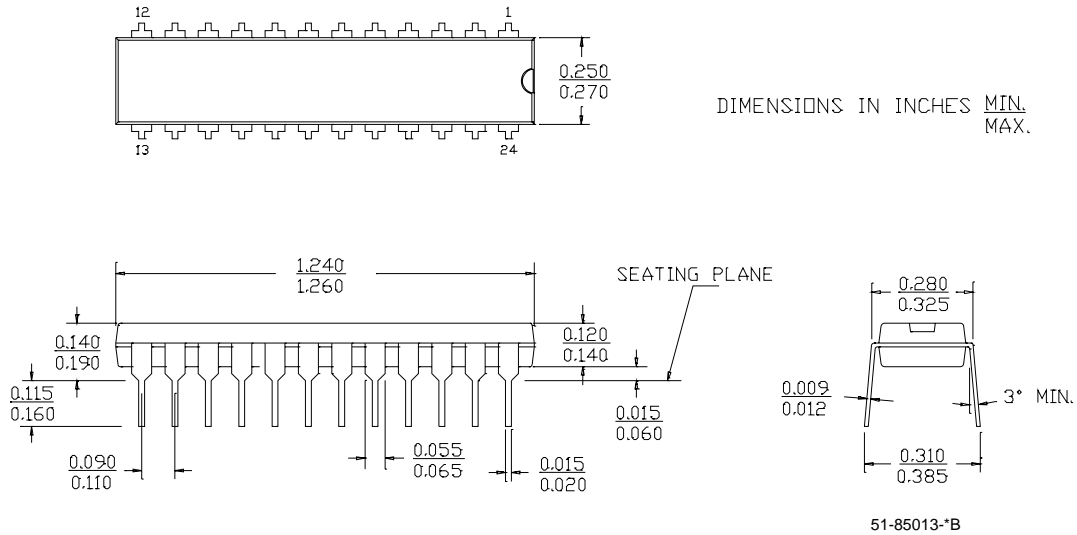
Package Diagrams (Continued)

Figure 3. 28-Square Leadless Chip Carrier L64



Package Diagrams (Continued)

Figure 4. 24-Lead (300-Mil) PDIP P13



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Document History Page

Document Title: CY7C225A 512 x 8 Registered PROM Document Number: 38-04001				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	113858	03/06/02	DSG	Changed from Spec number: 38-00228 to 38-04001
*A	118892	10/09/02	GBI	Updated ordering information
*B	122242	12/27/02	RBI	Added power up requirements to Maximum Ratings Information
*C	499538	See ECN	PCI	Updated ordering information