74ABT16240A

16-bit inverting buffer/line driver; 3-state

Rev. 04 — 25 March 2009 Product data sheet

1. General description

The 74ABT16240A high-performance Bipolar CMOS (BiCMOS) device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16240A is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-state outputs.

2. Features

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA and –32 mA
- Live insertion and extraction permitted
- Latch-up performance: JESD 78 Class II
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - CDM JESD 22-C101-C exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16240ADGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT16240ADL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

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4. Functional diagram

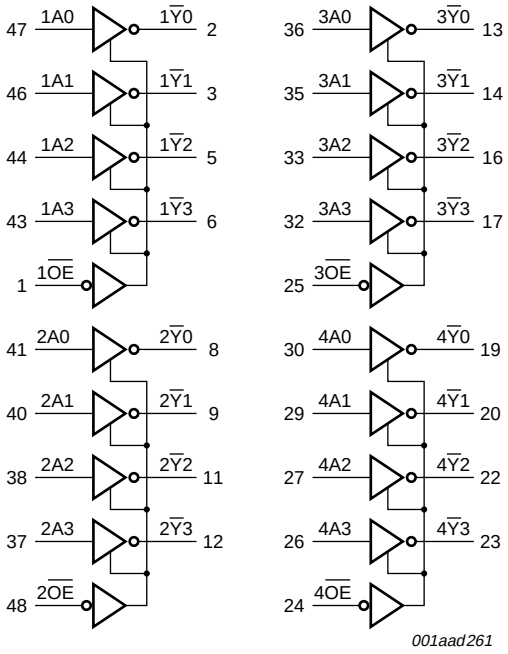


Fig 1. Logic symbol

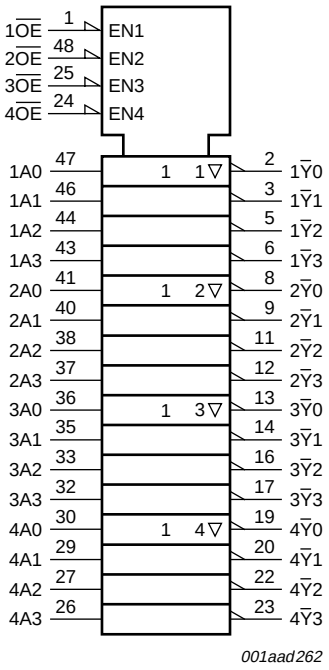


Fig 2. IEC logic symbol

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5. Pinning information

5.1 Pinning

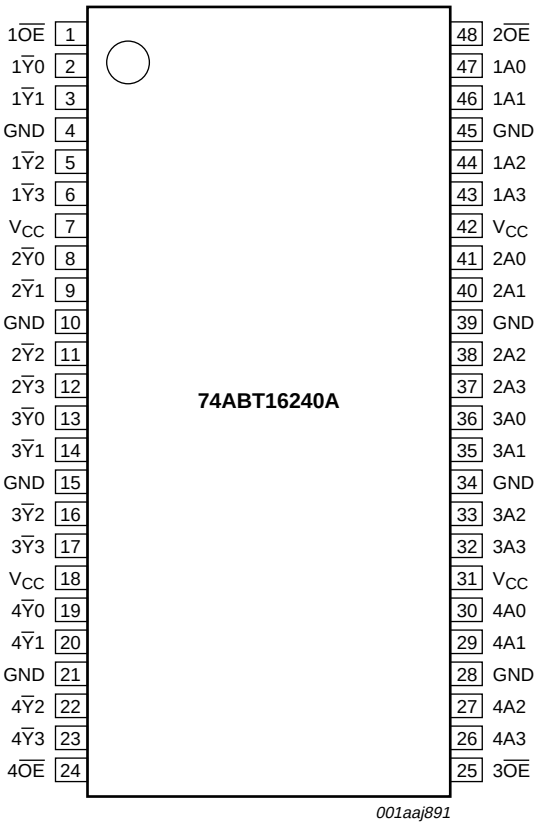


Fig 3. Pin configuration

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5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	1 output enable (LOW active)
$1\overline{Y}[0:3]$	2, 3, 5, 6	1 data output 0 to output 3
GND	4	ground (0 V)
V_{CC}	7	supply voltage
$2\overline{Y}[0:3]$	8, 9, 11, 12	2 data output 0 to output 3
GND	10	ground (0 V)
$3\overline{Y}[0:3]$	13, 14, 16, 17	3 data output 0 to output 3
GND	15	ground (0 V)
V_{CC}	18	supply voltage
$4\overline{Y}[0:3]$	19, 20, 22, 23	4 data output 0 to output 3
GND	21	ground (0 V)
$4\overline{OE}$	24	4 output enable (LOW active)
$3\overline{OE}$	25	3 output enable (LOW active)
GND	28	ground (0 V)
4A[0:3]	30, 29, 27, 26	4 data input 0 to input 3
V_{CC}	31	supply voltage
GND	34	ground (0 V)
3A[0:3]	36, 35, 33, 32	3 data input 0 to input 3
GND	39	ground (0 V)
2A[0:3]	41, 40, 38, 37	2 data input 0 to input 3
V_{CC}	42	supply voltage
GND	45	ground (0 V)
1A[0:3]	47, 46, 44, 43	1 data input 0 to input 3
$2\overline{OE}$	48	2 output enable (LOW active)

6. Functional description

Table 3. Function table[1]

Control	Input	Output
$n\overline{OE}$	**nAx**	**$n\overline{Y}x$**
L	L	H
L	H	L
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA
I_{OL}	LOW-level output current		-	-	32	mA
		duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	-	–1.2	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.42	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $n\overline{OE}$ = V_{CC}	[1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		output HIGH-state at V_O = 5.5 V		-	1.0	10	-	10	µA
		output LOW-state at V_O = 0.5 V		-	–1.0	–10	-	–10	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	1.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	–70	–180	–50	–180	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.5	1.0	-	1.0	mA
		outputs LOW-state		-	8	19	-	19	mA
		outputs 3-state		-	0.5	1.0	-	1.0	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V and other inputs at V_{CC} or GND	[1][3]	-	10	200	-	200	µA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	6	-	-	-	pF

[1] This is the increase in supply current for each input at 3.4 V.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This data sheet limit may vary among suppliers.

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10. Dynamic characteristics

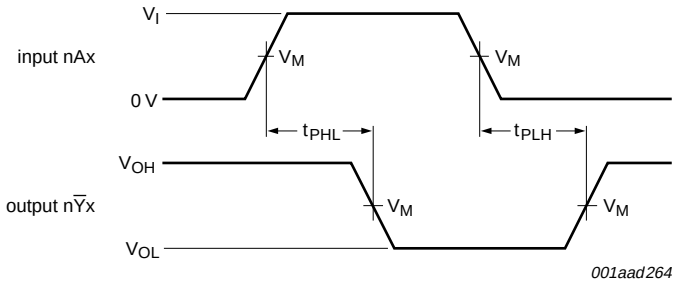
Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Figure 6.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			–40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nAx to n$\overline{Y}$x, see Figure 4	1.0	2.0	3.0	1.0	3.7	ns
t_{PHL}	HIGH to LOW propagation delay	nAx to n$\overline{Y}$x, see Figure 4	1.0	1.5	3.0	1.0	3.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	n$\overline{OE}$ to n$\overline{Y}$x; see Figure 5	1.2	2.4	3.3	1.2	4.2	ns
t_{PZL}	OFF-state to LOW propagation delay	n$\overline{OE}$ to n$\overline{Y}$x; see Figure 5	1.2	2.3	3.2	1.0	4.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	n$\overline{OE}$ to n$\overline{Y}$x; see Figure 5	1.3	2.7	4.1	1.6	4.7	ns
t_{PLZ}	LOW to OFF-state propagation delay	n$\overline{OE}$ to n$\overline{Y}$x; see Figure 5	1.3	2.5	3.6	1.4	4.1	ns

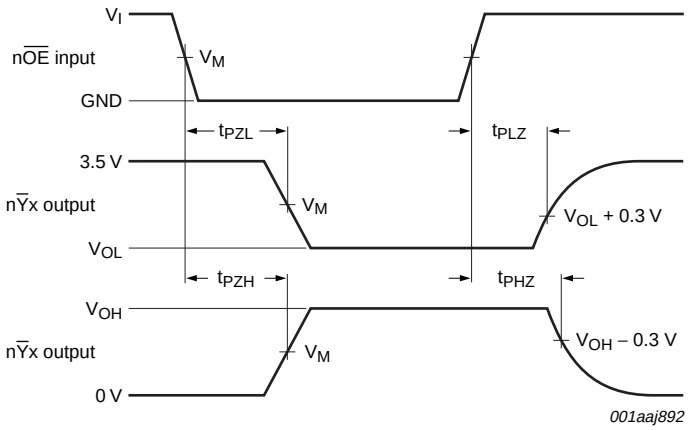
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11. Waveforms



V_M = 1.5 V; V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 4. Input (nAx) to output (nȲx) propagation delay

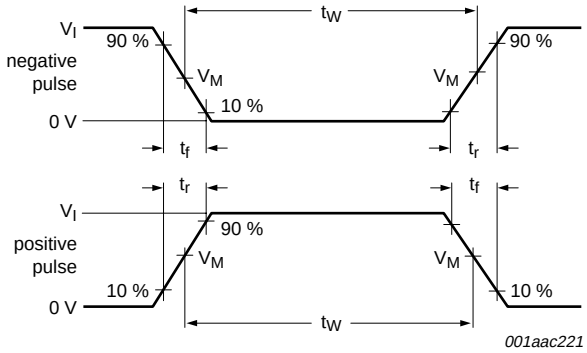


V_M = 1.5 V; V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. 3-state output enable and disable times

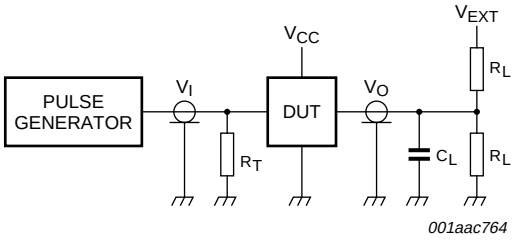
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12. Test information



V_M = 1.5 V.

a. Input pulse definition



Test data is given in Table 8.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

b. Test circuit for 3-state outputs

Fig 6. Load circuitry for switching times

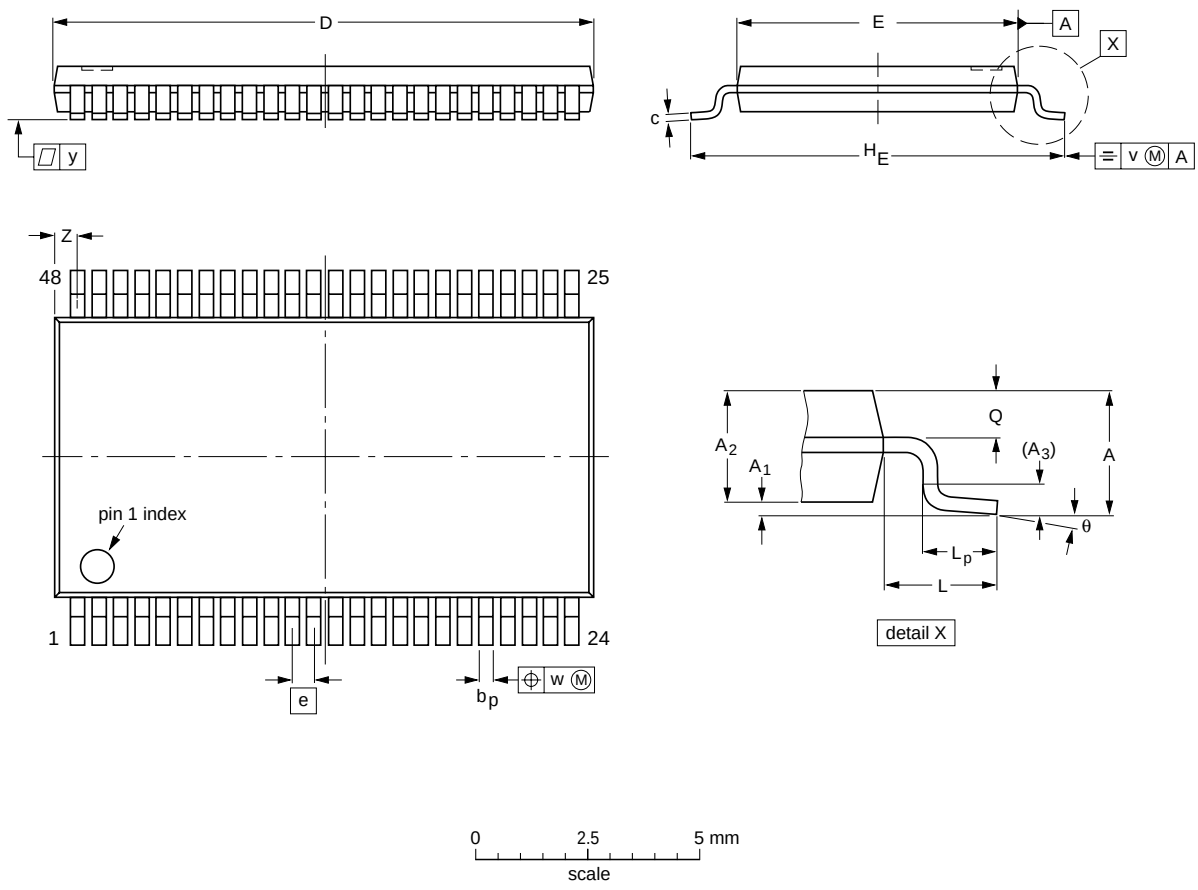
Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

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13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

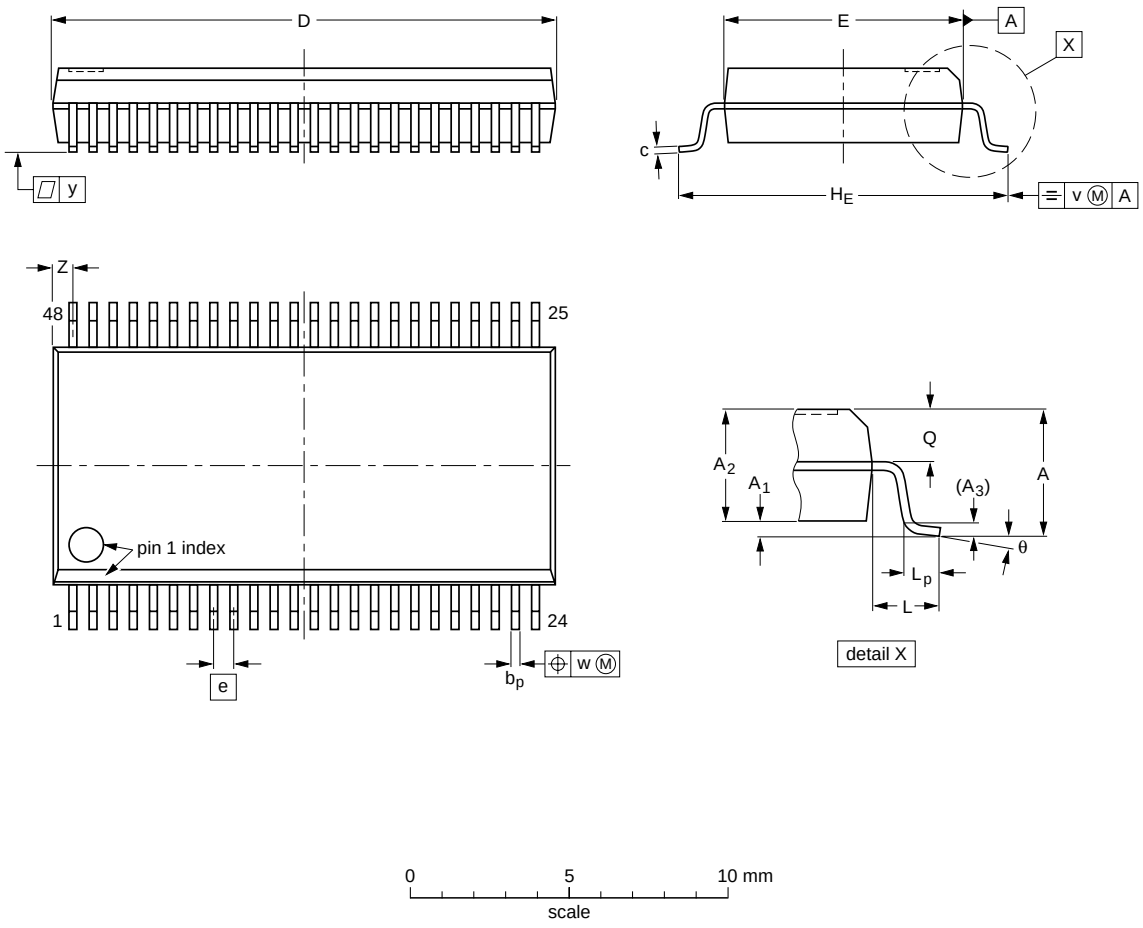
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT362-1 (TSSOP48)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT370-1 (SSOP48)

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14. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16240A_4	20090325	Product data sheet	-	74ABT16240A_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74ABT16240A_3 (9397 750 12893)	20040212	Product specification	01-A15420	74ABT_H16240A_2
74ABT_H16240A_2 (9397 750 03481)	19980225	Product specification	853-1880 19019	74ABT_H16240A
74ABT_H16240A	19961001	Product specification	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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