LPS001WP

MEMS pressure sensor
300-1100 mbar absolute digital output barometer

Preliminary data

Features

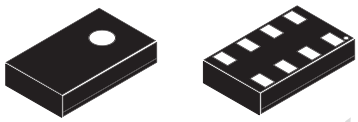
- Piezoresistive pressure sensor
- 300-1100 mbar absolute pressure range
- 0.065 mbar resolution
- Embedded offset and span temperature compensation
- Embedded 16-bit ADC
- SPI and I^2C interfaces
- Supply voltage 2.2 V to 3.6 V
- High shock survivability (10000 g)
- Small and thin package
- ECOPACK® lead-free compliant

Applications

- Altimeter and barometer for portable devices
- Smartphones
- Indoor navigation
- GPS applications
- Weather station equipment
- Sports watches

Description

The LPS001WP is an ultra compact absolute piezoresistive pressure sensor. It includes a monolithic sensing element and an IC interface able to take information from the sensing element and to provide a digital signal to the external world.



HCLGA-8L (3x5x1 mm)

The sensing element consists of a suspended membrane realized inside a single mono-silicon substrate. It is capable of detecting pressure and is manufactured using a dedicated process developed by ST, called *VENSENS*.

The *VENSENS* process allows the building of a mono-silicon membrane above an air cavity with controlled gap and defined pressure.
The membrane is very small compared to the traditionally built silicon micromachined membranes. Membrane breakage is prevented by intrinsic mechanical stoppers.

The IC interface is manufactured using a standard CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LPS001WP is available in a small plastic land grid array (HCLGA) package and is guaranteed to operate over a temperature range extending from -40 °C to +85 °C. The package is holed to allow external pressure to reach the sensing element.

The LPS001WP belongs to a family of products suitable for a variety of applications.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LPS001WP	-40 to +85	HCLGA-8L	Tray
LPS001WPTR			Tape and reel

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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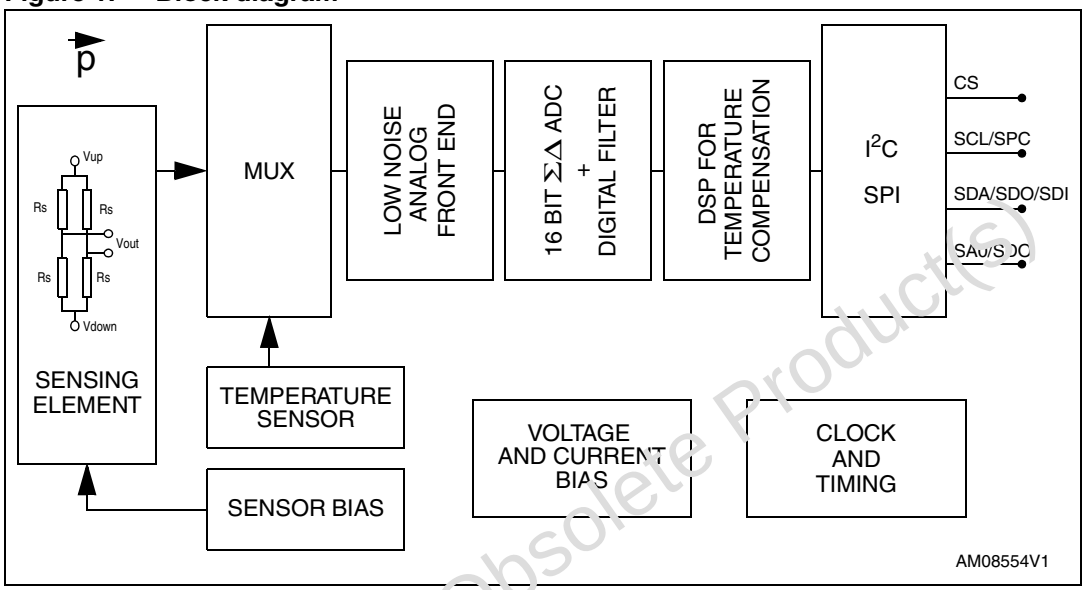
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

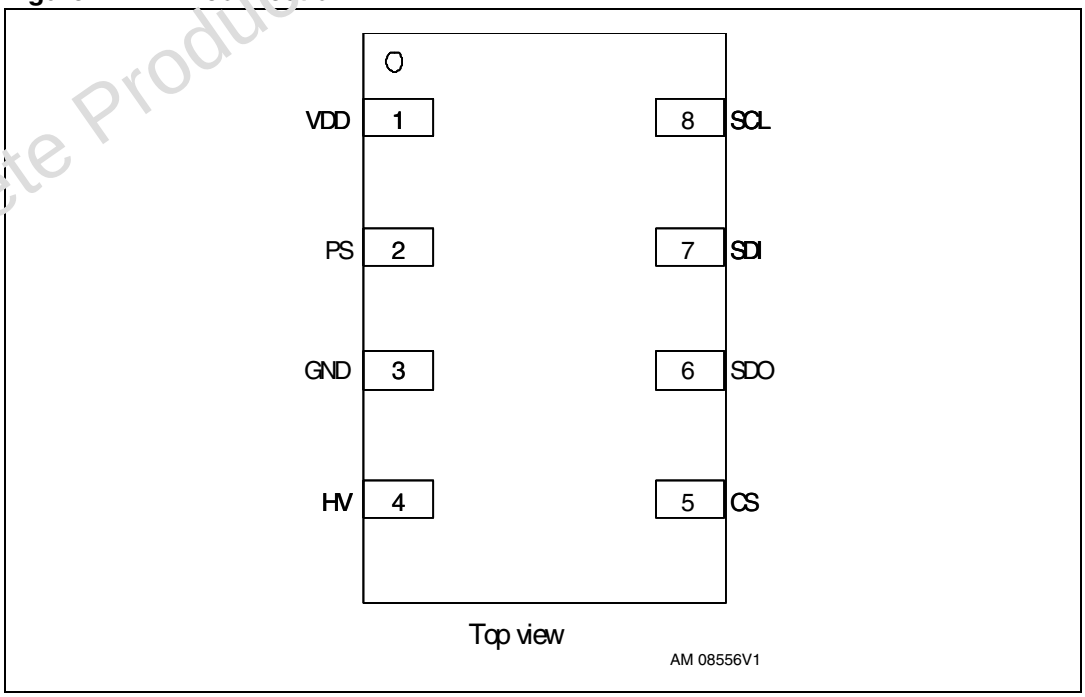


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Table 2. Pin description

Pin n°	Pin name	Function
1	Vdd	Power supply
2	PS	Protocol selection I^2C/SPI mode selection (logic 1: I^2C mode; logic 0: SPI enabled)
3	GND	0 V supply
4	HV	Connect to VDD (logical '1')
5	CS	SPI enable (chip select)
6	SA0/SDO	I^2C less significant bit of device slave address (SA0) SPI serial data output
7	SDA/ SDI/ SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
8	SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)

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2 Mechanical and electrical specifications

Conditions @ Vdd = 2.5 V, T = 25 °C, unless otherwise noted.

2.1 Mechanical characteristics

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Pop	Operating pressure range		300		1100	mbar
Res(2)	Pressure resolution			16		Lsb/mbar
Pn	Pressure noise density			0.028		mbar/sqrt (Hz)
Acc	Accuracy	P = 300 to 1100 mbar T = -10 to 85 °C		+/-2.5		mbar
TSo	Temperature resolution			64		LSb/°C

1. Typical specifications are not guaranteed.
2. Parameter given as standard deviation value.

2.2 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.2		3.6	V
Idd	Supply current	Continous mode ODR_P = 7 Hz ODR_T = 1 Hz		190		µA
		During conversion		400		
IddPdn	Supply current in power-down mode			1		µA
ODR_P	Pressure output data rate(2)			7	12.5	Hz
ODR_T	Temperature output data rate(3)		1	7	12.5	Hz
Top(3)	Extended operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. For pressure and temperature output data rate configurations refer to *Table 18*.
3. Datasheet specification guaranteed only between -10 to 85 °C.

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3 Absolute maximum ratings

Stress above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin	-0.3 to Vdd +0.3	V
P	Overpressure	20	bar
T_{STG}	Storage temperature range	-40 to +125	°C

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

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4 Functionality

The LPS001WP is a high-resolution, digital-output pressure sensor packaged in an LGA holed package. The complete device includes a sensing element based on a piezoresistive Whetstone bridge approach, and an IC interface capable of providing information from the sensing element to external applications as a digital signal.

4.1 Sensing element

An ST proprietary process is used to obtain a mono-silicon µ-sized membrane for MEMS pressure sensors, without requiring substrate-to-substrate bonding.

When pressure is applied, membrane deflection induces an imbalance in the Wheatstone bridge piezoresistors, whose output signal is converted by the IC interface.

Intrinsic mechanical stoppers prevent breakage in case of pressure overstress, ensuring measurement repeatability.

The pressure inside the buried cavity under the membrane is constant and controlled by process parameters.

To be compatible with traditional packaging technologies, a silicon holed cap is placed on top of the sensing element. During the moulding phase, this opening is covered by dedicated protection to avoid membrane blocking.

The package design leaves the holed cap exposed, allowing ambient pressure to reach the sensing element.

4.2 IC interface

The complete measurement chain consists of a low-noise capacitive amplifier, which converts the resistive unbalance of the MEMS sensor into an analog voltage signal, and of an analog-to-digital converter, which translates the produced signal into a digital bitstream.

The converter is coupled with a dedicated reconstruction filter which removes the high frequency components of the quantization noise and provides low rate and high resolution digital words.

The pressure data can be accessed through an I^2C/SPI interface, making the device particularly suitable for direct interfacing with a microcontroller.

4.3 Factory calibration

The IC interface is factory-calibrated at two temperatures and two pressure levels for sensitivity and accuracy.

The trimming values are stored inside the device using a non-volatile structure. Each time the device is turned on, the trimming parameters are downloaded into the registers to be employed during normal operation. This allows the user to employ the device without requiring further calibration.

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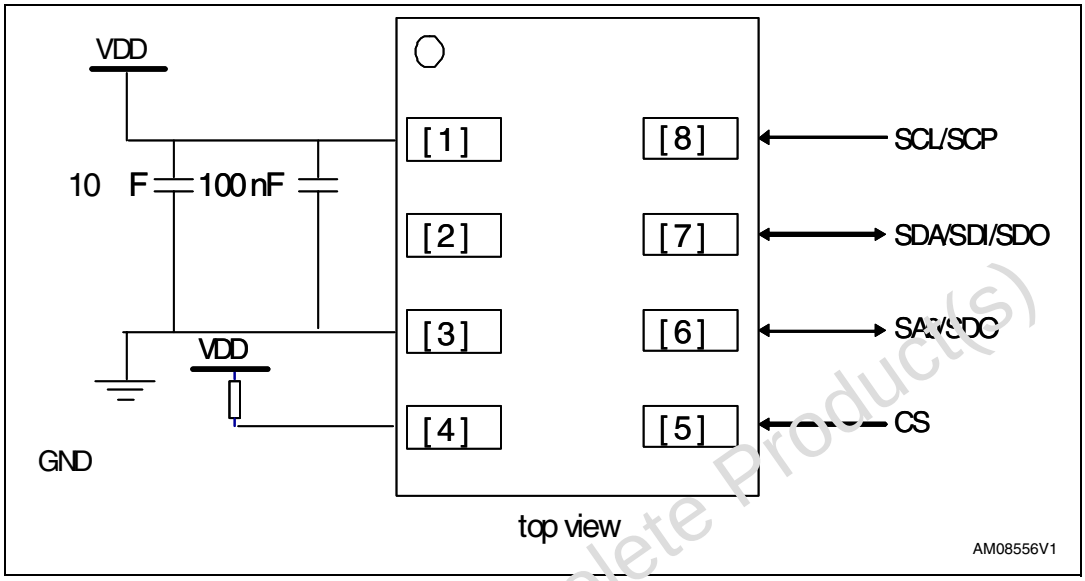
5 Application hints

Figure 3. LPS001WP electrical connection



The device core is supplied through the Vdd line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to the supply pad of the device (common design practice).

The functionality of the device and the measured data outputs are selectable and accessible through the I²C/SPI interface. When using the I²C, CS must be tied high.

It is possible to change, on the fly, the communication interface used to access the device registers. The PS (Protocol Selection) pin performs this change.

5.1 Soldering information

The HCLGA package is compliant with the ECOPACK® standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

5.2 Procedure for single acquisition (low power consumption)

If the LPS001WP output data rate requested is lower than 7 Hz, a dedicated procedure to reduce the power consumption can be implemented.

LPS001WP is in power down, then it is woken up for the acquisition and again put in power down. This procedure reduces the power consumption.

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5.2.1 Reduced power consumption procedure

1. LPS001WP power down and low resolution mode
   a) Write CTRL_REG1 (20h) <= ‘1000xxxx’b

or

   b) Write CTRL_REG1 (20h) <= ‘0000xxxx’b (normal resolution)
2. LPS001WP wake up
   a) Write CTRL_REG1 (20h) <= ‘1100xxxx’b

or

   b) Write CTRL_REG1 (20h) <= ‘0100xxxx’b (normal resolution)
3. Wait 80 ms - settling time
4. Output read
   a) Read PRESS_OUT_H (29h)
   b) Read PRESS_OUT_L (28h)
   c) Read TEMP_OUT_H (2Bh)
   d) Read TEMP_OUT_L (2Ah)
5. LPS001WP power down and low power mode
   a) Write CTRL_REG1 (20h) <= ‘1000xxxx’b

or

   b) Write CTRL_REG1 (20h) <= ‘0000xxxx’b (normal resolution)

Note: *Power down and normal mode configuration:* CTRL_REG1 (20h) <= ‘0000xxxx’b

Table 6. Power consumption @ 1 Hz and @ 4 Hz ODR

Power consumption		Condition	Min.	Typ.(1)	Max.	Unit
Idd	Supply current	Low resolution ODR = 1 Hz		21		µA
		Normal resolution ODR = 4 Hz		75		
		Normal resolution ODR = 1 Hz		40		
		Normal resolution ODR = 4 Hz		150		

1. Typical specifications are not guaranteed.

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6 Digital interfaces

The registers embedded inside the LPS001WP may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, CS line must be tied high.

PS pin select I^2C or SPI interface.

If the I^2C interface is disabled (PS pin connected to GND or logical '0') and CS is kept high (logical '1'), pin SDO and SDI are put in tri-state.

Table 7. Serial interface pin description

PIN Name	PIN Description
PS	Protocol selection I^2C/SPI mode selection (logic 1: I^2C mode; logic 0: I^2C disabled)
CS	SPI enable (chip select)
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0/SDO	I^2C less significant bit of device slave address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LPS001WP I^2C is a bus slave. The I^2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in *Table 8*.

Table 8. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd through a pull-up resistor embedded inside the LPS001WP. When the bus is free, both lines are high.

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The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A start condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LPS001WP is 101110xb. The SDO pad can be used to modify the less significant bit of the device address. If the SDO pad is connected to voltage supply, LSb is '1' (address 1011101b), otherwise, if the SDO pad is connected to ground, the LSb value is '0' (address 1011100b). This solution permits to connect and address two different LPS001WPs to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I²C embedded inside the LPS001WP behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent (SAD + R/W), once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted (SUB): the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow a multiple data read/write.

The slave address is completed with a read/write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write), the master transmits to the slave with an unchanged direction. *Table 9* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

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Table 9. SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	101110	0	1	10111001 (B9h)
Write	101110	0	0	10111000 (B8h)
Read	101110	1	1	10111011 (BBh)
Write	101110	1	0	10111010 (BAh)

Table 10. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 11. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 12. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 13. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW, to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes incrementing the register address, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to read.

In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

6.2 SPI bus interface

The LPS001WP SPI is a bus slave. The SPI allows to write and read the registers of the device.

The serial interface interacts with the outside world with 4 wires: CS, SPC, SDI and SDO.

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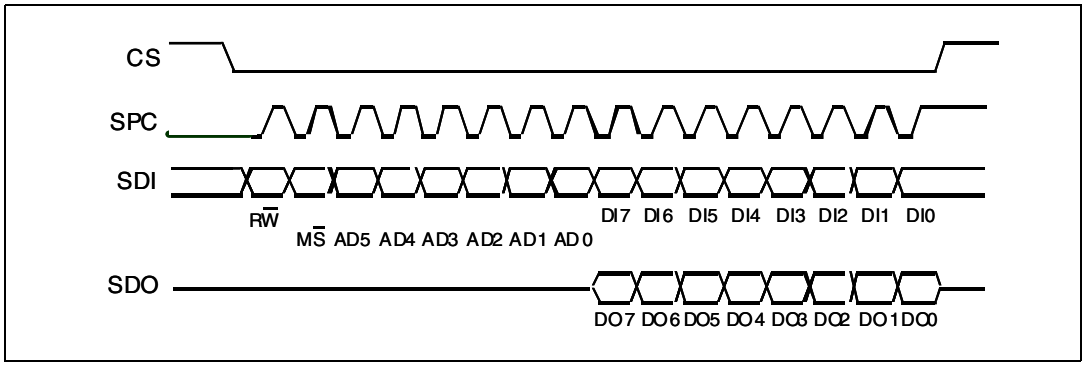
Figure 4. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. SPC is the serial port clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SDI and SDO are respectively the serial port data input and output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple byte read/write. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of CS.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives SDO at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of SDI and SDO remain unchanged.

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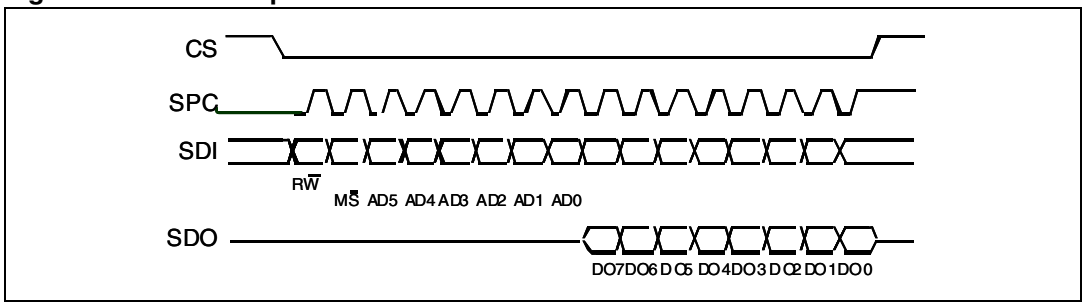
6.2.1 SPI read

Figure 5. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

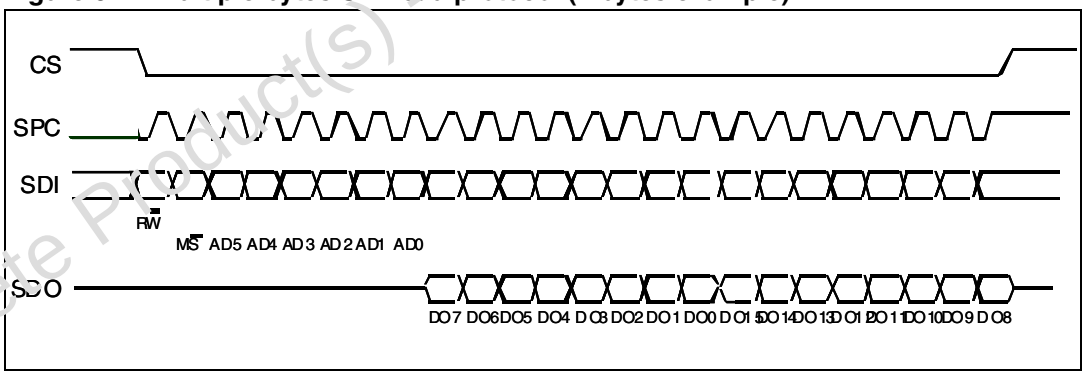
bit 1: MS bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

bit 16-... : data DO(...-8). Further data in multiple byte readings.

Figure 6. Multiple bytes SPI read protocol (2 bytes example)



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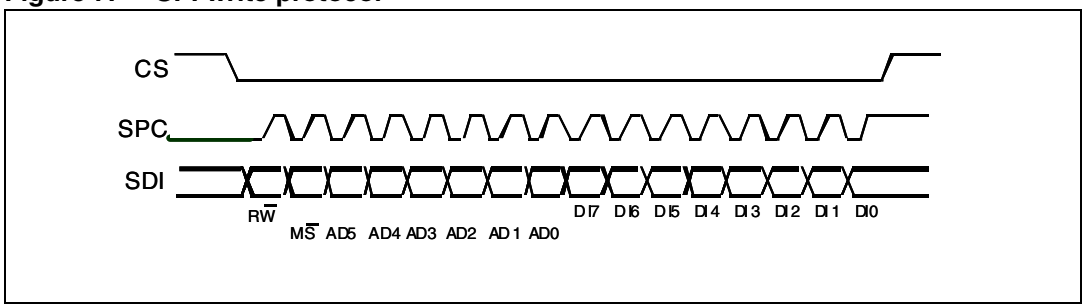
6.2.2 SPI write

Figure 7. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

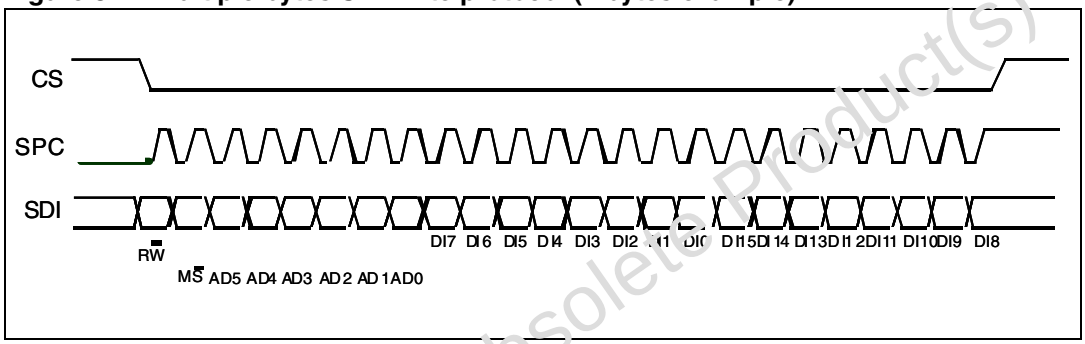
bit 1: MS bit. When 0, do not increment the address, when 1, increment the address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writings.

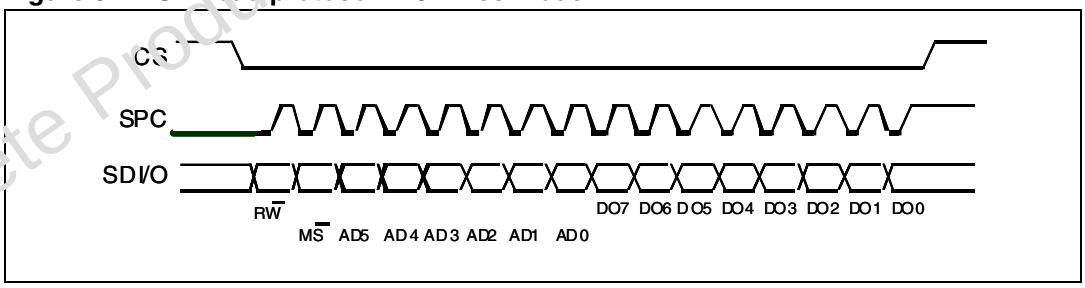
Figure 8. Multiple bytes SPI write protocol (2 bytes example)



6.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI serial interface mode selection) in the internal control register.

Figure 9. SPI read protocol in 3-wires mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: MS bit. When 0, do not increment the address, when 1, increment the address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

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7 Register mapping

Table 14 below provides a listing of the 8-bit registers embedded in the device and the related addresses.

Table 14. Registers address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (Do not modify)		00-0E			Reserved
WHO_AM_I	r	0F	000 1111	10111010	Dummy register
Reserved (Do not modify)		10-1F			Reserved
CTRL_REG1	rw	20	010 0000	00000000	
CTRL_REG2	rw	21	010 0001	00000000	
Reserved (Do not modify)		23-26			Reserved
Status_Reg	r	27	010 0111	00000000	
PRESS_OUT_L	r	28	010 1000	output	
PRESS_OUT_H	r	29	010 1001	output	
TEMP_OUT_L	r	2A	010 1010	output	
TEMP_OUT_H	r	2B	010 1011	output	
DELTA_P_L	r	2C	010 1100	output	
DELTA_P_H	r	2D	010 1101	output	
Reserved (Do not modify)		2E-2F			Reserved
REF_P_L	rw	30	011 0000	00000000	
REF_P_H	rw	31	011 0001	00000000	
THS_P_L	rw	32	011 0010	00000000	
THS_P_H	rw	33	011 0011	00000000	
INTERRUPT_CFG	rw	34	011 0100	00000000	
INT_SOURCE	r	35	011 0101	output	
INT_ACK	r	36	011 0110		Dummy register
Reserved (Do not modify)		37-3F			Reserved

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Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve pressure and temperature data. The registers address, made up of 7 bits, is used to identify them and to read/write the data through the serial interface.

8.1 WHO_AM_I (0Fh)

Table 15. WHO_AM_I (0Fh) register

1	0	1	1	1	0	1	0

Device identification register.

This read only register contains the device identifier which, for LPS001WP, is set to BAh.

8.2 CTRL_REG1 (20h)

Table 16. CTRL_REG1 (20h) register

X	PD	ODR1	ODR0	DIFF_EN	BDU	BLE	SIM

Table 17. CTRL_REG1 (20h) register description

Reserved	Low power functionality. Default value: 0 (0: normal mode; 1: low-power activated)
PD	Power down control. Default value: 0 (0: power-down mode; 1: active mode)
ODR1 ODR0	Output data rate selection. Default value: 00 (see *Table 18*)
DIFF_EN	Interrupt circuit enable. Default value: 0 (0: interrupt generation disabled; 1: interrupt circuit enabled)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian selection. Default value: 0 (0: little endian; 1: big endian)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

PD bit allows to turn on the device. The device is in power-down mode when PD = ‘0’ (default value after boot). The device is active when PD is set to ‘1’.

ODR1 - ODR0 bits allow to change the output data rates of pressure and temperature samples. The default value is “00” which corresponds to a data rate of 7 Hz for pressure

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output and 1Hz for temperature output. ODR1 and ODR2 bits can be configured as described in *Table 18*.

Table 18. Output data rate bit configurations

ODR1(1)	ODR0	Pressure output data rate	Temperature output data rate
0	0	7 Hz	1 Hz
0	1	7 Hz	7 Hz
1	1	12.5 Hz	12.5 Hz

1. “10” bit configuration is not allowed and may cause incorrect device functionality.

DIFF_EN bit is used to enable the circuitry for the computing of delta pressure output, DELTA_P. In default mode (DIFF_EN = ‘0’) this circuitry is turned off.
It is suggested to turn on the circuitry only after the configuration of the REF_P_L, REF_P_H, THS_P_L and THS_P_H registers used by the circuitry.

BDU bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = ‘0’) the lower and upper register parts are updated continuously. If it doesn’t read the output fast enough, the data update is blocked until the two registers have been read. In this way, after the reading of the lower (upper) register part, the content of that output register is not updated until the upper (lower) part is read too. This feature avoids reading LSB and MSB related to different samples.

BLE bit is used to select big endian or little endian representation for output registers. In the big endian one, MSB values are located in PRESS_OUT_L (pressure), TEMP_OUT_L (temperature) and DELTA_P_L (delta pressure), while LSB values are located in PRESS_OUT_H, TEMP_OUT_H and DELTA_P_H. In little endian representation the order is inverted (refer to data registers description for more details).

SIM bit selects the SPI serial interface mode. When SIM is ‘0’ (default value) the 4-wire interface mode is selected and data coming from the device are sent to pin #4 (SDO). In 3-wire interface mode, output data are sent to pin #5 (SDI/SDO).

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8.3 CTRL_REG2 (21h)

Table 19. CTRL_REG2 (21h) register

BOOT	X	X	X	X	X	X	0(1)

1. Bit to be kept to ‘0’ for correct device functionality

Table 20. CTRL_REG2 (21h) register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)

BOOT bit is used to refresh the content of internal registers stored in the flash memory block. At device power-up, the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed, it is sufficient to use this bit

to restore the correct values. When the BOOT bit is set to ‘1’ the content of internal flash is copied inside the corresponding internal registers and is used to calibrate the device. These values are factory trimmed and they are different for every device. They permit a good behavior of the device and normally they do not have to be changed. At the end of the boot process the BOOT bit is set again to ‘0’.
The BOOT bit takes effect after one ODR clock cycle.

8.4 STATUS_REG (27h)

0	0	P_OR	T_OR	0	0	P_DA	T_DA

P_OR	Pressure data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for pressure has overwritten the previous one)
T_OR	Temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for temperature has overwritten the previous one)
P_DA	Pressure data available. Default value: 0 (0: new data for pressure is not yet available; 1: new data for pressure is available)
T_DA	Temperature data available. Default value: 0 (0: new data for temperature is not yet available; 1: new data for temperature is available)

The content of this register is updated every ODR cycle, regardless of the BDU value in CTRL_REG1.

P_DA is set to '1' whenever a new pressure sample is available. P_DA is cleared anytime the PRESS_OUT_H (29h) register is read.

T_DA is set to '1' whenever a new temperature sample is available. T_DA is cleared anytime the TEMP_OUT_H (2Bh) register is read.

P_OR bit is set to '1' whenever new pressure data is available and P_DA was set in the previous ODR cycle and not cleared. P_OR is cleared anytime the PRESS_OUT_H (29h) register is read.

T_OR is set to '1' whenever new temperature data is available and T_DA was set in the previous ODR cycle and not cleared. T_OR is cleared anytime the TEMP_OUT_H (2Bh) register is read.

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8.5 PRESS_OUT_L (28h)

Table 21. PRESS_OUT_L (28h) register

POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0

Table 22. RESS_OUT_L (28h) register description

POUT7 - POUT0	Pressure data LSB (when BLE bit in the CTRL_REG1 is set to ‘0’, little endian)

Pressure data are expressed as absolute values. Values exceeding the operating pressure range (see *Table 3*) are clipped.

In big endian mode (BLE bit in CTRL_REG1 set to ‘1’) the content of this register is the MSB pressure data.

8.6 PRESS_OUT_H (29h)

Table 23. PRESS_OUT_H (29h) register

POUT15	POUT14	POUT13	POUT12	POUT11	POUT10	POUT9	POUT8

Table 24. PRESS_OUT_H (29h) register description

POUT15 - POUT8	Pressure data MSB (when BLE bit in CTRL_REG1 is set to ‘0’)

In big endian mode (BLE bit in CTRL_REG1 set to ‘1’) the content of this register is the LSB pressure data.

8.7 TEMP_OUT_L (2Ah)

Table 25. TEMP_OUT_L (2Ah) register

TOUT7	TOUT6	TOUT5	TOUT4	TOUT3	TOUT2	TOUT1	TOUT0

Table 26. TEMP_OUT_L (2Ah) register description

TOUT7 - TOUT0	Temperature data LSB (when BLE bit in CTRL_REG1 register is set to ‘0’, little endian)

Temperature data are expressed as 2s complement numbers.

In big endian mode (BLE bit in CTRL_REG1 set to ‘1’) the content of this register is the MSB temperature data.

8.8 TEMP_OUT_H (2Bh)

Table 27. TEMP_OUT_H (2Bh) register

TOUT15	TOUT14	TOUT13	TOUT12	TOUT11	TOUT10	TOUT9	TOUT8

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Table 28. TEMP_OUT_H (2Bh) register description

TOUT8 - TOUT15	Temperature data MSB (when BLE bit in CTRL_REG1 register is set to '0')

Temperature data are expressed as 2s complement numbers.

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the LSB temperature data.

8.9 DELTA_P_L (2Ch)

Table 29. DELTA_P_L (2Ch) register

DP7	DP6	DP5	DP4	DP3	DP2	DP1	DP0

Table 30. DELTA_P_L (2Ch) register description

DP7 - DP0	Delta pressure data LSB (when BLE bit in CTRL_REG1 register is set to '0')

DELTA_P registers store a delta pressure representing the difference between a constant reference value, REF_P registers, and the actual pressure measured, PRESS_OUT registers.

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the MSB delta pressure data.

8.10 DELTA_P_H (2Dh)

Table 31. DELTA_P_H (2Dh) register

DP15	DP14	DP13	DP12	DP11	DP10	DP9	DP8

Table 32. DELTA_P_H (2Dh) register description

DP15 - DP8	Delta pressure data MSB (when BLE bit in CTRL_REG1 register is set to '0').

In big endian mode (BLE bit in CTRL_REG1 set to '1') the content of this register is the LSB delta pressure data.

8.11 REF_P_L (30h)

Table 33. REF_P_L (30h) register

REFL7	REFL6	REFL5	REFL4	REFL3	REFL2	REFL1	REFL0

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Table 34. REF_P_L (30h) register description

REFL7 - REFL0	Reference pressure LSB data. Default value: 00h.

This register contains the lower part of the reference pressure for computing of delta pressure.
Full value is REF_P_H & REF_P_L and it is represented as an unsigned number.

8.12 REF_P_H (31h)

Table 35. REF_P_H (31h) register

REFL15	REFL14	REFL13	REFL12	REFL11	REFL10	REFL9	REFL8

Table 36. REF_P_H (31h) register description

REFL15 - REFL8	Reference pressure MSB data. Default value: 00h.

This register contains the higher part of the reference pressure for computing of delta pressure.
Full value is REF_P_H & REF_P_L and it is represented as an unsigned number.

8.13 THS_P_L (32h)

Table 37. THS_P_L (32h) register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 38. THS_P_L (32h) register description

THS7 - THS0	Threshold pressure LSB. Default value: 00h.

This register contains the low part of threshold value for pressure interrupt generation.
The complete threshold value is given by THS_P_H & THS_P_L and is expressed as an unsigned number.

8.14 THS_P_H (33h)

Table 39. THS_P_H (33h) register

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

Table 40. THS_P_H (33h) register description

THS15 - THS8	Threshold pressure MSB. Default value: 00h.

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This register contains the high part of threshold value for pressure interrupt generation. The complete threshold value is given by THS_P_H & THS_P_L and is expressed as an unsigned number.

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9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 41. HCLGA-8L mechanical data

Dimensions			
Ref.	mm		
	Min.	Typ.	Max.
E1	2.850	3.0	3.150
E3		0	
D1	4.850	5.0	5.150
D3		1.200	
R1		1.0	
A1		1.0	
N1		1.0	
N2		0.625	
L1		2.0	
L2		3.750	
P1		1.300	
P2		2.300	
T1		0.800	
d		0.200	
T2		0.500	
K		0.050	
M1		0.100	

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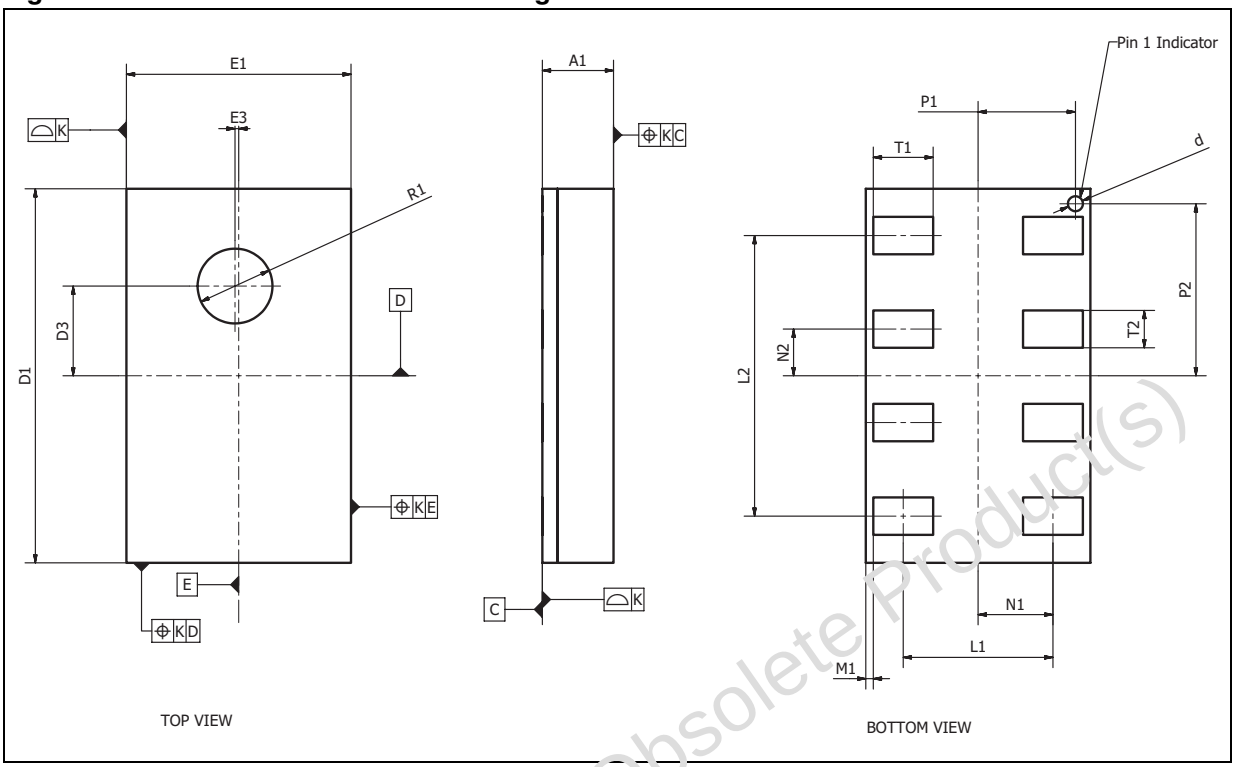
Figure 10. HCLGA-8L mechanical drawing



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10 Revision history

Table 42. Document revision history

Date	Revision	Changes
05-Nov-2010	1	Initial release.

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