

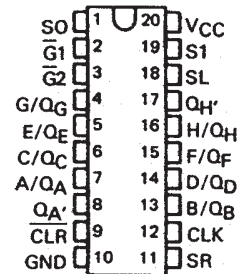
SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:
Hold (Store) Shift Left
Shift Right Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

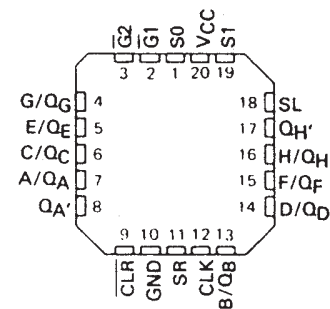
SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS299, SN54S299 . . . FK PACKAGE

(TOP VIEW)



- Applications:
Stacked or Push-Down Registers
Buffer Storage, and Accumulator Registers

TYPE	GUARANTEED SHIFT (CLOCK) FREQUENCY	TYPICAL POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS										OUTPUTS	
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	†	X	H	H	QAn	QBn	QCn	QDn	QEn	QFn	QGn	H	QGn
	H	L	H	L	L	†	X	L	L	QAn	QBn	QCn	QDn	QEn	QFn	QGn	L	QGn
Shift Left	H	H	L	L	L	†	H	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	H	QBn	H
	H	H	L	L	L	†	L	X	QBn	QCn	QDn	QEn	QFn	QGn	QHn	L	QBn	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

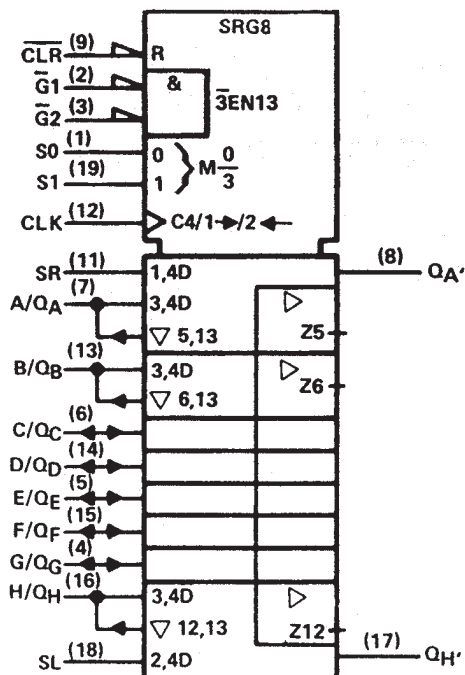
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

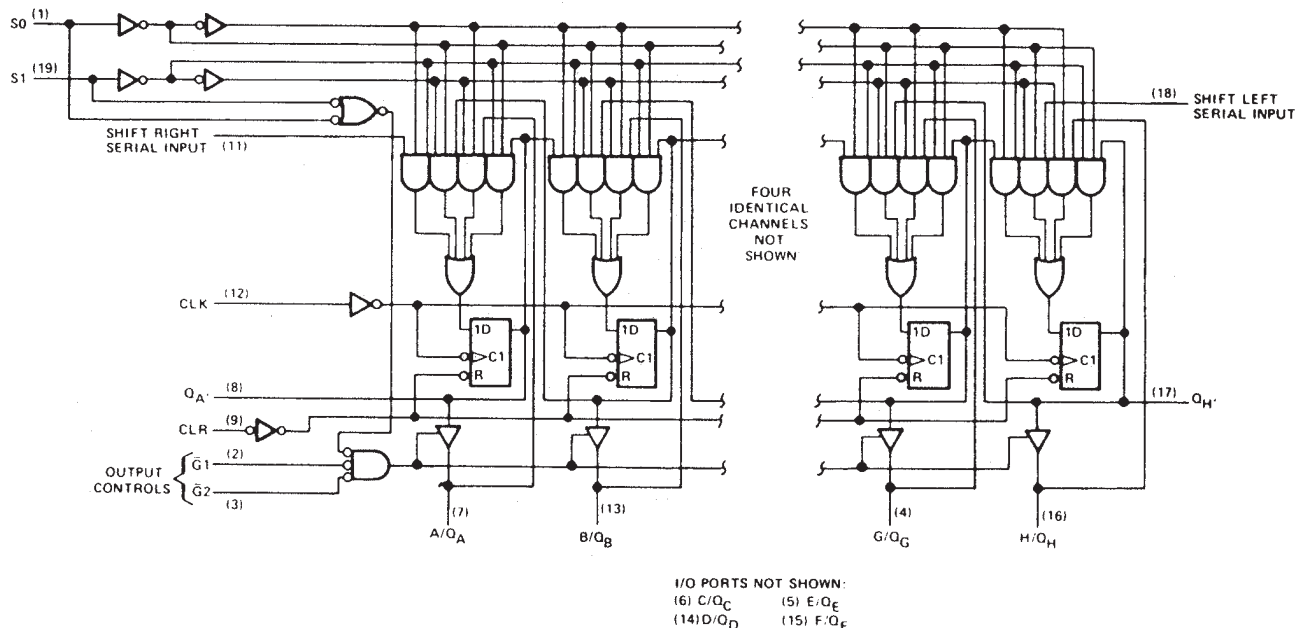
SDLS156 – MARCH 1974 – REVISED MARCH 1988

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

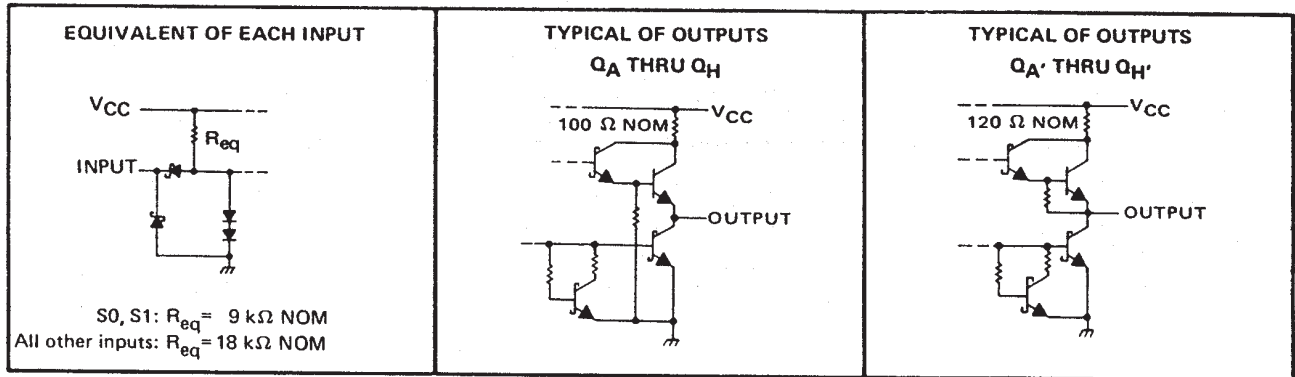


Pin numbers shown are for DW, J, N, and W packages.

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	-55°C to 125°C
SN74LS299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V	
High-level output current, I _{OH}	Q _A thru Q _H	-1			-2.6			mA	
	Q _A ' or Q _H '	-0.4			-0.4				
Low-level output current, I _{OL}	Q _A thru Q _H	12			24			mA	
	Q _A ' or Q _H '	4			8				
Clock frequency, f _{clock}		0			0			20	MHz
Width of clock pulse, t _w (clock)	Clock high	30			30			ns	
	Clock low	18			10				
Width of clear pulse, t _w (clear)		Clear low			20			ns	
Setup time, t _{su}	Select	35†			35†			ns	
	High-level data†	20†			20†				
	Low-level data†	20†			20†				
	Clear inactive-state	24†			20†				
Hold time, t _h	Select	10†			10†			ns	
	Data†	3†			0†				
Operating free-air temperature, T _A		-55			0			70	°C

† Data includes the two serial inputs and the eight input/output data lines.

SN54LS299, SN54S299, SN74LS299, SN74S299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS299			SN74LS299			UNIT	
			MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IH}	High-level input voltage		2			2			V	
V _{IL}	Low-level input voltage		0.7			0.8			V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA	-1.5			-1.5			V	
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	2.4	3.1	V		
		Q _A ' or Q _H '	V _{IL} = V _{ILmax} , I _{OH} = MAX	2.5	3.4	2.7	3.4			
V _{OL}	Low-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax}	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
				I _{OL} = 24 mA			0.35	0.5		
		Q _A ' or Q _H '		I _{OL} = 4 mA	0.25	0.4	0.25	0.4		
				I _{OL} = 8 mA			0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.7 V	40			40		μA	
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.4 V	-400			-400		μA	
I _I	Input current at maximum input voltage	S0, S1	V _{CC} = MAX	V _I = 7 V	200			200		μA
		A thru H		V _I = 5.5 V	100			100		
		Any other		V _I = 7 V	100			100		
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V	40			40		μA	
		Any other		20			20			
I _{IL}	Low-level input current	S0, S1	V _{CC} = MAX, V _I = 0.4 V	-0.8			-0.8		mA	
		Any other		-0.4			-0.4			
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX	-30	-130	-30	-130	mA		
		Q _A ' or Q _H '		-20	-100	-20	-100			
I _{CC}	Supply current	V _{CC} = MAX	33 53			33 53			mA	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			See Note 2	20	35		MHz
t_{PLH}	CLK	Q_A' or Q_H'	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		22	33	ns
t_{PHL}		Q_A' or Q_H'			26	39	
t_{PHL}		Q_A' or Q_H'			27	40	ns
t_{PLH}	CLK	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 45 \text{ pF}$		17	25	ns
t_{PHL}		Q_A thru Q_H			26	39	
t_{PHL}		Q_A thru Q_H			26	40	ns
t_{PZH}	$\overline{G1}, \overline{G2}$	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 5 \text{ pF}$		13	21	ns
t_{PZL}		Q_A thru Q_H			19	30	
t_{PHZ}	$\overline{G1}, \overline{G2}$	Q_A thru Q_H	$R_L = 665 \Omega, C_L = 5 \text{ pF}$		10	20	ns
t_{PLZ}		Q_A thru Q_H			10	15	

¶ f_{max} = maximum clock frequency

t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max} , all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

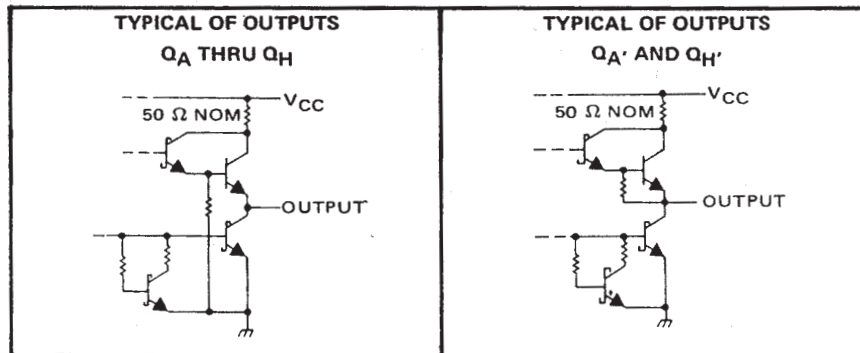
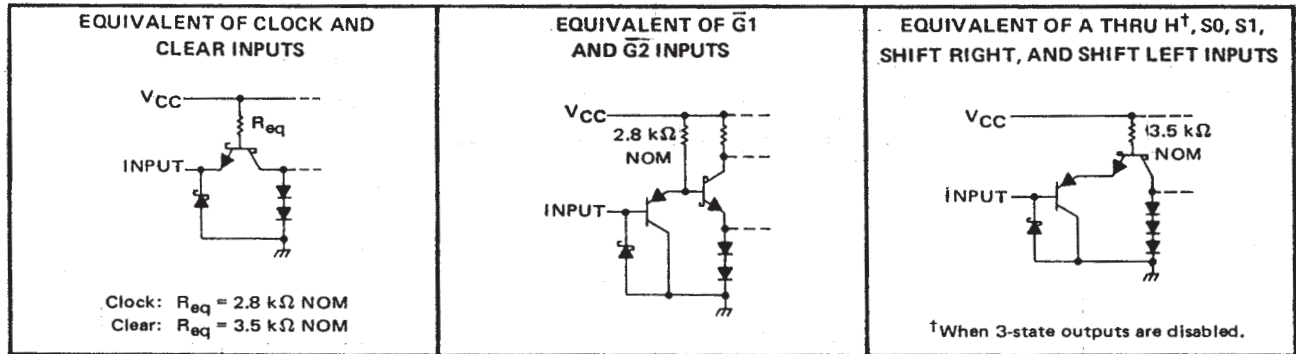


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S299 (See Note 1)	–55 °C to 125 °C
SN74S299	0 °C to 70 °C
Storage temperature range	–65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			–2			–6.5	mA
	Q_A' or Q_H'			–0.5			–0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	Q_A' or Q_H'			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$		10			10			ns
Setup time, t_{su}	Select	15 [†]			15 [†]			ns
	High-level data [†]	7 [†]			7 [†]			
	Low-level data [†]	5 [†]			5 [†]			
	Clear inactive-state	10 [†]			10 [†]			
Hold time, t_h	Select	5 [†]			5 [†]			ns
	Data [†]	5 [†]			5 [†]			
Operating free-air temperature, T_A		–55		125	0		70	°C

[†] Data includes the two serial inputs and the eight input/output data lines.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN54LS299, SN54S299, SN74LS299, SN74S299

8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = –18 mA			–1.2	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	V
		Q _A ' or Q _H '	V _{IL} = 0.8 V, I _{OH} = MAX	2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		100	μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		–250	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V		1		mA
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V		100	μA
		Any other			50	
I _{IL}	Low-level input current	CLK or CLR	V _{CC} = MAX, V _I = 0.5 V		–2	mA
		S0, S1			–500	μA
		Any other			–250	μA
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX	–40	–100	mA
		Q _A ' or Q _H '		–20	–100	
I _{CC}	Supply current	V _{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 1 kΩ, C _L = 15 pF		12	20	ns
t _{PHL}					13	20	
t _{PHL}	CLR	Q _A ' or Q _H '			14	21	ns
t _{PLH}	CLK	Q _A thru Q _H	R _L = 280 Ω, C _L = 45 pF		15	21	ns
t _{PHL}					15	21	
t _{PHL}	CLR	Q _A thru Q _H			16	24	ns
t _{PZH}	G1, G2	Q _A thru Q _H			10	18	ns
t _{PZL}					12	18	
t _{PHZ}	G1, G2	Q _A thru Q _H	R _L = 280 Ω, C _L = 5 pF		7	12	ns
t _{PLZ}							

¶ f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.