AN3090
Application note

Power saving and LED status detection using the STP16DPPS05 device

Introduction

Today, the use of LEDs is growing in many market segments, including portable applications, due to their improving performance and lower cost.

This new scenario requires that LED drivers be capable of providing good performance at low current, and include power saving capabilities.To address these requirements, STMicroelectronics has introduced the STP16xPPx05 family of LED drivers.

This application note describes the STP16DPPS05 low voltage 16-bit constant current LED sink driver, with particular focus on two important features: output error detection and auto power-saving.

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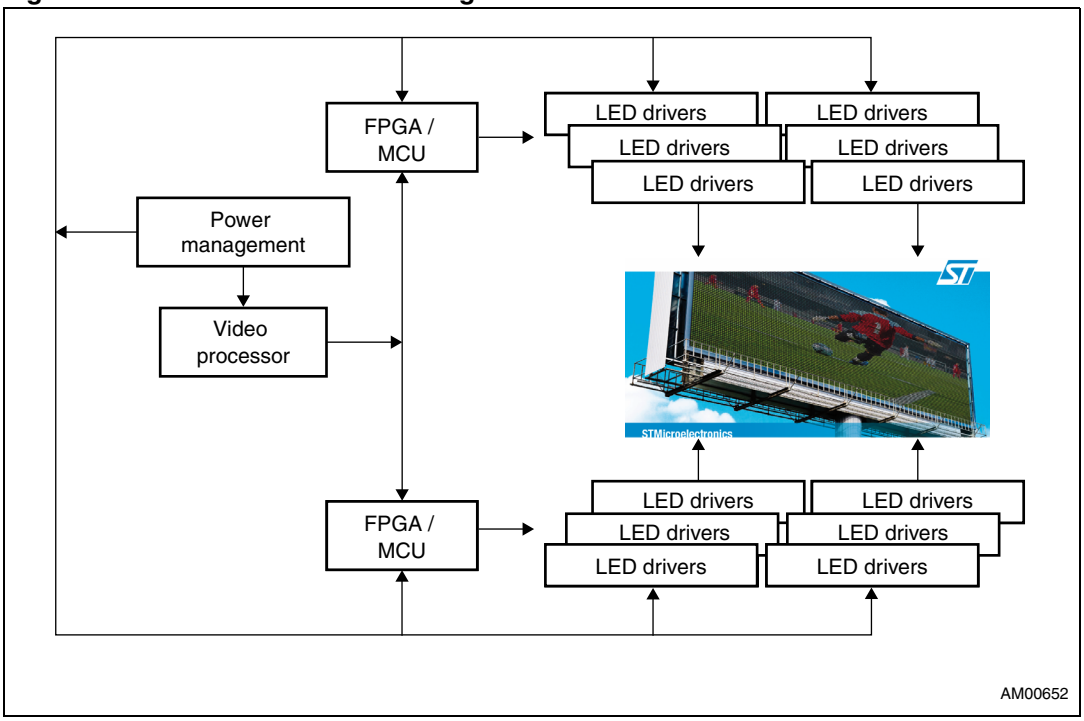
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1 Device description

The STP16DPPS05 device is a monolithic, low voltage, low current power shift register. It contains a 16-bit serial IN, parallel OUT shift register that feeds a 16-bit D-type storage register. Sixteen regulated currents are present in the output stage, which is capable of providing 3-40 mA of constant current to drive the LEDs. *Figure 1* shows the application block diagram of the STP16DPPS05 device.

Figure 1. STP16DPPS05 block diagram



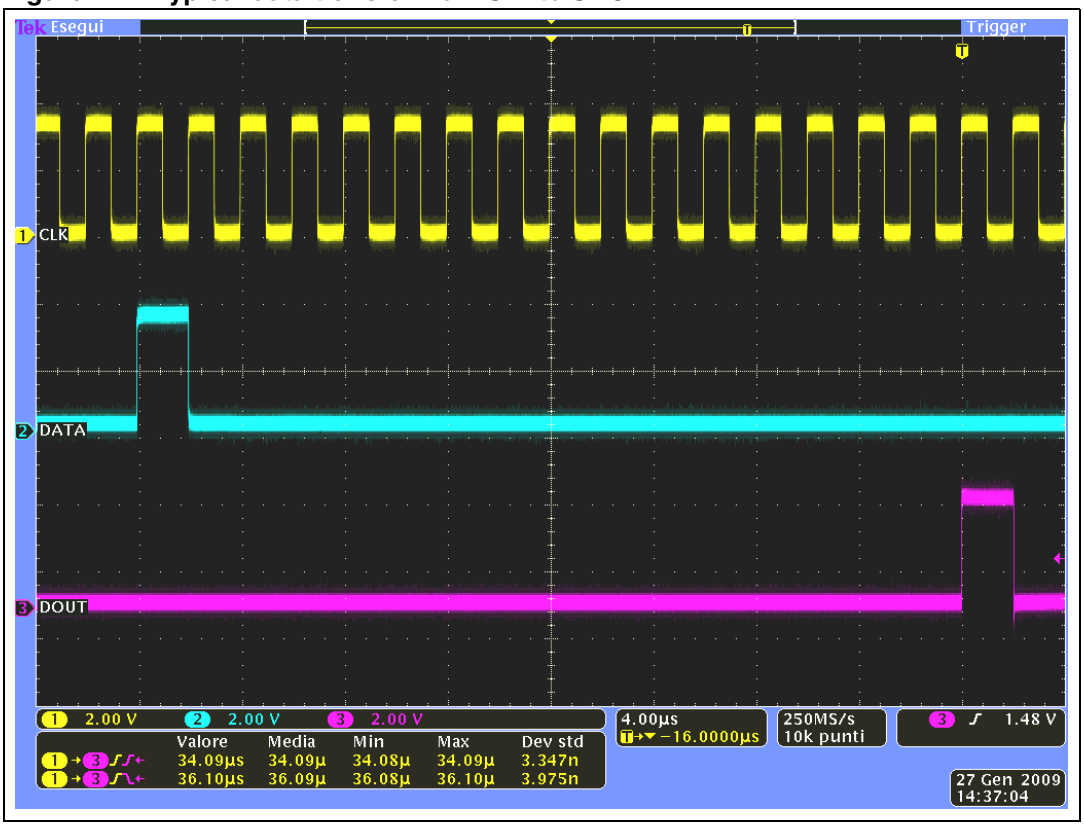
Two important features of STP16DPPS05 are output status checking to detect LED errors during driving (error detection), and power saving when the device is not managing data (auto power safe).

2 Normal mode functionality

During normal operation, the serial data present on the SDI pin is transferred to the shift register in synchronization with the CLK rising edge. After 16 CLK pulses, the data loaded on the SDI pin is shifted to the SDO pin with a typical delay of 22 ns, as shown on the plot in *Figure 2*.

This delay guarantees the correct synchronization of the CLK and SDI signals if two or more STP16DPPS05 devices are cascaded.

Figure 2. Typical data transfer from SDI to SDO



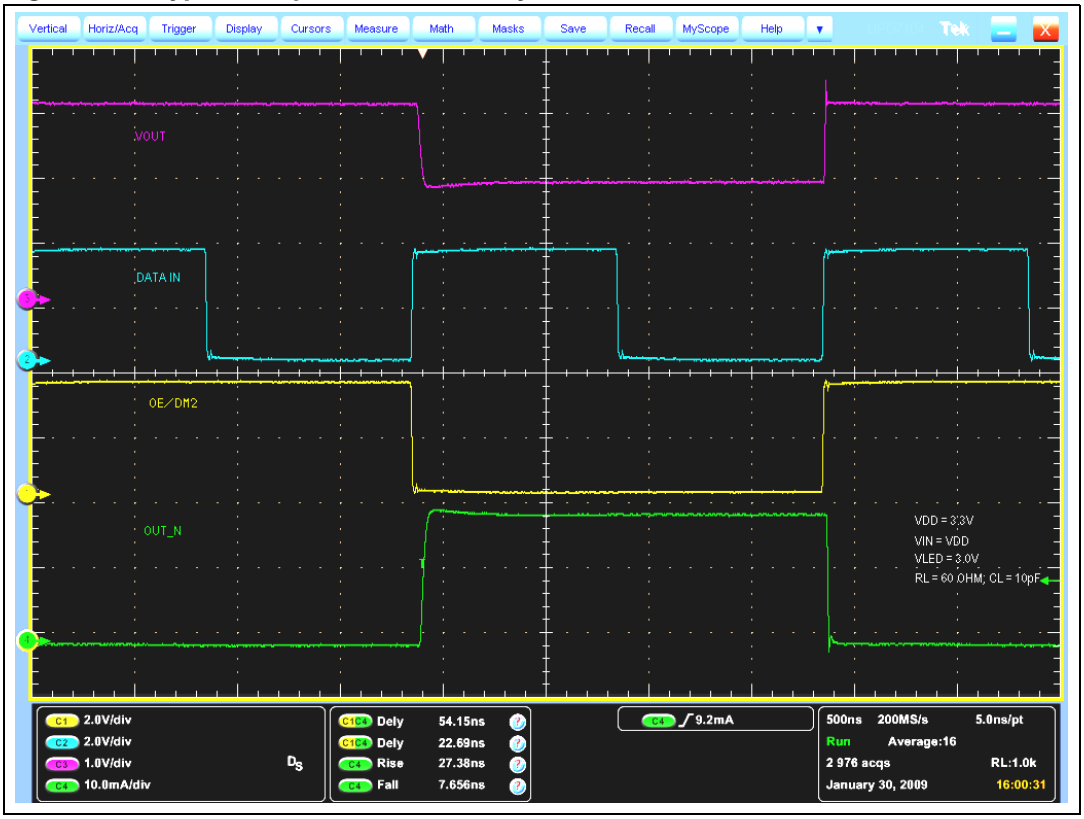
The data present in any register is transferred to the respective latch when the latch-enable (LE/DM1) signal is high (serial-to-parallel conversion).

After this step, the data is transferred to the outputs via the output-enable pin ($\overline{\text{OE/DM2}}$), which turns on the LEDs at the current set by the external resistor.

By changing the $\overline{\text{OE/DM2}}$ duty cycle, it is possible to set the output dimming if the application requires slow or fast frame visualization.

The plot in *Figure 3* shows typical output switching in normal mode at V_{DD} = 3.3 V.

Figure 3. Typical output_n functionality in normal mode



The following signals are shown on the plot above:

- Ch1 (yellow) = $\overline{OE/DM2}$ signal
- Ch2 (blue) = SDI signal
- Ch3 (purple) = V_{OUT}
- Ch4 (green) = OUPUT signal

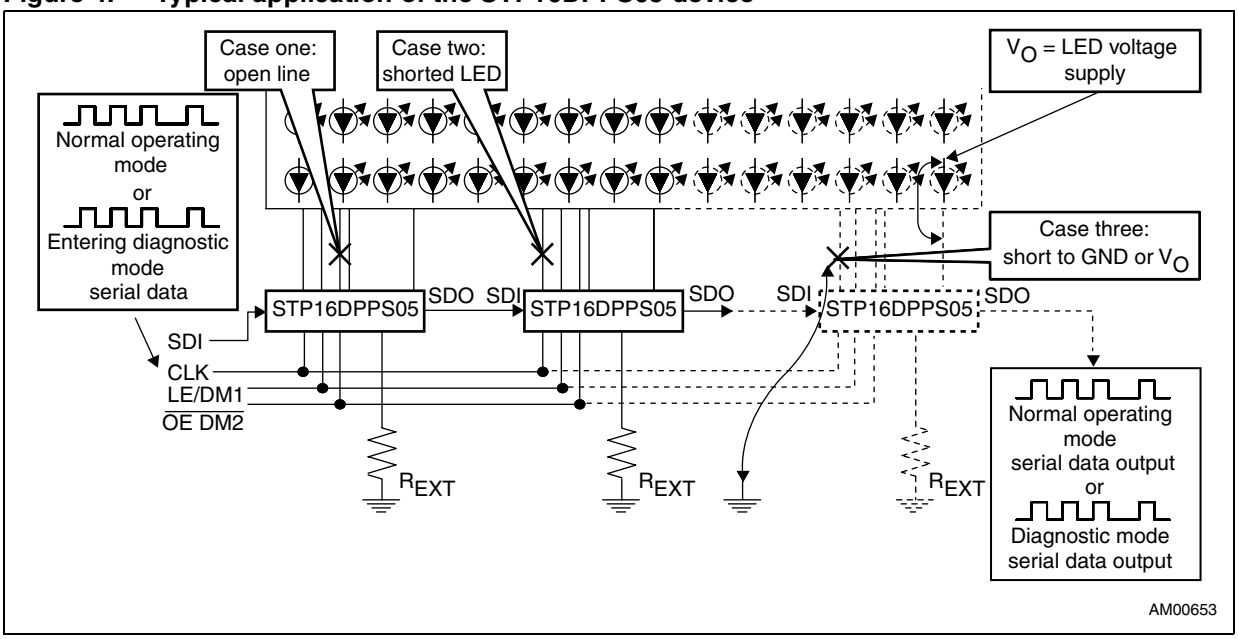
It should be highlighted that the LE/DM1 and $\overline{OE/DM2}$ signals are NOT synchronized with the rising or falling edges of the CLK signal. This mechanism is useful in all applications, especially where it is necessary to stop the CLK switching. For example, after the frame loading, it is necessary to stop the CLK switching to reduce noise between the lines.

3 Error detection feature

The output error detection feature allows LED functionality checks by means of output status detection. This feature covers two types of detection: open-circuit and short-circuit detection.

The schematic in *Figure 4* shows a typical application where multiple STP16DPPS05 devices are cascaded.

Figure 4. Typical application of the STP16DPPS05 device



From “normal mode”, the device is switched to “error detection mode” (EDM) by a logic sequence on the LE/DM1 and $\overline{OE}$/DM2 pins. In order to switch on all the outputs during the detection time, the sixteen data bits must be set to “1”.

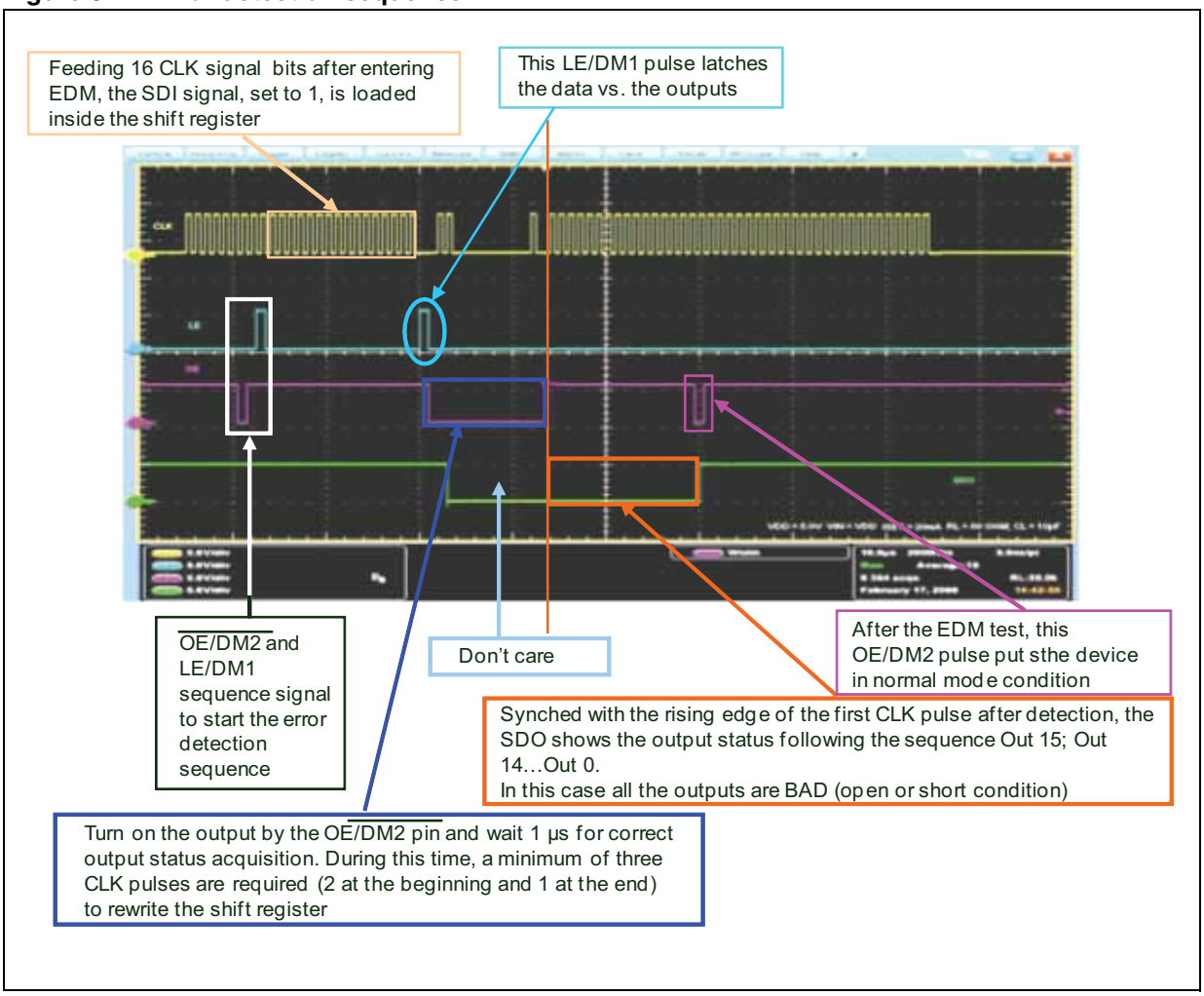
The data are latched by the LE/DM1, after which the outputs are ready for the detection process.

When the microcontroller switches the $\overline{OE}$/DM2 to low, the device drives the LEDs to check if an open or short condition has occurred. The acquisition time ($\overline{OE}$/DM2 to low) necessary to allow for correct LED feedback is typically 1 µs. Two CLK pulses must be sent after the minimum detection time (typical: 500-600 ns), in order to set the SDO pin to the correct output error detection value. In this way, the data loaded in the shift register is updated (rewritten) with the error detection data when the $\overline{OE}$/DM2 signal goes high.

In synchronization with the rising edge of the CLK signal, the LED status is provided by the SDO pin: a “1” logic level signals a good output, while a “0” logic level signals an output fault condition (short or open condition).

The plot in *Figure 5* shows all the steps required to perform the EDM test.

Figure 5. Error detection sequence



As described above, the output status detection sequence is synchronized with the rising edge of the CLK signal after $\overline{\text{OE/DM2}}$ changes to high. An overview of the output results is shown in *Table 1*.

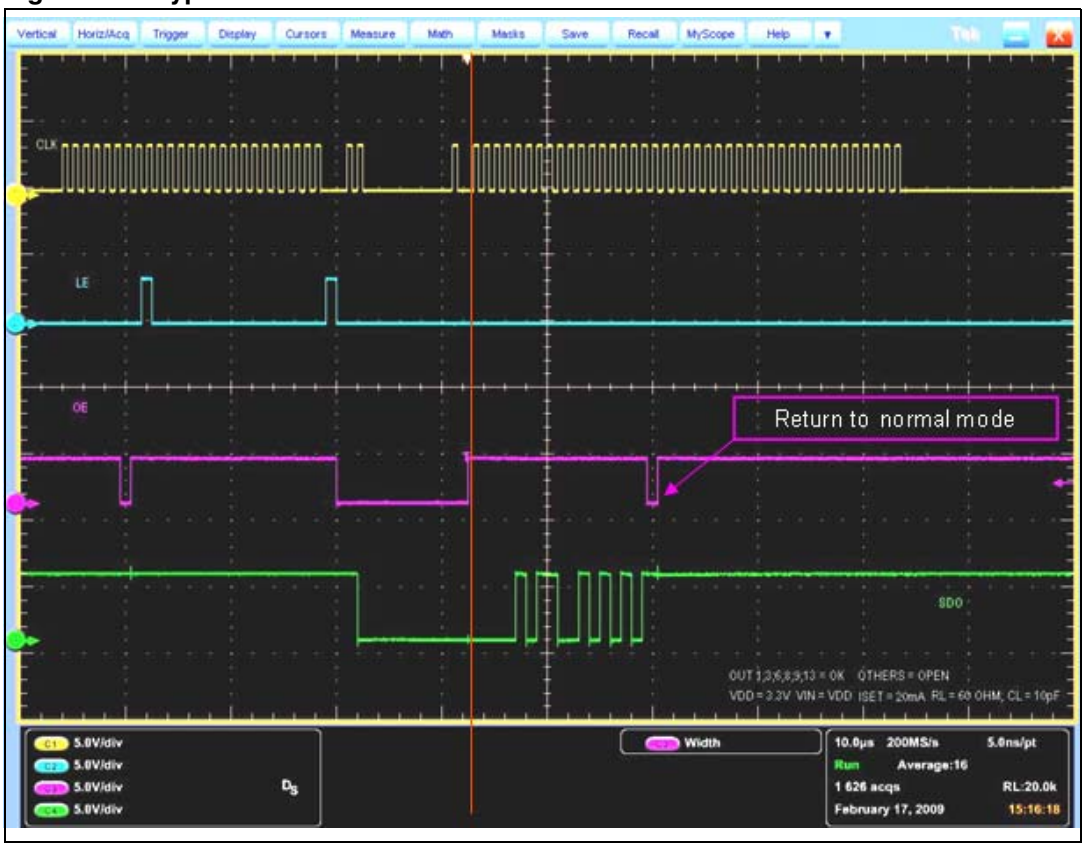
Table 1. Output error detection sequence after $\overline{OE/DM2}$ acquisition

CLK pulse after OE turns to high level	Output results
1st CLK rising edge	Output 16
2nd CLK rising edge	Output 15
3rd CLK rising edge	Output 14
4th CLK rising edge	Output 13
5th CLK rising edge	Output 12
6th CLK rising edge	Output 11
7th CLK rising edge	Output 10
8th CLK rising edge	Output 9
9th CLK rising edge	Output 8
10th CLK rising edge	Output 7
11th CLK rising edge	Output 6
12th CLK rising edge	Output 5
13th CLK rising edge	Output 4
14th CLK rising edge	Output 3
15th CLK rising edge	Output 2
16th CLK rising edge	Output 1

To resume normal mode functionality, it is mandatory to apply another $\overline{OE/DM2}$ pulse after 16 CLK pulses.

The plot in *Figure 6* shows a typical example of error detection feedback. Observing the SDO (green signal) and $\overline{OE/DM2}$ (purple signal) it is possible to verify, respectively, the output status and how the device returns to normal mode.

Figure 6. Typical error detection results



The following signals are shown on the plot above:

- Ch1 (yellow) = CLK signal
- Ch2 (blue) = LE/DM1 signal
- Ch3 (purple) = $\overline{OE}$/DM2 signal
- Ch4 (green) = SDO signal

Figure 7 shows the $\overline{\text{OE/DM2}}$ and LE/DM1 digital key combination necessary to start the EDM test. If this sequence is incorrect, the EDM test does not start.

Figure 7. Entering output error detection timing

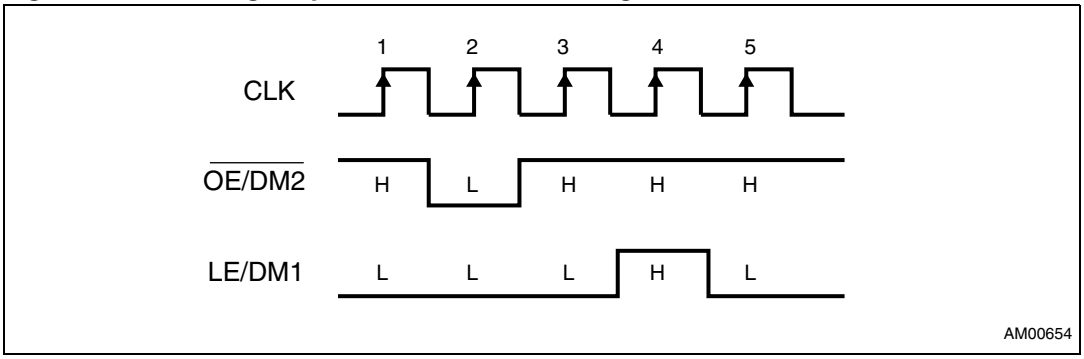
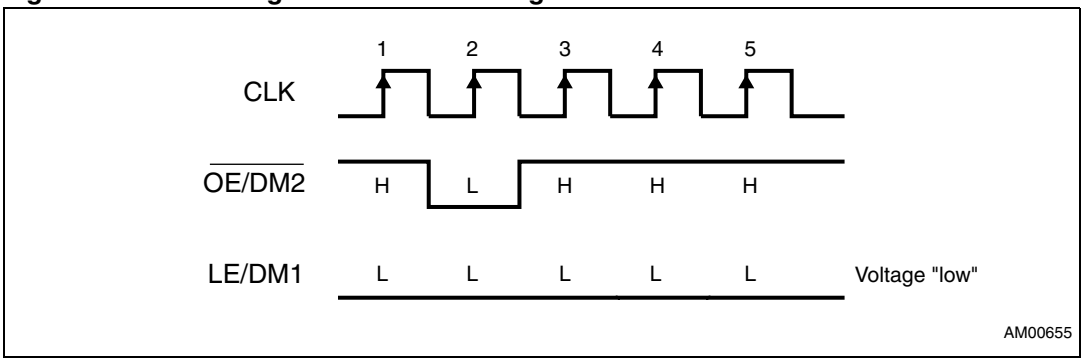


Figure 8 shows the timing sequence necessary to resume normal operation after the LED status acquisition is completed.

Figure 8. Resuming normal mode timing



4 Error detection output test circuit

During the error detection time, the internal structure of the device allows a single output current test. Specifically, the test is performed by comparing the current flowing from the output, to the current set by the R_{EXT} programming resistor.

If the current detected is less than 50% (typ) of the current set by the R_{EXT} resistor, the device marks the output as malfunctioning, and converts the previous data loaded into the shift register from “1” to “0”. Subsequently, these results are transferred as feedback by the SDO pin.

Table 2 shows a typical example of the measured error detection threshold for several output current levels set by the R_{EXT} resistor.

Table 2. Error threshold test results

V_{DD} (V)	I_{SET} (mA)	Measured error threshold (mA)
3.3	1	0.359
	2	0.841
	3	1.36
	5	2.10
	10	4.80
	20	10.2
	40	19.68
5.0	1	0.355
	2	0.831
	3	1.21
	5	2.40
	10	5.00
	20	9.90
	40	19.55

For output error detection to function correctly, all the signals must be synchronized with the falling edge of the CLK signal. This is necessary to avoid any setup\hold time violations.

In some cases, due to application conditions, this cannot be applied (i.e.: data generated by an MCU). To address this, it is possible to switch all of the other signals by applying a 15 ns delay after the rising edge of the CLK signal.

Only one error detection reading can be made within the acquisition time window. For this reason, if two or more readings are required it is necessary the complete the error detection sequence, then repeat each step again.

5 Auto power-saving feature

This section explains the benefits of the auto power-saving feature of the STP16DPPS05 device.

The plot in *Figure 9* shows the I_{DD} supply voltage consumption during normal mode and in the auto power-saving condition.

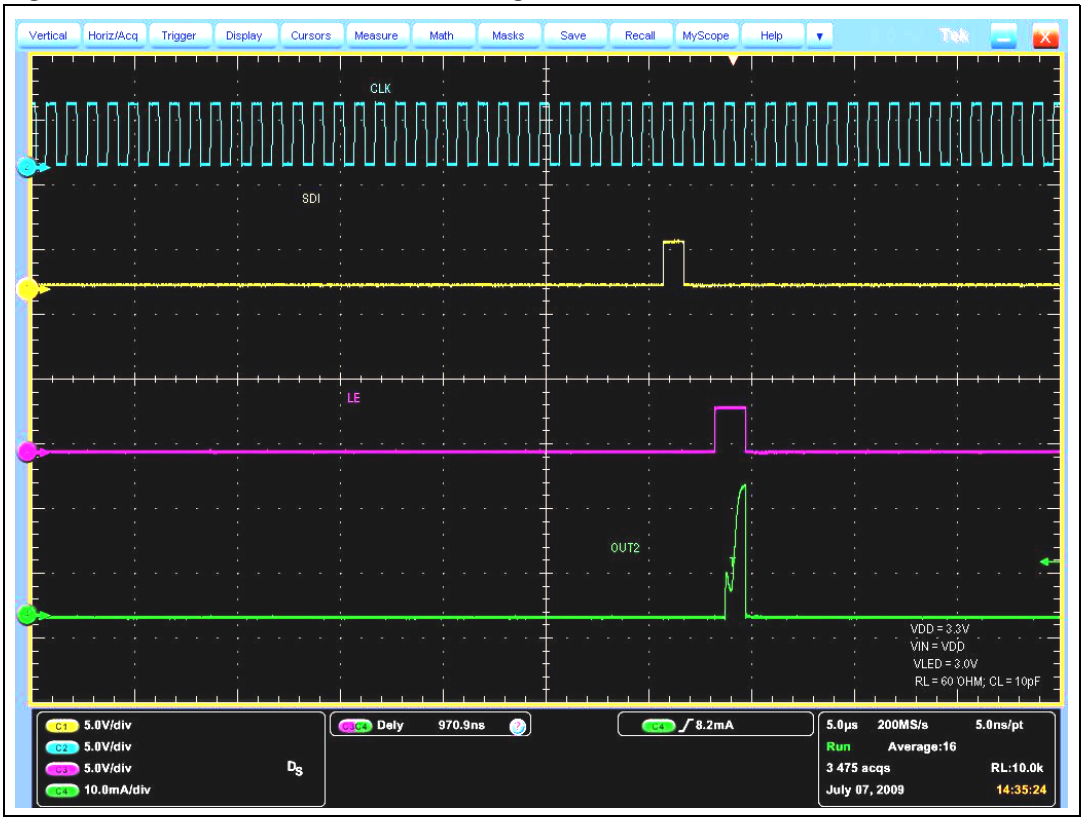
Figure 9. I_{DD} consumption in normal mode and auto power-saving condition



In the plot above, I_{DD} consumption (Ch4 green) falls after 16 CLK pulses (Ch2 blue) if no SDI data (Ch1 yellow) were latched by the LE/DM1 signal (Ch3 purple). When the first active data is available on the SDI pin (Ch1) and is latched by the LE/DM1 signal (Ch3), the device switches from auto power-saving mode to normal mode and I_{DD} consumption rises to typical values.

Figure 10 shows the typical shape of the first output turn-on when the device switches from auto power-saving to normal mode.

Figure 10. First out "ON" after resuming normal mode



The following signals are shown on the plot above:

- Ch1 (yellow) = SDI signal
- Ch2 (blue) = CLK signal
- Ch3 (purple) = LE/DM1
- Ch4 (green) = first output switched on after return from auto power-saving to normal mode

5.1 Value added by the auto power-saving feature

To demonstrate the added benefits provided by the auto power-saving feature, consider a typical application, such as an LED display panel supplied by battery cell, where 100 STP16DPPS05 devices are used.

If the outputs of each device are driven with a 40 mA current capability (R_{EXT} = 497 Ω), the I_{DD} supply current of each device is typically 8 mA.

The LED display supply current (I_{DD}) is:

Total $I_{DD} = I_{DD} \times n$

(Where *n* is the number of STP16DPPS05 devices used).

In this case:

Total I_{DD} (mA) = 0.008 x 100 = 800 mA

Using the power-saving feature, considering that the I_{DD} of one device in shutdown condition is typically 140 µA, the LED display supply current (I_{DD}) is:

Total I_{DD} (mA) = 0.00014 x 100 = 14 mA

As a result:

With all devices in auto-shutdown, the power supply consumption is 1.75% versus normal operating conditions, resulting in power savings of 98.25%.

Usually, when an LED panel is used in standard mode, it is common to have from 15% to 40% of the drivers with no active outputs. Also, in this condition the devices switching from auto power-up to auto-shutdown are able to save power to increase battery time span.

6 Conclusion

The two highlighted features of the STP16DPPS05 generate benefits for a wide range of applications.

The device can provide the MCU with feedback of the overall LED system via the EDM test, which can be managed either locally or remotely through a network.

The STP16DPPS05 is suitable for all applications where power saving is important, such as in traffic panels or electronic advertising, where it is possible to switch off parts of the panels, when not necessary, to increase the battery time span.

7 Revision history

Table 3. Document revision history

Date	Revision	Changes
03-Dec-2009	1	Initial release.

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