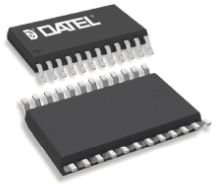
DAC-1212

12-Bit, 125MSPS, Low-Power D/A Converters



FEATURES

- 12-bit resolution
- 125MSPS conversion rate
- 35 ns settling time to ±0.05%
- Operates from single +3V to +5V supply
- Humidity and stress resistant ceramic LCC package for -QL and /883 models
- -40°C to +105°C and -55°C to +125°C operating temperature ranges
- 100% testing over temperature
- High-Rel process flow, burn-in, environmental, lot and ATE traceability
- Low power, 150mW (5V supply) 76mW (+3V supply)
- Internal +1.2V temperature compensated bandgap reference with an external reference option
- Outstanding dynamic performance
- Guaranteed monotonicity over temperature
- ±1 LSB Differential Non-Linearity (Max) over temperature
- ±2 LSB Integral Non-Linearity (Max) over temperature
- TSSOP package (SE,SM models), Pb-free RoHS compliant

PRODUCT OVERVIEW

The 12-bit DAC-1212 is one in a series of high speed pin to pin compatible 8 to 14 bit D/A's from DATEL. This D/A converter offers up to 125MSPS conversion rate from a segmented current source topology that is built on an advanced CMOS process and delivers a low glitch energy output of 2mA to 20mA.

This series is offered in either a small 28-pin TSSOP or a fully hermetic sealed ceramic LCC package. The hermetic package, offered for the –QL and /883 versions, protects the IC from the effects of moisture making the precision DC characteristics of the DAC more stable in environments where humidity is a concern. In addition, the LCC package isolates the IC from the stresses that may occur on the printed circuit board caused by variations in temperature.

The DAC-1212 operates from a single +3V to +5V supply and contains a precision internal 1.2V temperature compensated bandgap voltage reference, external reference option, edge-triggered CMOS input latches and a power-down "sleep" mode. This converter provides excellent dynamic performance making it ideal for applications such as signal reconstruction, high-resolution imaging, cellular base-stations, and medical/test instruments.

DATEL offers these converters fully tested over temperature with ATE results recorded and stored for the operating temperature ranges of -40°C to +105°C (Enhanced) or –55°C to +125°C (military). Burn-in and environmental screening are also available.

Products are offered in military temperature grades as well as fully screened High-Reliability -QL and /883 models.

APPLICATIONS

- MIL-STD/883 systems
- Defense/ aerospace applications
- Signal reconstruction
- High resolution imaging
- Cellular base stations
- Scientific test instruments

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	CLK
2	BIT 2	27	DVDD
3	BIT 3	26	DGND
4	BIT 4	25	AGND
5	BIT 5	24	AVDD
6	BIT 6	23	NC
7	BIT 7	22	IOUTA
8	BIT 8	21	IOUTB
9	BIT 9	20	AGND
10	BIT 10	19	COMP
11	BIT 11	18	GAINADJ
12	BIT 12 (LSB)	17	REFI/O
13	DGND	16	REFSEL
14	DGND	15	SHTDWN

*Pinout TSSOP package

BLOCK DIAGRAM

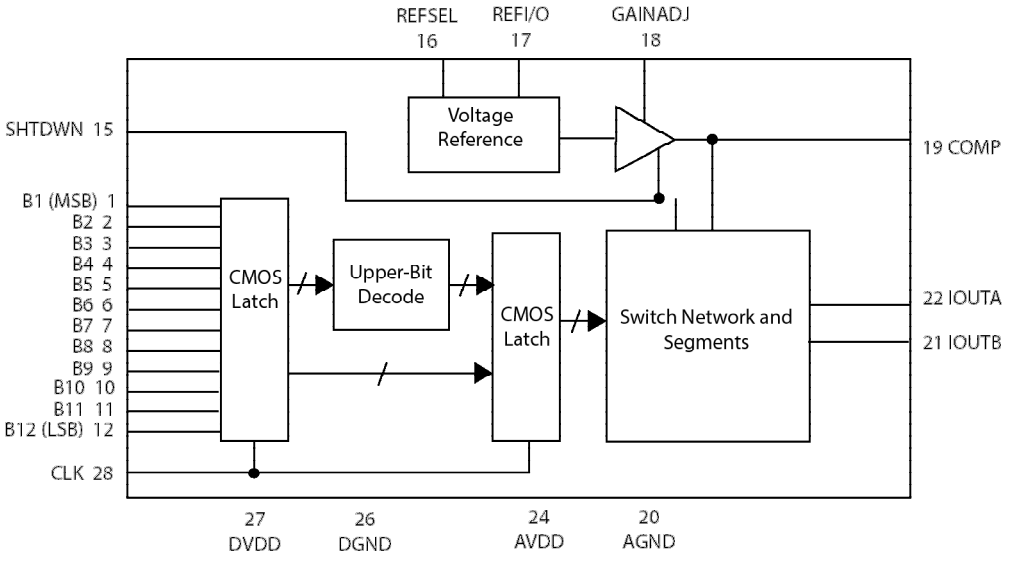


Figure 1. DAC-1212 Functional Block Diagram

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048 USA • Tel: (508) 964-5397 • www.datel.com • e-mail: help@datel.com

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	LIMITS	UNITS
DVDD to DGND (Pins 27/26)	+5.5	Volts
AVDD to AGND (Pins 24/20)	+5.5	Volts
AGND to DGND (Pins 20/26)	-0.3 to +0.3	Volts
Digital Inputs (Pins 1-10, 15,28)	DVDD to DVDD+0.3	Volts
Reference Output Current (Pin 17)	±50µA	Volts
Analog Output Current (21,22)	24mA	°C

Note:
1. Exceeding specifications listed in Absolute Maximum Ratings may cause permanent damage to the device.
2. θja is measured with device soldered to a PCB in still air.

PHYSICAL/ENVIRONMENTAL				
PARAMETERS	MIN.	TYP.	MAX.	UNITS
Operating Temp. Range, Case				
C- suffix	0	—	+70	°C
E - suffix	–40	—	+85	°C
M, QL, 883 - suffix	–55	—	+125	°C
Thermal Impedance				
θja - SOIC package	—	75	—	°C/Watt
θja - TSSOP package	—	135	—	°C/Watt
Maximum Junction Temperature			+150	°C
Storage Temperature Range	–65	—	+150	°C
Maximum Lead Temperature 10s (SOIC lead tipsonly)			+300	°C

FUNCTIONAL SPECIFICATIONS [1]

(Typical at +25°C, AVDD = DVDD = +5V, VREF = Internal, IOUT full scale = 20mA unless otherwise specified.)

DIGITAL INPUT	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Resolution		12			
Logic Levels					
Logic "1"	DVDD = +5V	3.5	5		Volts
Logic "1"	DVDD = +3V	2.1	3		Volts
Logic "0"	DVDD = +5V		0	1.3	Volts
Logic "0"	DVDD = +3V		0	0.9	Volts
Input Current HI		-10		+10	µA
Input Current LO		-10		+10	µA
SHTDWN Input Current		-27		+27	µA
Digital Input Capacitance			3		pf
STATIC PERFORMANCE					
Full Scale Output Current		2		20	mA
Differential Nonlinearity		-1	±0.5	+1	LSB
Integral Nonlinearity	Best Fit Method	-2	±0.5	+2	LSB
Offset Error		-0.025		+0.025	% FSR
Offset Tempco			0.1		ppm FSR/°C
Gain Error[2]	Internal Reference	-10	±0.8	+10	% FSR
Gain Error[2]	External Reference	-10	±1.5	+10	% FSR
Gain Tempco	Internal Reference		±95		ppm FSR/°C
Gain Tempco	External Reference		±45		ppm FSR/°C
Output Compliance Voltage		-0.3		1.25	Volts
Output Capacitance			10		pf
DYNAMIC PERFORMANCE					
Conversion Rate		125			MHz
Output Settling Time	0.05% FSR (±2 LSB)		35		ns
Glitch Area	RL = 25Ω		5		pV/s
Output Rise Time	Full Scale Step		2.4		ns
Output Fall Time	Full Scale Step		2.4		ns
Output Noise	Iout = 2mA		28		pA/√Hz
Output Noise	Iout = 20mA		50		pA/√Hz
Total Harmonic Distortion[5] (AVDD = +5V, DVDD = +5V)					
Fout = 4.0MHz, Fclk = 100MHz	Up to Nyquist		-71		dBc
Fout = 2.0MHz, Fclk = 50MHz	Up to Nyquist		-76		dBc
Fout = 1.0MHz, Fclk = 25MHz	Up to Nyquist		-77		dBc
Spurious Free Dynamic Range[5] (within a window, AVDD = +5V, DVDD = +5V)					
Fout = 20.2MHz, Fclk = 100MHz	30MHz Span		77		dBc
Fout = 5.02MHz, Fclk = 100MHz	8MHz Span		96		dBc
Fout = 5.02MHz, Fclk = 50MHz	8MHz Span		96		dBc
Spurious Free Dynamic Range[5] (up to Nyquist, AVDD = +5V, DVDD = +5V)					
Fout = 40.2MHz, Fclk = 125MHz	Up to Nyquist		56		dBc
Fout = 10.2MHz, Fclk = 125MHz	Up to Nyquist		66		dBc
Fout = 5.02MHz, Fclk = 125MHz,	Up to Nyquist		74		dBc
Fout = 40.2MHz, Fclk = 100MHz	Up to Nyquist		54		dBc
Fout = 20.2MHz, Fclk = 100MHz	Up to Nyquist		63		dBc
Fout = 5.02MHz, Fclk = 100MHz,	Up to Nyquist		74		dBc

DYNAMIC PERFORMANCE (Cont.)	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Fout = 2.52MHz, Fclk = 100MHz,	Up to Nyquist		75		dBc
Fout = 20.2MHz, Fclk = 50MHz,	Up to Nyquist		64		dBc
Fout = 5.02MHz, Fclk = 50MHz,	Up to Nyquist		74		dBc
Fout = 2.52MHz, Fclk = 50MHz,	Up to Nyquist		76		dBc
Fout = 1.02MHz, Fclk = 50MHz,	Up to Nyquist		78		dBc
Fout = 1.02MHz, Fclk = 25MHz,	Up to Nyquist		79		dBc
Multi-Tone Power Ratio (8 Tones, AVDD = +5V, DVDD = +5V)					
Fout=2MHz to 2.9MHz, Fclk = 20 MHz	Tones shifted by 112kHz		76		dBc
Fout=10MHz to 14.9MHz, Fclk=100 MHz	Tones shifted by 112kHz		76		dBc
Total Harmonic Distortion[5] (AVDD = +3V, DVDD = +3V)					
Fout = 4.0MHz, Fclk = 100MHz	Up to Nyquist		-71		dBc
Fout = 2.0MHz, Fclk = 50MHz	Up to Nyquist		-76		dBc
Fout = 1.0MHz, Fclk = 25MHz	Up to Nyquist		-76		dBc
Spurious Free Dynamic Range[5] (within a window, AVDD = +3V, DVDD = +3V)					
Fout = 20.1MHz, Fclk = 100MHz	30MHz Span		73		dBc
Fout = 5.02MHz, Fclk = 100MHz	8MHz Span		93		dBc
Fout = 5.02MHz, Fclk = 50MHz	8MHz Span		93		dBc
Spurious Free Dynamic Range[5] (up to Nyquist, AVDD = +3V, DVDD = +3V)					
Fout = 40.2MHz, Fclk = 125MHz	Up to Nyquist		48		dBc
Fout = 10.2MHz, Fclk = 125MHz	Up to Nyquist		67		dBc
Fout = 5.02MHz, Fclk = 125MHz,	Up to Nyquist		73		dBc
Fout = 40.2MHz, Fclk = 100MHz	Up to Nyquist		49		dBc
Fout = 20.2MHz, Fclk = 100MHz	Up to Nyquist		57		dBc
Fout = 5.02MHz, Fclk = 100MHz,	Up to Nyquist		72		dBc
Fout = 2.52MHz, Fclk = 100MHz,	Up to Nyquist		77		dBc
Fout = 20.2MHz, Fclk = 50MHz,	Up to Nyquist		54		dBc
Fout = 5.02MHz, Fclk = 50MHz,	Up to Nyquist		74		dBc
Fout = 2.52MHz, Fclk = 50MHz,	Up to Nyquist		76		dBc
Fout = 1.02MHz, Fclk = 50MHz,	Up to Nyquist		76		dBc
Fout = 1.02MHz, Fclk = 25MHz,	Up to Nyquist		77		dBc
Multi-Tone Power Ratio (8 Tones, AVDD = +3V, DVDD = +3V)					
Fout=2MHz to 2.9MHz, Fclk = 20 MHz	Tones shifted by 112kHz		75		dBc
Fout=10MHz to 14.9MHz, Fclk=100 MHz	Tones shifted by 112kHz		76		dBc
REFERENCE					
Internal Reference Voltage		1.13	1.2	1.28	Volts
Reference Voltage Drift			±58		ppm/°C
Reference Current Sink/Source			50		µA
Reference Input Impedance			1		MΩ
Reference Input Mutiplying Bandwidth			1.4		MHz

TIMING CHARACTERISTICS	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Data Setup Time[7] (t_{su})			1.5		ns
Data Hold Time[7] (t_{hld})			1.3		ns
Propagation Delay Time[7] (t_{pd})			2.3		ns
Clock (CLK) Pulse Width HI[7]		4			ns
Clock (CLK) Pulse Width LO[7]		4			ns
POWER REQUIREMENTS					
Power Supply Ranges					
AVDD[3]		2.7	5.0	5.5	Volts
DVDD[3]		2.7	5.0	5.5	Volts
Power Supply Currents					
AVDD[4] (3V to 5V)	IOUT = 20mA		24		mA
AVDD[4] (3V to 5V)	IOUT = 2mA		6		mA
DVDD[4]	5V		12		mA
DVDD[4]	3V		6		mA
AVDD Shut-Down Mode	3V or 5V		2.7		mA
Power Dissipation	5V, IOUT = 2mA[4]		80		mW
	5V, IOUT = 20mA[6]		150		mW
	3V, IOUT = 2mA[4]		32		mW
	3V, IOUT = 20mA[6]		76		mW
Power Supply Rejection Ratio		-0.2		+0.2	% FSR/V

1. See Glossary of Specifications
2. Gain Error specified as ratio of output current to current through Rset (pin 18). Ideal ratio = 31.969.
3. For optimal performance, when operating with supply voltages below 3V IOUT should be less than 12mA.
4. fclock = 100MHz, fout = 39MHz.
5. Spectrum Analysis using differential coupled transformer.
6. fclock = 50MHz, fout = 2MHz
7. See Figure 4

TECHNICAL NOTES

Theory of Operation

The DAC-1212 is an 12-bit, 20mA current output, CMOS, digital to analog converter. The maximum conversion rate is 125MSPS with an operating power supply range of +3V to +5V. The design topology incorporates segmented current source circuitry that reduces transient glitches. The upper bits are divided into major current sources of equivalent current. The remaining lower bits are comprised of binary weighted current sources. In the situation where an input waveform to the converter is ramped through all the codes from 0 to 4095, when the lower bit current sources are all on and reach the first upper bit transition, the lower bits all turn off and the first major current source turns on. As the input continues to ramp up, the lower bits will again count up until the next major current source turns on and the lower bits turn off. In earlier D/A architectures the converter had a substantially larger amount of current turning on and off at major code transitions such as ¼, ½, and ¾ scale of the full scale range. The reduction of current switching at these major transitions significantly reduces the overall glitch of the converter thereby improving output settling times and transient spikes.

Digital Inputs / Termination

The DAC-1212 digital inputs are specified to CMOS logic levels. However, lowering the supply voltage to 3V will reduce the logic threshold level and thereby provide TTL compatible inputs. The internal CMOS register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the inputs are driven from 50Ω drivers then 50Ω termination resistors should be located as close to the inputs and DGND as possible.

Voltage Reference

The internal +1.2V voltage reference of the device has a drift specification of ±60 ppm/°C over the full temperature range. It is recommended that a bypass capacitor be placed as close as possible to the REFI/O pin, connected to AGND. The REFSEL (pin 16) selects whether an internal or external reference is used.. The internal reference can be selected if pin 16 is tied low (AGND). If an external reference is desired, then pin 16 should be tied high (AVDD) and the external reference driven into REFI/O, pin 17. The full scale output current of the converter is a function of both the reference voltage and the value of RSET. IOUT should be within the 2mA to 20mA range. Performance may degrade at 2mA FS Iout.
If the internal reference is used, the voltage at GAINADJ (VGAINADJ) will equal approximately 1.16V (pin 18). If an external reference is used, the voltage at GAINADJ will equal the external reference. IOUT Full Scale can be calculated as:

IOUT FS = (VGAINADJ/RSET)x 32

If the full scale output current is set to 20mA by using the internal voltage reference (1.16V) and a 1.86kΩ RSET resistor, then the input coding to output current vs input coding will be as follows:

INPUT CODE / IOUT		
INPUT CODE (B1 - B12)	IOUTA (mA)	IOUTB (mA)
1111 1111 1111	20	0
1000 0000 0000	10	10
0000 0000 0000	0	20

Output Current

IOUTA and IOUTB provide complementary output current. The sum of IOUTA and IOUTB is always equal to the full scale output current minus one LSB. For single-ended applications, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be terminated with an equivalent value resistance or connected to AGND. The voltage developed at the output must not exceed the output voltage compliance range (see specifications). The termination resistor is chosen to produce the desired output voltage:

VOUT = IOUT X RLOAD

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were attained using a 1:1 transformer on the output of the DAC (see Figure 2). With the center tap grounded, the output swing of pins 21 and 22 will be biased at zero volts. It is important to note here that the negative voltage output compliance range limit is -300mV, imposing a maximum of 600mVp-p amplitude with this configuration. The loading as shown in Figure 2 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set t

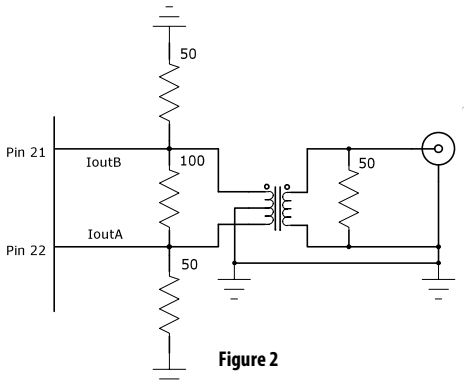


Figure 2

Vout = 2 x Iout x Requivalent. (Requivalent. ~ 12.5Ω)

Ground Planes

If separate DGND and AGND planes are used, then all of the digital functions of the device and the corresponding components should be located over the DGND plane and terminated to the DGND plane. The same is true for the analog components and the AGND. If proper grounding practices are implemented the converter will function properly with a single common ground plane.

Supply Bypassing

To minimize power supply noise, 0.1uF capacitors should be placed as close as possible to the converter's power supply pins, AVDD and DVDD. Be assured that capacitors are bypassed to their proper AGND or DGND planes.

Humidity Susceptibility

Plastic mold compounds that are used to house ICs can absorb moisture. When these devices are exposed to humidity the plastic package can undergo slight changes that can apply pressure to the internal die. Stresses placed on a precision data converters can cause changes in its performance in the order of 100ppm. The fully hermetic package offered for the –QL and /883 versions are not affected by humidity, and are therefore more stable in environments where humidity is a concern.

Board Mounting Considerations

For applications requiring the highest accuracy, attention should be paid to the board mounting location of SE and SM devices. These models use a plastic TSSOP package that could subject the die to mild stresses when the printed circuit board is cooled or heated. Placing the device in areas subject to slight twisting may cause die stresses and consequently degradation in the accuracy of the converter. It is preferred that the device be placed in the center of the PCB or near the edge of the shortest side where stresses due to flexing are reduced. Mounting the device in a cutout also minimizes flex. Mounting the device on an extremely thin PCB or flexprint will increase the potential for loss of accuracy due to stress. The CLCC package offered for -QL and /883 devices eliminates the potential for die stress.

Board Assembly Considerations

Precision converters provide high accuracy over temperature extremes, but some PC board assembly precautions are necessary. Changes in DC parameters can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures, this may reduce device initial accuracy.

PIN DESCRIPTIONS

PIN	PIN NAME	DESCRIPTION
1 -12	BIT 1(MSB) through B12 (LSB)	Digital Data input bits. B1 (MSB), B12 (LSB).
13-14	NC	No Connection. For noise rejection may be tied to AGND.
15	SHTDWN	Control pin to power-down the DAC. Sleep = HI, On = LO. Internal 20µA active pull-down current.
16	REFSEL	Connect to AGND to enable internal 1.2V reference. Connect to AVDD to disable internal reference.
17	REFI/O	Reference voltage output when using internal 1.2V reference Input pin when supplying external reference.
18	GAINADJ	Full Scale current adjustment (gain). Use resistor to AGND to set current (see technical notes).
19	COMP	External capacitor to AGND helps to reduce bandwidth.
20	AGND	Analog Ground
21	IOUTB	Complimentary output current. Full scale is attained when digital inputs are at all 0's.
22	IOUTA	True output current. Full scale is attained when digital inputs are at all 1's.
23	NC	Do not connect. Internal resistive connection to AGND.
24	AVDD	Supply for analog circuitry (typically +3V to +5V).
25	AGND	Analog Ground
26	DGND	Digital Ground
27	DVDD	Supply for digital circuitry (typically +3V to +5V).
28	CLK	Rising edge of clock latches data into input registers thereby updating converter.

GLOSSARY OF SPECIFICATIONS

DIFFERENTIAL LINEARITY ERROR: The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of FSR/2n.

DIFFERENTIAL LINEARITY TEMPCO: The change in differential linearity error with temperature for a data converter, expressed in ppm/°C of FSR (Full Scale Range).

GAIN ERROR: The difference in slope between the actual and ideal transfer functions for a data converter or other circuit. It is expressed as a percent of analog magnitude.

GAIN TEMPCO: The change in gain (or scale factor) with temperature for a data converter or other circuit, generally expressed in ppm/°C.

INTEGRAL LINEARITY ERROR: The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

INTERNAL REFERENCE VOLTAGE DRIFT. The maximum deviation from the measured value at room temperature as compared with the value measured at either Tmin or Tmax.

OUTPUT COMPLIANCE RANGE: The allowable Maximum Voltage at the output of a D/A.

OFFSET ERROR: The deviation from the ideal at analog zero output

OFFSET DRIFT: The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

POWER SUPPLY REJECTION RATIO (PSRR): The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

REFERENCE INPUT MULTIPLYING BANDWIDTH: The -3dB reduction in the output when applying a sinusoidal voltage to the external reference (digital inputs are set to all 1s). The frequency is increased until the amplitude of the output waveform is -3dB of its original value.

SETTLING TIME: The time elapsed from the application of a full scale step input to a circuit to the time when the output has entered and remained within a specified error band around its final value. This term is an important specification for operational amplifiers, analog multiplexers, and D/A converters.

TOTAL HARMONIC DISTORTION: The ratio of the rms sum of the first 5 harmonics to the rms of the fundamental signal, usually expressed in dB

GLITCH AREA: The transient appearing at the output when the input switches from one code to another. Typically the worst case is found at the MSB code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification.

SPURIOUS FREE DYNAMIC RANGE (SFDR): The largest harmonic, spurious frequency or noise component in a signal FFT. It is expressed in db with respect to the fundamental frequency.

TYPICAL CONNECTION DIAGRAM

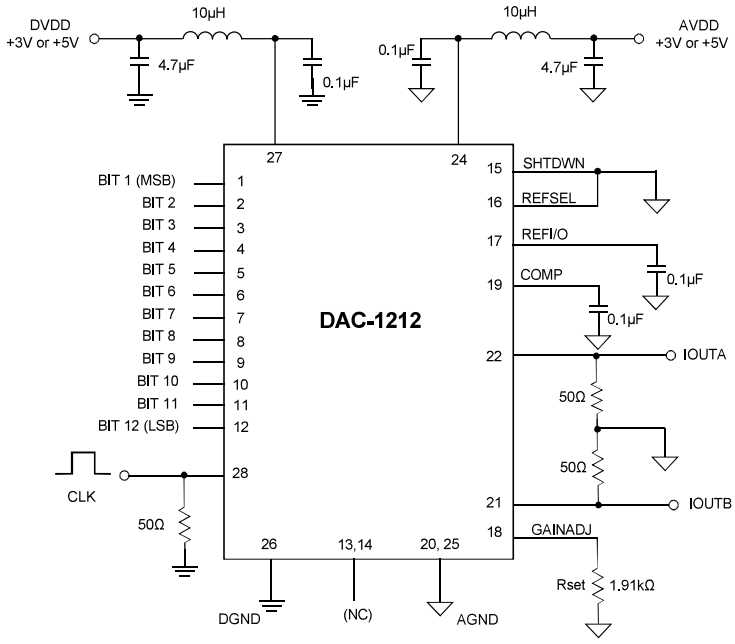


Figure 3. Typical Connection Diagram

TIMING DIAGRAM

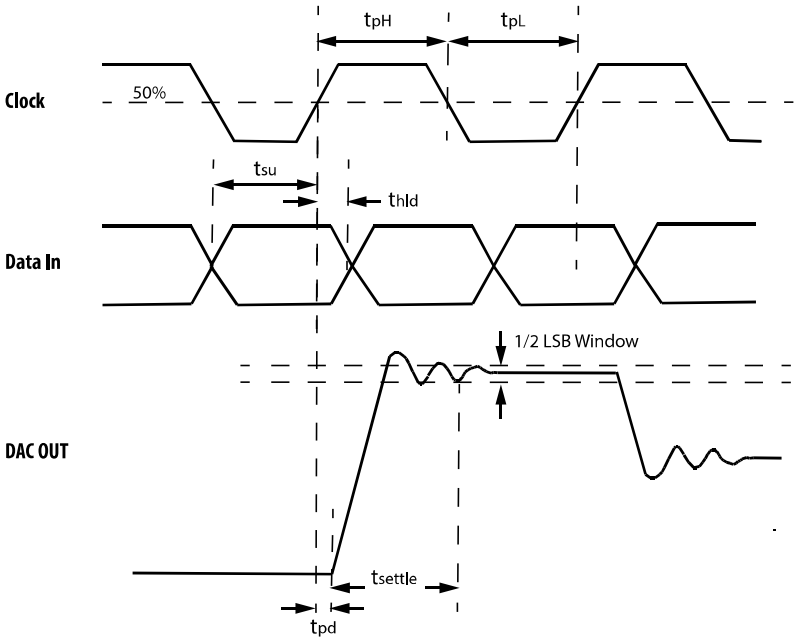


Figure 4. Timing / Settling Diagram

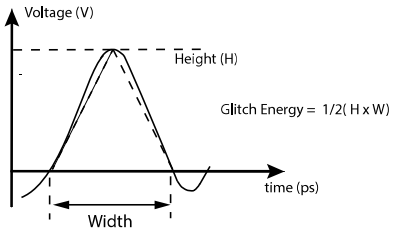
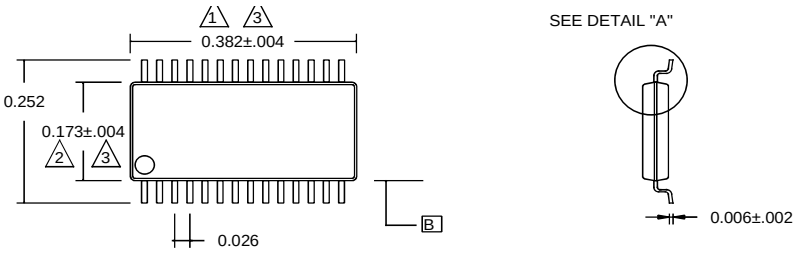
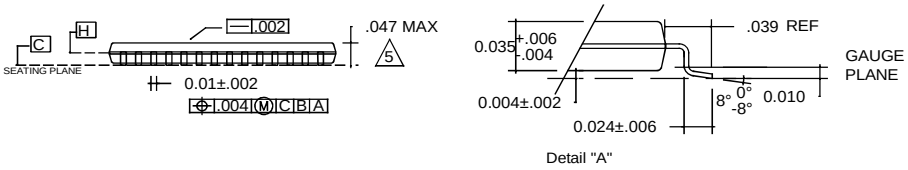
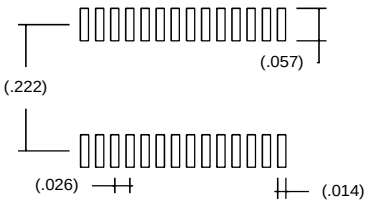


Figure 5. Peak Glitch Area

MECHANICAL DIMENSIONS - INCHES (mm)







1. Dimension does not include mold flash, protrusions or gate burrs
   Mold flash, protrusions or gate burrs shall not exceed 0.006 per side
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.010 per side
3. Dimension are measured at datum plane H

Dimension and tolerancing per ASME Y14.5M-1994.

5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.003in total in excess of dimension at maximun material condition. Minimum space between protrusion and adjacent lead is 0.003in.

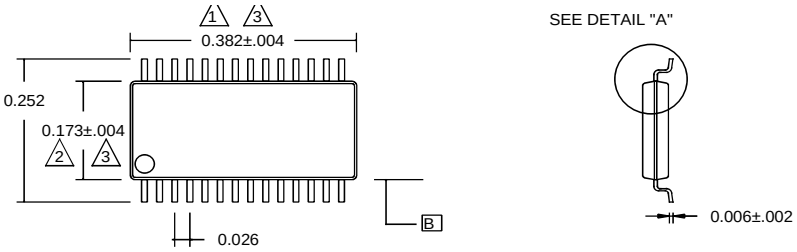
Dimensions in ( ) are for reference only

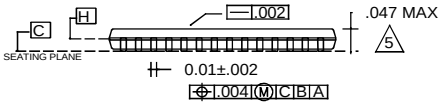
Conforms to JEDEC MO-153

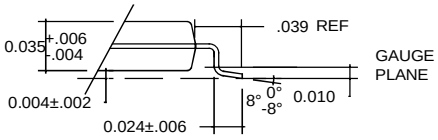
ORDERING INFORMATION

ORDERING INFORMATION			
MODEL NUMBER	OPERATING TEMP. RANGE (°C)	PACKAGE	SHIPPING
DAC-1212SE	-40 to +105	28 Pin TSSOP	Tube
DAC-1212SM	-55 to +125	28 Pin TSSOP	Tube
DAC-1212-QL	-55 to +125	Ceramic LCC	Tray
DAC-1212/883	-55 to +125	Ceramic LCC	Tray

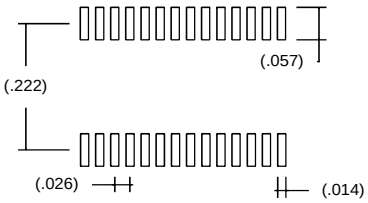
MECHANICAL DIMENSIONS - INCHES (mm)







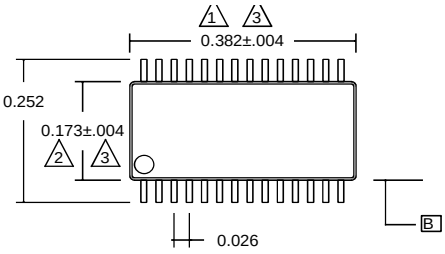
Detail "A"

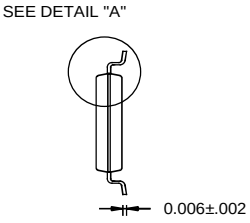


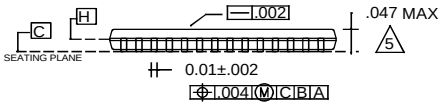
1. Dimension does not include mold flash, protrusions or gate burrs
   Mold flash, protrusions or gate burrs shall not exceed 0.006 per side
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.010 per side
3. Dimension are measured at datum plane H
   Dimension and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.003in total in excess of dimension at maximun material condition. Minimum space between protrusion and adjacent lead is 0.003in.

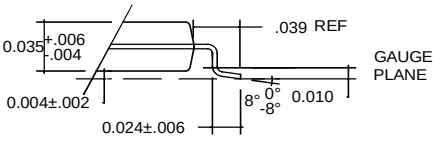
Dimensions in ( ) are for reference only

Conforms to JEDEC MO-153

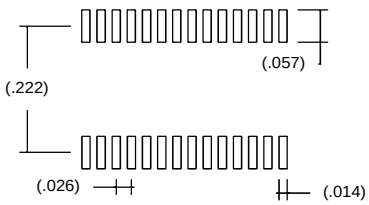








Detail "A"



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