FAN8006D3

4-CH Motor Driver

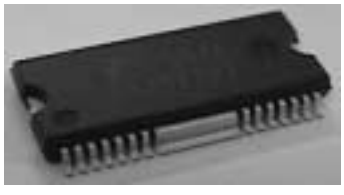
Features

- 4-Channel BTL (Balanced transformer-less) driver
- Built-in thermal shutdown circuit
- Built-in power save circuit
- Separated power supply
- Operating supply voltage: 4.5V ~ 13.2V
- Corresponds to 3.3V or 5V DSP

Description

The FAN8006D3 is a monolithic integrated circuit, suitable for 4-CH motor driver which drives focus actuator, tracking actuator, sled motor and loading motor of a CD-media system.

28-SSOPH-375SG2



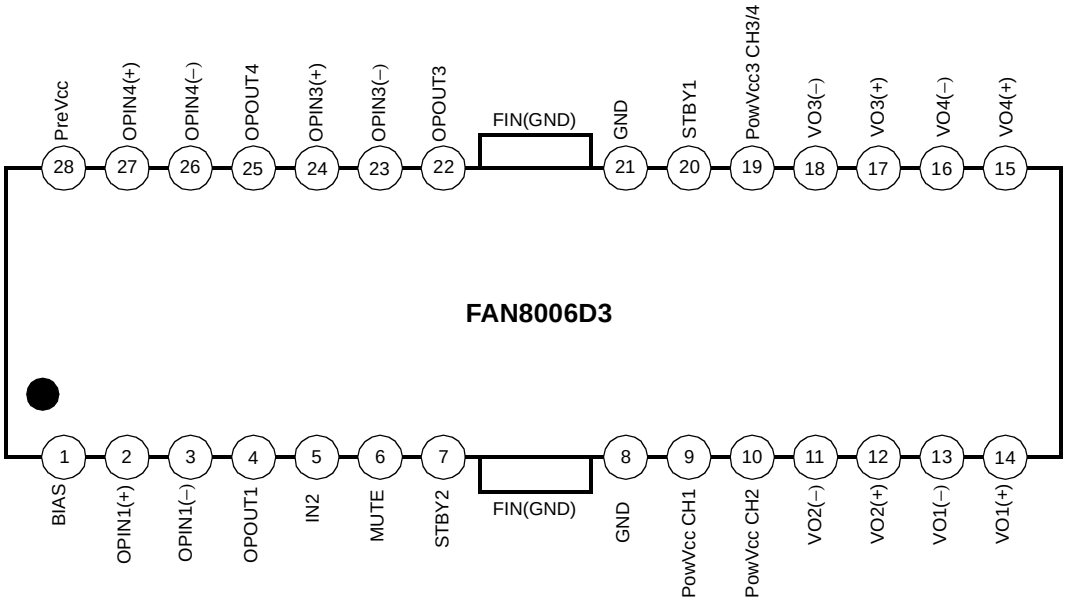
Target Application

- Compact disk player
- Digital video disk player
- Compact disk ROM

Ordering Information

Device	Package	Ope. Temp.
FAN8006D3	28-SSOPH-375SG2	–35°C ~ +85°C
FAN8006D3TF	28-SSOPH-375SG2	–35°C ~ +85°C

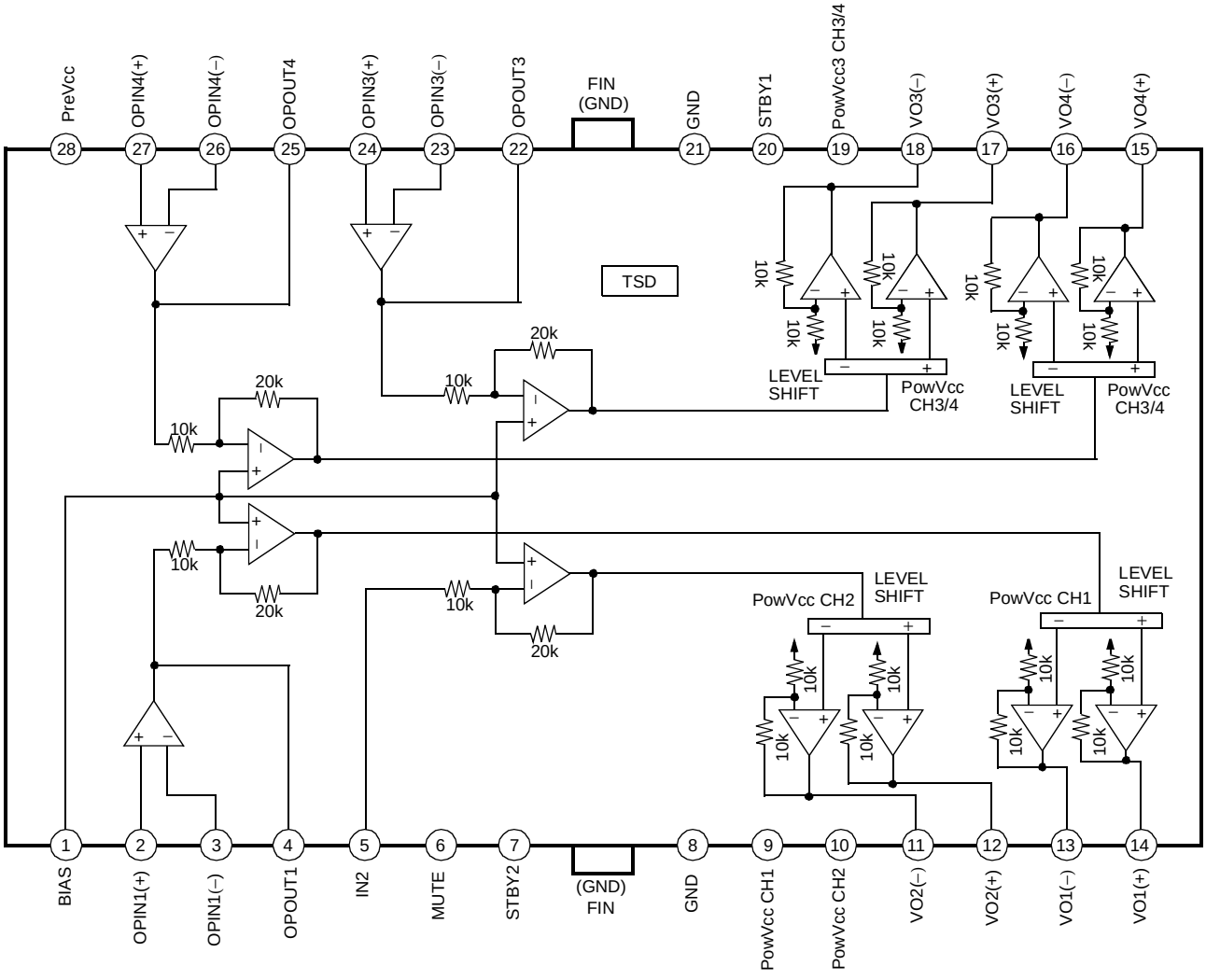
FAN8006D3 Pin Assignments



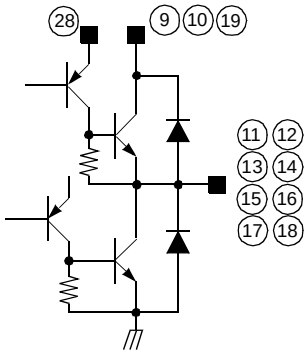
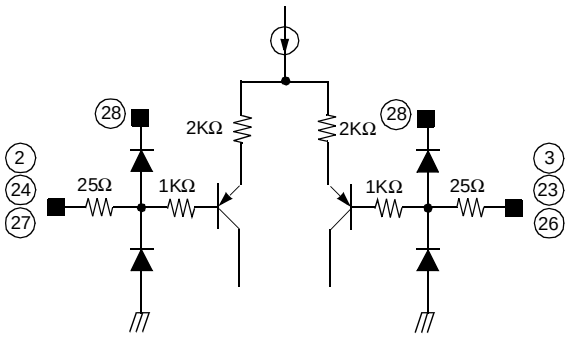
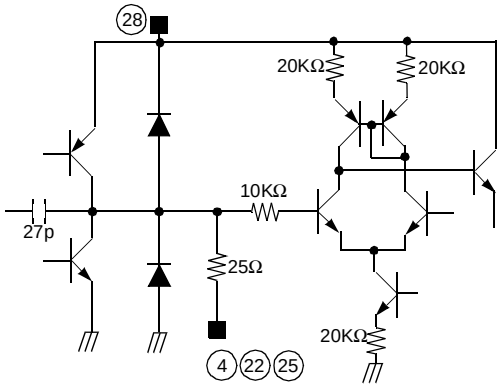
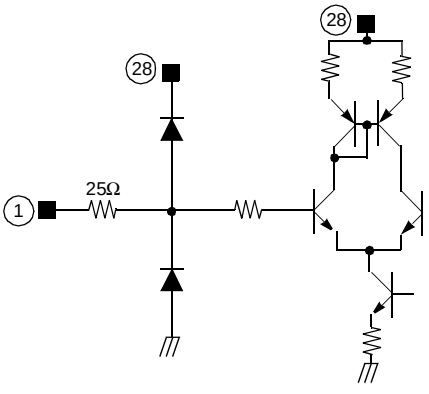
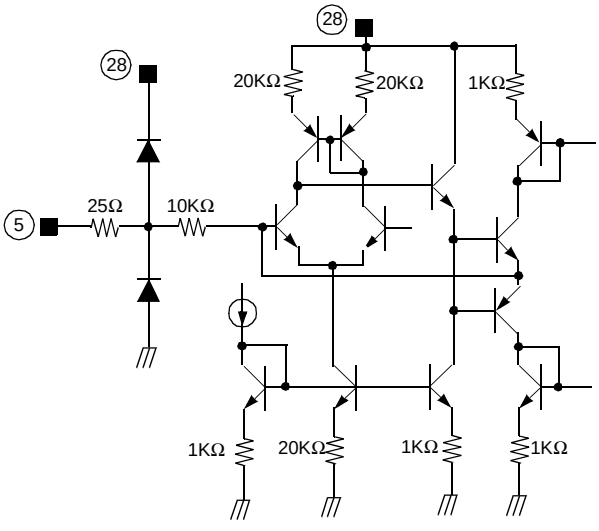
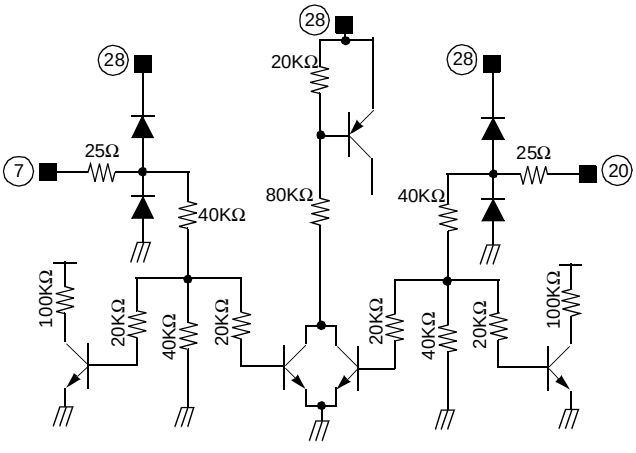
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	BIAS	I	Bias voltage input
2	OPIN1(+)	I	Op-amp CH1 input (+)
3	OPIN1(–)	I	Op-amp CH1 input (–)
4	OPOUT1	O	Op-amp CH1 output
5	IN2	I	CH2 input
6	MUTE	I	CH1 mute control when STBY1 is logic high
7	STBY2	I	CH2 standby control
8	GND	-	Signal ground
9	PowVcc1 CH1	-	BTL CH1 power supply
10	PowVcc2 CH2	-	BTL CH2 power supply
11	VO2(–)	O	Drive2 output (–)
12	VO2(+)	O	Drive2 output (+)
13	VO1(–)	O	Drive1 output (–)
14	VO1(+)	O	Drive1 output (+)
15	VO4(+)	O	Drive4 output (+)
16	VO4(–)	O	Drive4 output (–)
17	VO3(+)	O	Drive3 output (+)
18	VO3(–)	O	Drive3 output (–)
19	PowVcc3 CH3/4	-	BTL CH3/4 power supply
20	STBY1	I	Input for CH1/3/4 standby control
21	GND	-	Ground
22	OPOUT3	O	Op-amp CH3 output
23	OPIN3(–)	I	Op-amp CH3 input (–)
24	OPIN3(+)	I	Op-amp CH3 input (+)
25	OPOUT4	O	Op-amp CH4 output
26	OPIN4(–)	I	Op-amp CH4 input (–)
27	OPIN4(+)	I	Op-amp CH4 input (+)
28	PreVcc	-	Vcc for pre block

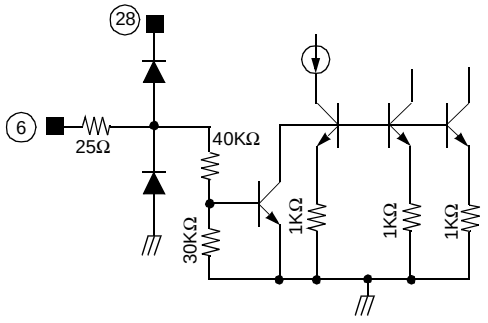
Internal Block Diagram



Equivalent Circuits (Continued)

POWER OUTPUT	CHANNEL OPAMP INPUT
	
CHANNEL OP-AMP OUTPUT	**BIAS INPUT**
	
CHANNEL 2 INPUT	**STANDBY 1/2 INPUT**
	

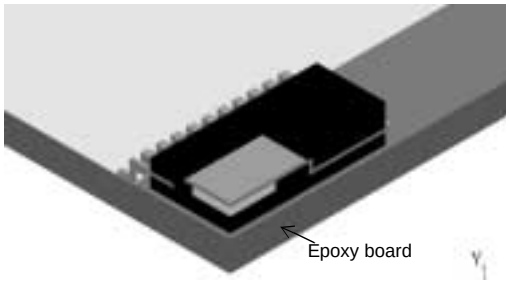
Equivalent Circuits

MUTE INPUT	
	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum supply voltage	$PreV_{ccmax}$	15	V
Power dissipation	P_D	2.5[note]	W
Operating temperature range	T_{OPR}	–35 ~ +85	°C
Storage temperature range	T_{STG}	–55 ~ +150	°C

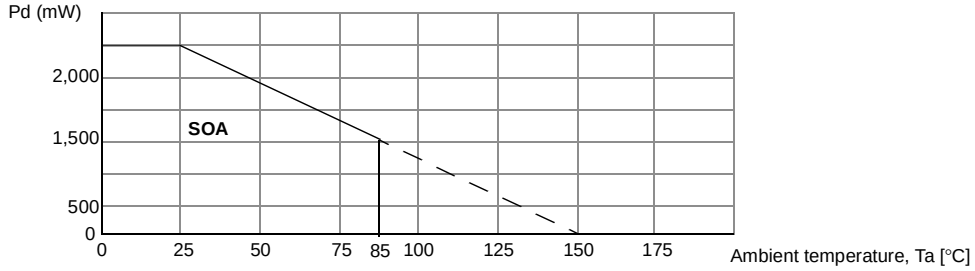
NOTE:



Pd is measured base on the JEDEC/STD(JESD 51-2)

Pd=2.5W

1. Test PCB is single layer PCB which has only 1 signal plane. PCB size is 76mm × 114mm × 1.6mm.
2. Power dissipation is reduced for using above Ta=25°C. It's slope is -20.0mW/°C.
3. Do not exceed P_D and SOA (Safe Operating Area).



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	PreVcc	4.5	-	13.2	V
Supply voltage	PowVcc CH1	4.5	-	PreVcc	V
Supply voltage	PowVcc CH2	4.5	-	PreVcc	V
Supply voltage	PowVcc CH3/4	4.5	-	PreVcc	V

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, $PreV_{CC}$=12V, PowVcc CH1=PowVcc CH3/4=5V, PowVcc CH2=12V, RL=8Ω,24Ω)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent current1	I_{CC1}	STBY1,2=0.5V,Mute=2V,RL=∞	-	0.1	1	mA
Quiescent current2	I_{CC2}	STBY1,2=2V,Mute=0.5V,RL=∞	-	22.0	31.0	mA
Quiescent current3	I_{CC3}	STBY2=2V, STBY1,Mute=0.5V	-	5.5	8.5	mA
Quiescent current4	I_{CC4}	STBY2=0.5V, STBY1,Mute=2V	-	12.0	17.0	mA
Quiescent current5	I_{CC5}	STBY2,Mute=0.5V,STBY1=2V,	-	17.5	24.5	mA
Mute on voltage	V_{MON}	-	2.0	-	-	V
Mute off voltage	V_{MOFF}	-	-	-	0.5	V
STBY1 on voltage	V_{STON1}	-	-	-	0.5	V
STBY1 off voltage	V_{STOFF1}	-	2.0	-	-	V
STBY2 on voltage	V_{STON2}	-	-	-	0.5	V
STBY2 off voltage	V_{STOFF2}	-	2.0	-	-	V
BTL DRIVE CIRCUIT						
Channel 1,3,4(RL=8Ω)						
Output offset voltage 1,3,4	$V_{OF1,3,4}$	-	–50	-	+50	mV
Maximum output voltage 1,3,4	$V_{OM1,3,4}$	-	3.6	4.0	-	V
Closed loop voltage gain 1,3,4	$G_{VC1,3,4}$	-	17	18	19	dB
Ripple rejection ratio 1,3,4	$RR_{1,3,4}$	-	-	60	-	dB
Slew rate 1,3,4	$SR_{1,3,4}$	-	-	1	-	V/µs
Channel 2(RL=24Ω)						
Output offset voltage 2	V_{OF2}	-	–50	-	+50	mV
Maximum output voltage 2	V_{OM2}	-	9.5	10.5	-	V
Closed loop voltage gain 2	G_{VC2}	-	17	18	19	dB
Ripple rejection ratio 2	RR_2	-	-	60	-	dB
Slew rate 2	SR_2	-	-	1	-	V/µs
INPUT OP-AMP						
Input offset voltage	V_{OFOP}	-	–10	-	+10	mV
Input bias current	I_{BOP}	-	-	-	400	nA
High level output voltage	V_{OHOP}	PreVcc=5V, RL=∞	4.5	-	-	V
Low level output voltage	V_{OLOP}	PreVcc=5V, RL=∞	-	-	0.5	V
Output sink current	I_{SINK}	PreVcc=5V, RL=50Ω	3	-	-	mA
Output source current	I_{SOURCE}	PreVcc=5V, RL=50Ω	2	-	-	mA
Open loop voltage gain	G_{VO}	V_{IN}= -75dB, 1KHz	-	75	-	dB
Ripple rejection ratio	RR_{OP}	V_{IN}= 120KHz, $2V_{PP}$	-	60	-	dB
Slew rate	SR_{OP}	V_{IN}= -20dB, 120Hz	-	1	-	V/µs
Common mode rejection ratio	CMRR	V_{IN}= -20dB, 1KHz	-	80	-	dB
Common mode input range	CMIR	PreVcc=5V	-0.3	-	4	V

Application Information

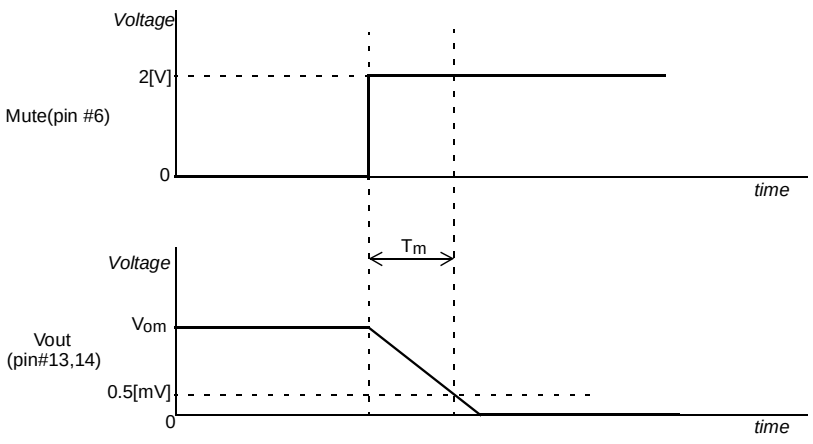
1. Standby/Mute Input

FAN8006D3 have 2 independent standby inputs that is , pin #7(STBY2) and pin #20(STBY1), and 1 independent mute input(pin #7). The digital logics of these functions are as below.

	STBY1=>Low		STBY1=>High		STBY2	
	Mute=>Low	Mute=>High	Mute=>Low	Mute=>High	High	Low
CH 1	standby		operate	high impedance	-	-
CH3/4				operate	-	-
CH2	-	-	-	-	operate	standby

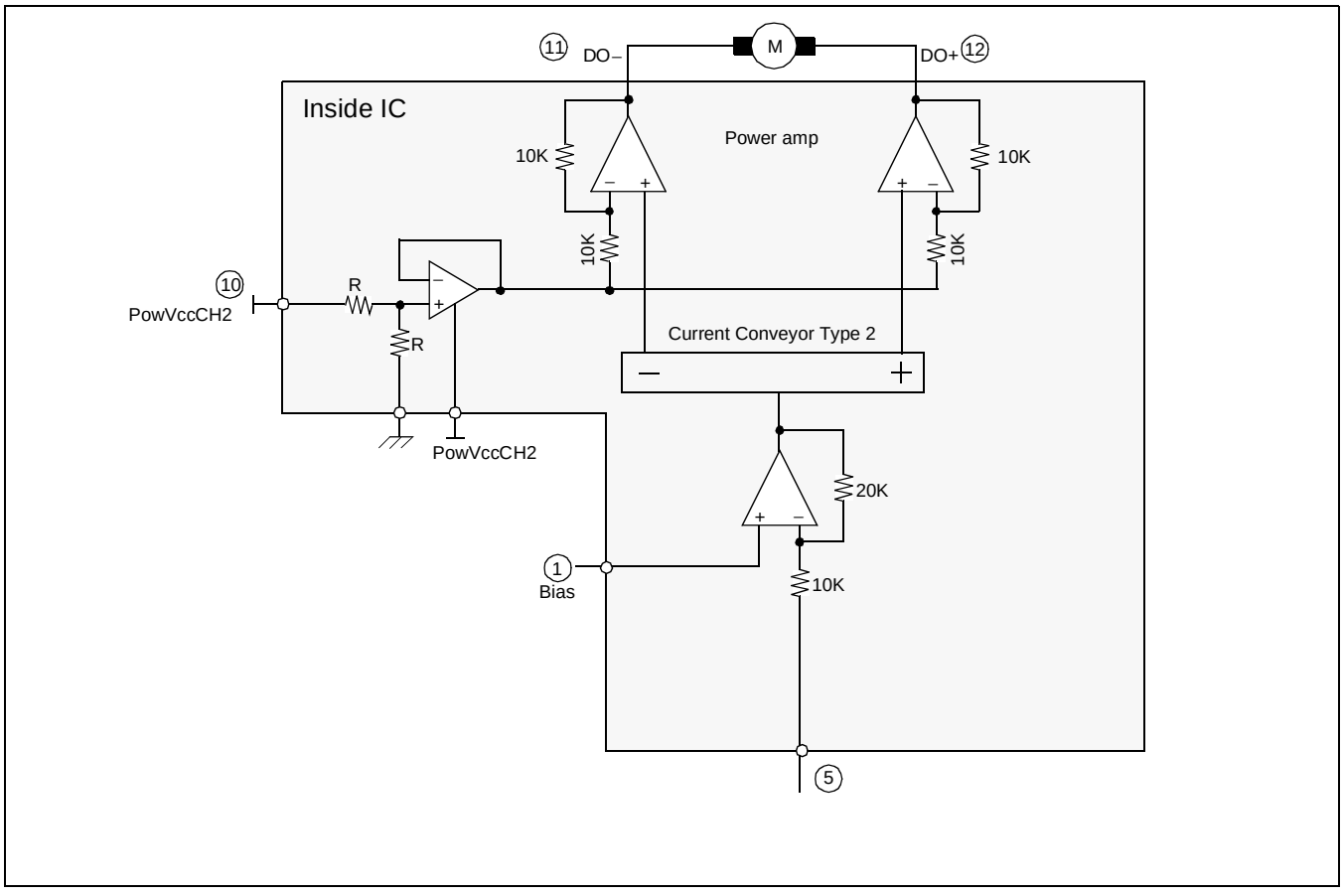
2. Mute Timing Chart

If the mute input(pin #6) voltage rises above 2.0V, the output(CH1) current can be muted under normal operating conditions, make sure to open pin #7 or pull it down below 0.5V. Below figure is high impedance mute timing chart.



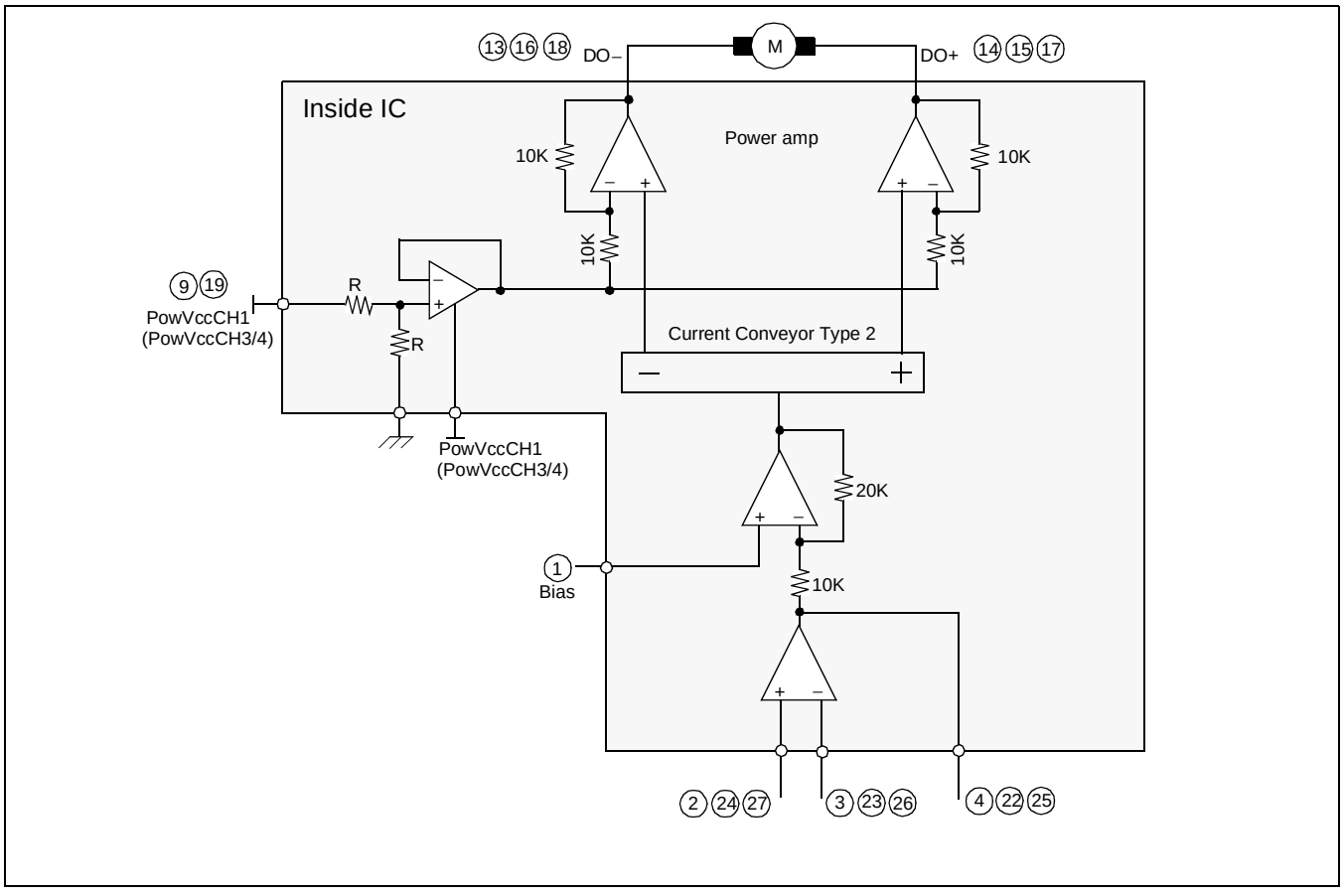
PreVcc = 12V
PowVcc CH1= 5V
BIAS = 1.65V
RL = 8Ω
$T_m \leq 125\mu sec$

3. CH2 Drive Output Schematic



- The reference voltage BIAS is given externally through pin 1.
- The input signal is amplified by (20K/10K) times and then fed to the current conveyor type 2 circuit and the power amp circuit.
- The power amp circuit produces the differential output voltages and drives two output power amplifier circuits.
- Since the differential gain of the power amplifier is equal to $2 \times (1+10K / 10K)$, the output signal of the input OP-amp is amplified totally 8.
- If the total gain is insufficient or large, external resistor can be used to adjust the gain.

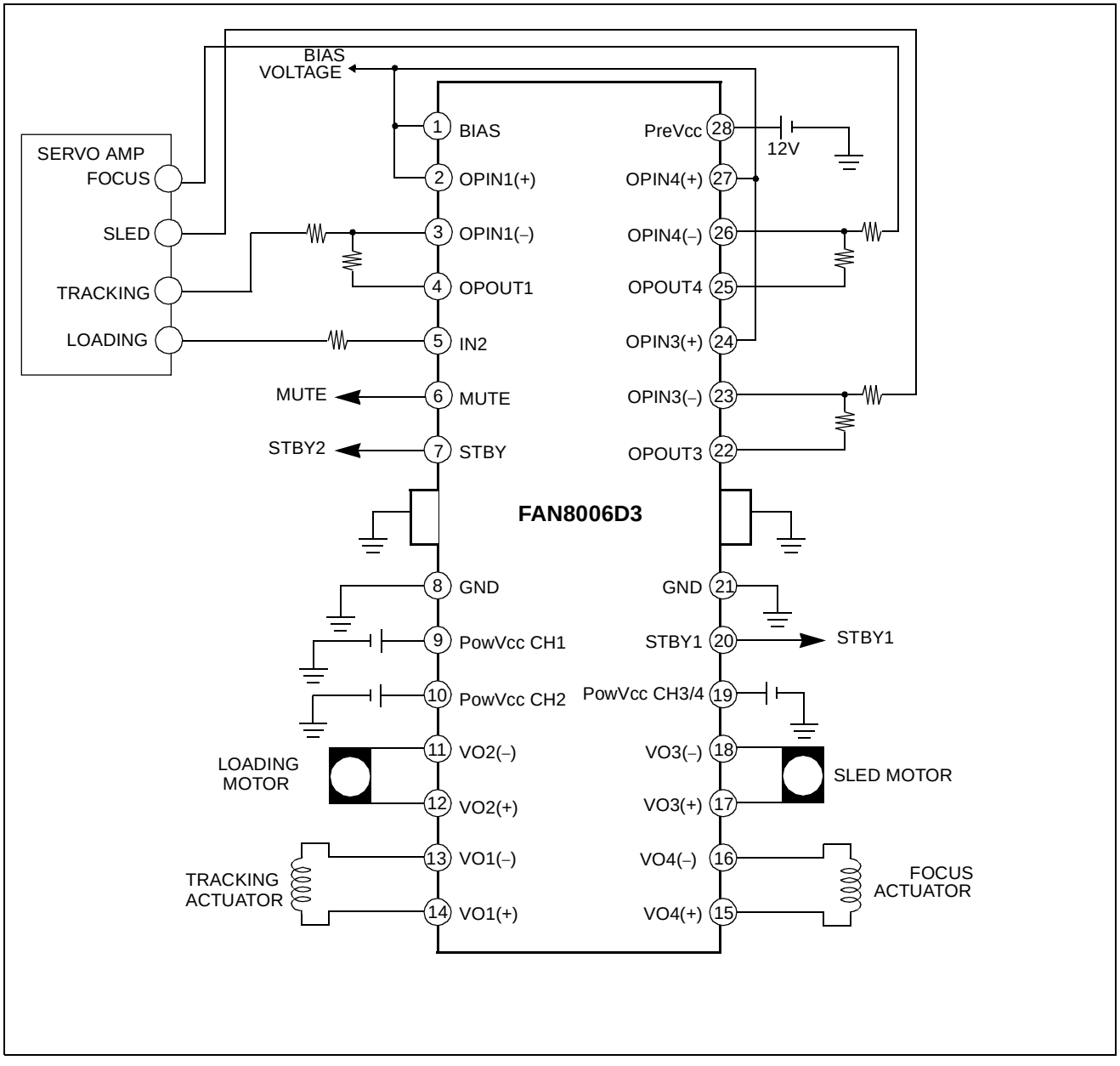
4. CH1/3/4 Drive Output Schematic



- The reference voltage BIAS is given externally through pin 1.
- The input OP-amp output signal is amplified by (20K/10K) times and then fed to the current conveyor type 2 circuit and the power amp circuit.
- The power amp circuit produces the differential output voltages and drives two output power amplifier circuits.
- Since the differential gain of the power amplifier is equal to $2 \times (1+10K / 10K)$, the output signal of the input OP-amp is amplified totally 8.
- If the total gain is insufficient or large, the input OP-amp and the external resistors can be used to adjust the gain.

Application Circuits

(Voltage control mode)



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