24V, 4A Asynchronous Boost Converter

Features

- Wide 2.6V to 6V Input Voltage Range
- Built-in 125mΩ N-Channel MOSFET
- Built-in Adjustable Soft-Start Function
- High Efficiency up to 90%
- Current-Mode Operation
  - Stable with Ceramic Output Capacitors
  - Fast Transient Response
- Current-Limit Protection
- Over-Temperature Protection with Hysteresis
- Built in EN Function For Timing Control
- Selectable Frequency 600kHz/1.2MHz
- Available in TDFN3x3-10 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Panel
- IEEE1394 Port
- Thunderbolt Application
- Boost Regulators

General Description

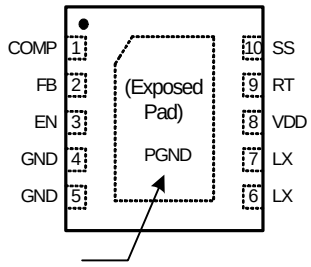
The APW7272 is a asynchronous rectifier, fixed switching frequency (600kHz or 1.2MHz typical), and current-mode step-up regulator. The device allows use of small inductors and output capacitors. The current-mode control scheme provides fast transient response and good output voltage accuracy.

At light loads, the APW7272 will automatically enter in Pulse Skip Mode (PSM) operation to reduce the dominant switching losses. During PSM operation, the IC consumes very low quiescent current and maintains high efficiency over the complete load range.

The APW7272 also includes current-limit and over-temperature shutdown to prevent damage in the event of an output overload.

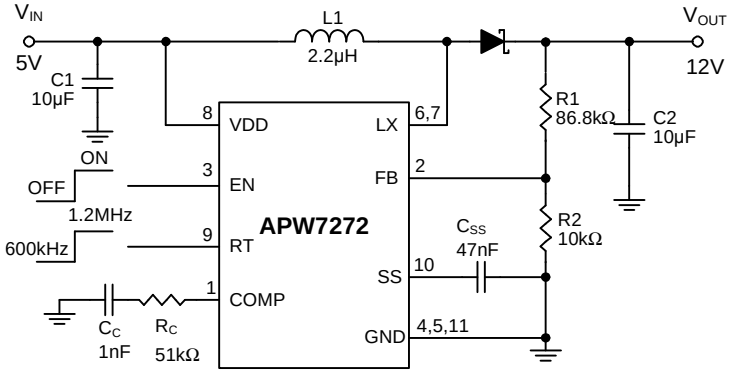
The APW7272 is available in 3mmx3mm TDFN3x3-10 package.

Pin Configuration



TDFN3x3-10 (Top View)

Simplified Application Circuit



Ordering and Marking Information

APW7272 □□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN3x3-10 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7272 QB : 	X - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Converter Supply Voltage (V_{DD} to GND)	-0.3 ~ 7	V
V_{LX}	LX to GND Voltage	-0.3 ~ 28	V
	COMP, FB, EN, RT, SS to GND Voltage	-0.3 ~ 7	V
	PGND to GND (4,11: Signal GND, 5: PGND)	-0.3 ~ +0.3	V
P_D	Power Dissipation	Internally Limited	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TDFN3x3-10	55
θ_{JC}	Junction-to-Case Resistance	TDFN3x3-10	20

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{OUT}	Output and IC Supply Voltage (V_{OUT} to GND)	2.6 ~ 24	V
V_{DD}	Converter Supply Voltage (V_{DD} to GND)	2.6 ~ 5.5	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Please refer to the typical application circuit.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over. V_{DD}=3.3V, V_{OUT}=12V, T_A=25°C.

Symbol	Parameter	Test Conditions	APW7272			Unit
			Min.	Typ.	Max.	
SUPPLY VOLTAGE AND CURRENT						
V_{DD}	Converter Supply Voltage Range		2.6	-	5.5	V
	Converter Supply Voltage Range	18V < V_{OUT} < 24V	4	-	5.5	V
V_{OUT}	Converter Output Voltage		2.6	-	24	V
V_{UVLO}	V_{DD} Under Voltage Lockout Threshold	V_{DD} Rising	2.2	2.4	2.6	V
	V_{DD} Under Voltage Lockout Hysteresis	V_{DD} Falling	-	0.2	-	V
I_{DD1}	No Switching Quiescent Current	V_{FB} = 1.3V	-	0.5	-	mA
I_{DD2}	Switching Quiescent Current	V_{FB} = 1V	-	4	-	mA
I_{DD3}	Shutdown Quiescent Current	EN=GND	-	0.2	4	uA
ERROR AMPLIFIER						
V_{REF}	Regulated Feedback Voltage		1.22	1.24	1.26	V
I_{FB}	FB Input Leakage Current	V_{FB}=1.3V	-100	-	100	nA
	FB Line Regulation	V_{DD}=2.7~5.5V, I_{OUT}=0.2A	-	-0.05	-	%/V
R_{SENSE}	Current Sense Transresistance		-	0.25	-	V/A
gm	Compensation Network	V_{DD}=3.3V~5V	-	135	-	uA/V
	COMP Pull Low Resistance	EN=GND	-	1	-	kΩ
INTERNAL POWER SWITCH						
F_{OSC}	Switching Frequency	RT=GND	450	600	750	kHz
		RT=V_{DD}	900	1200	1500	kHz
R_{N-FET}	N-FET Switch On Resistance	V_{DD}=3.3V	-	125	150	mΩ
	N-FET Current Limit	V_{DD}=3V~5.5V	4	5	6	A
D_{MAX}	SW Maximum Duty Cycle		85	90	95	%
	Minimum On-time		-	150	-	ns
	LX Leakage Current	V_{LX}=24V, V_{FB}=1.3V	-	1	10	uA

Electrical Characteristics

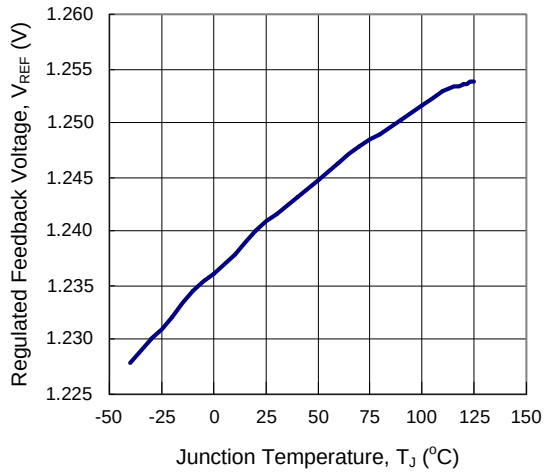
Refer to the typical application circuits. These specifications apply over. V_{DD}=3.3V, V_{OUT}=12V, T_A=25°C.

Symbol	Parameter	Test Conditions	APW7272			Unit
			Min.	Typ.	Max.	
SOFT-START						
I_{SS}	SS Charge Current		-	4	-	uA
CONTROL STAGE						
EN	EN Input Low Threshold		-	-	0.8	V
	EN Input High Threshold		1.8	-	-	V
RT	RT Input Low Threshold		-	-	0.8	V
	RT Input High Threshold		1.8	-	-	V
PROTECTION						
T_{OTP}	Over Temperature Protection (note 4)	T_J Rising	-	150	-	°C
	Over Temperature Protection Hysteresis(note 4)	T_J Falling	-	30	-	°C

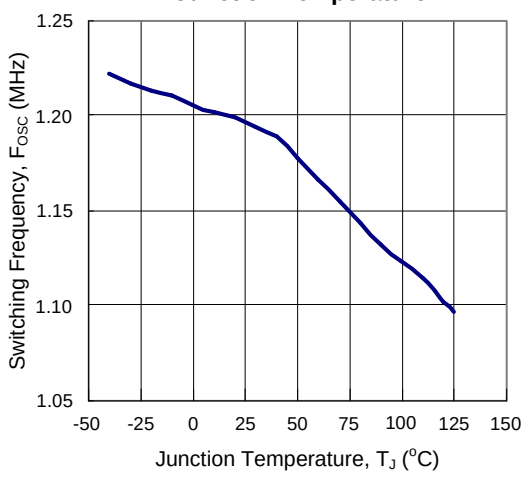
Note 4: Guaranteed by design, not production tested.

Typical Operating Characteristics

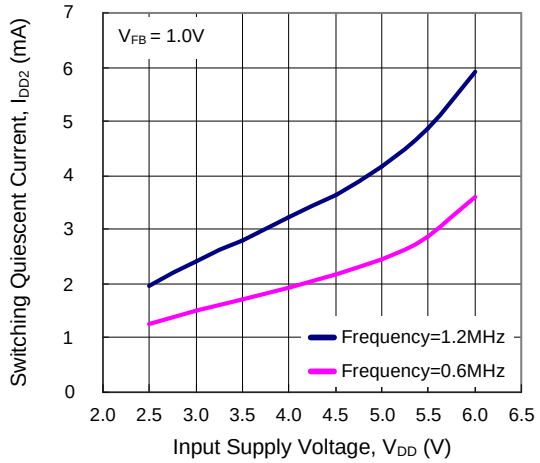
Regulated Feedback Voltage vs. Junction Temperature



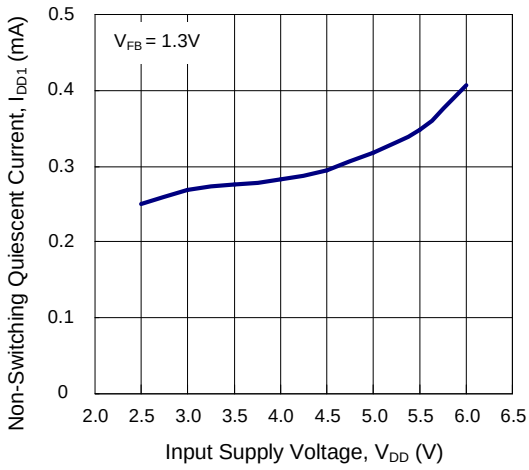
Switching Frequency vs. Junction Temperature



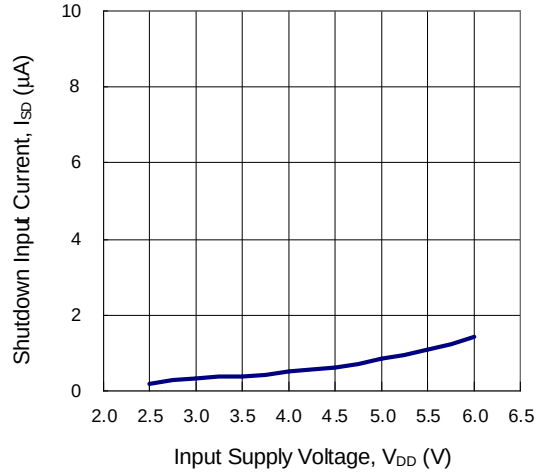
Switching Quiescent Current vs. Input Supply Voltage



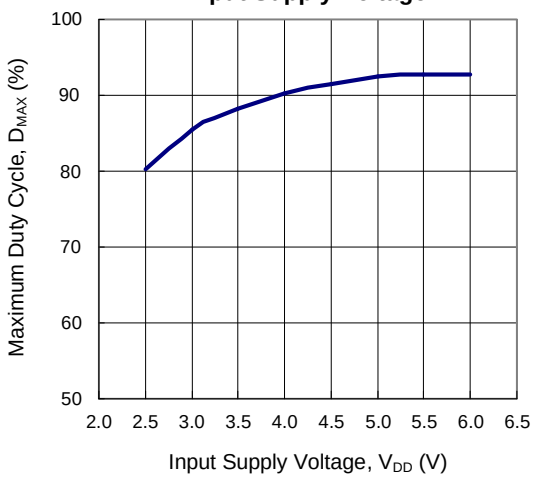
Non-Switching Quiescent Current vs. Input Supply Voltage



Shutdown Quiescent Current vs. Input Supply Voltage

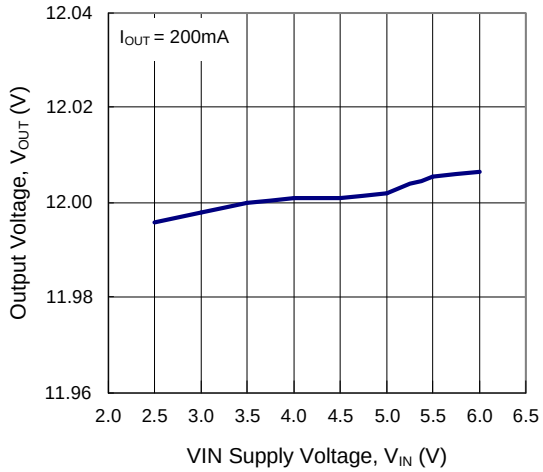


Maximum Duty Cycle vs. Input Supply Voltage

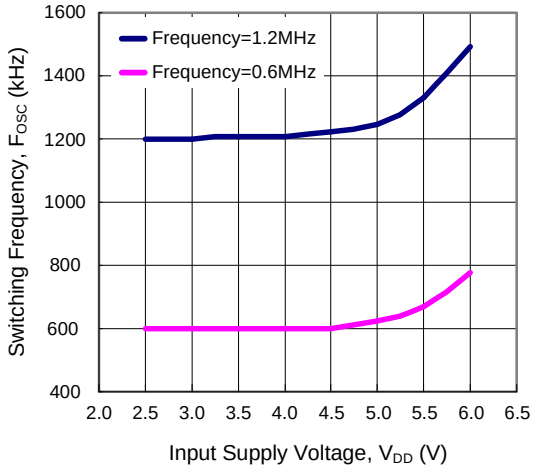


Typical Operating Characteristics (Cont.)

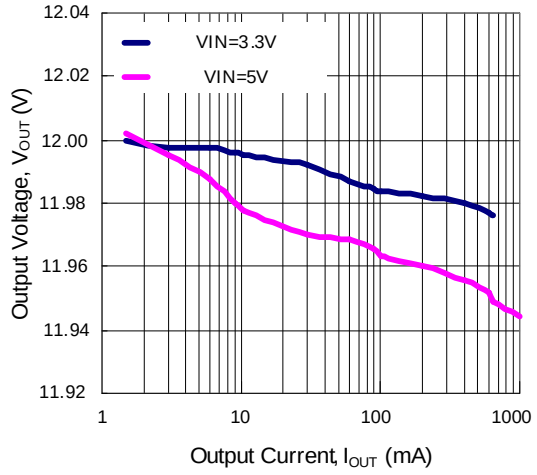
Output Voltage vs. VIN Supply Voltage



Switching Frequency vs. Input Supply Voltage



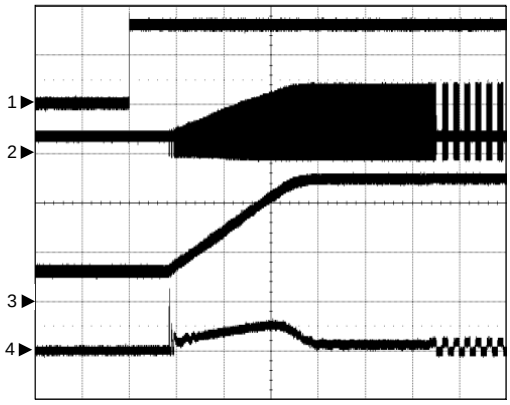
Output Voltage vs. Output Current



Operating Waveforms

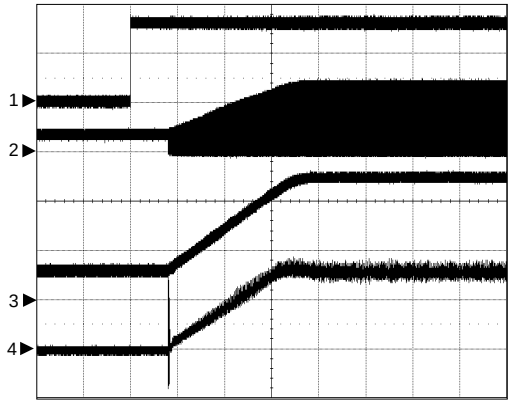
(Refer to the section “Typical Application Circuits”, V_{IN}=3.3V, T_A=25°C, unless otherwise specified)

Start-up at PSM Condition



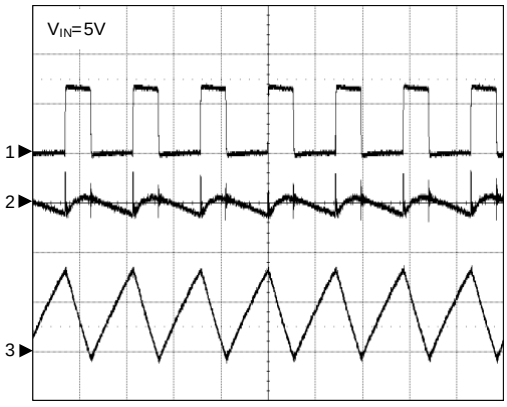
CH1: V_{EN}, 2V/Div, DC
CH2: V_{LX}, 10V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{IN}, 0.1A/Div, DC
TIME: 5ms/Div

Start-up at PWM Condition



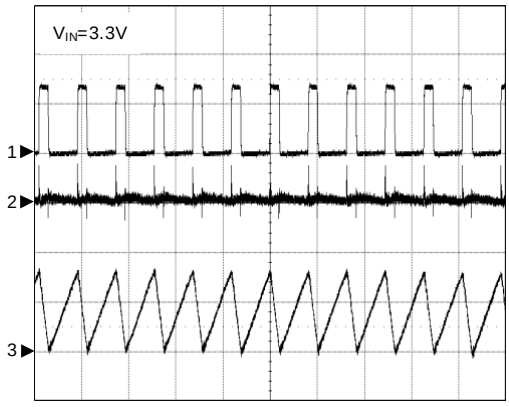
CH1: V_{EN}, 2V/Div, DC
CH2: V_{LX}, 10V/Div, DC
CH3: V_{OUT}, 5V/Div, DC
CH4: I_{IN}, 0.2A/Div, DC
TIME: 5ms/Div

Normal Operation at 600kHz



CH1: V_{LX}, 10V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: I_L, 1A/Div, DC
TIME: 1 μs/Div

Normal Operation at 1.2MHz

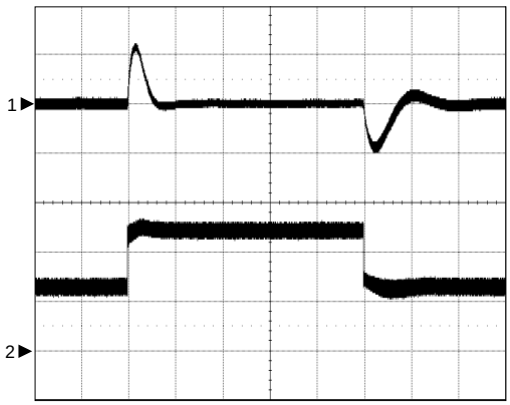


CH1: V_{LX}, 10V/Div, DC
CH2: V_{OUT}, 50mV/Div, AC
CH3: I_L, 0.5A/Div, DC
TIME: 1 μs/Div

Operating Waveforms (Cont.)

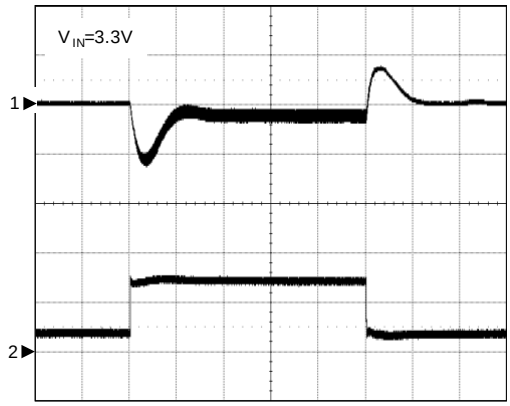
(Refer to the section “Typical Application Circuits”, V_{IN}=3.3V, T_A=25°C, unless otherwise specified)

Line Transient Response



CH1: V_{OUT}, 500mV/Div, AC
CH2: V_{IN}, 2V/Div, DC
TIME: 200 μs/Div

Load Transient Response

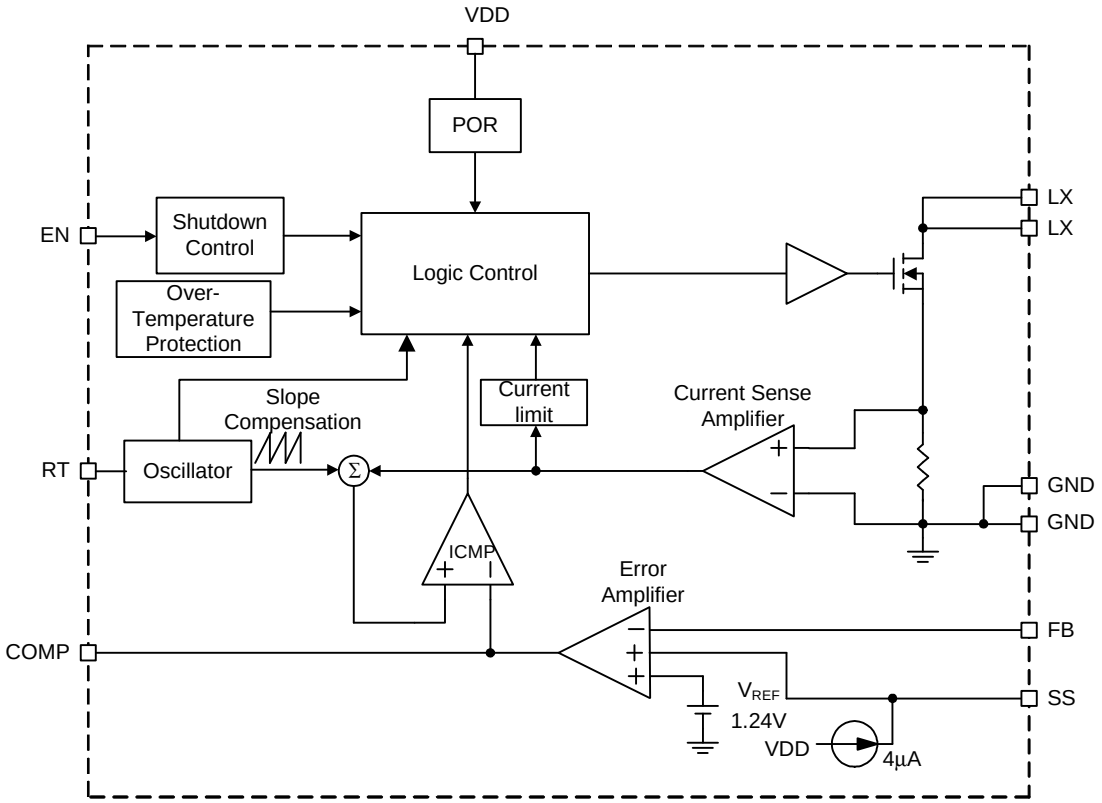


CH1: V_{OUT}, 500mV/Div, AC
CH2: I_{OUT}, 500mA/Div, DC
TIME: 100 μs/Div

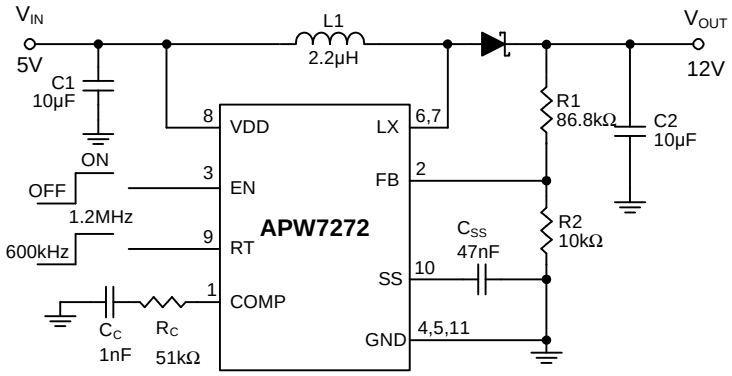
Pin Description

PIN.		FUNCTION
NO	NAME	
1	COMP	Error Amplifier Output. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
2	FB	Converter Feedback Input.
3	EN	Device Enable Control Input. Force V_{EN} exceed 1.8V enable the device. Left V_{EN} below 0.8V to shutdown.
4,5	GND	Signal and Power Ground. Connect this pin to exposed pad.
6,7	LX	Converter Switch Pin. Connect inductor and diode here.
8	VDD	Device Input Supply Voltage.
9	RT	Operation Frequency Setting. Force V_{RT} exceeds 1.8V set the oscillator operates at 1.2MHz. Pull V_{RT} below 0.8V at 600kHz.
10	SS	Soft Start Output. Connect a capacitor to GND to set the soft start interval.
Exposed Pad (11)	GND	Signal Ground. Tie this pin to the GND.

Block Diagram



Typical Application Circuits



V_{IN}(V)	V_{OUT}(V)	L1(H)	V_{OSC}(Hz)	R_C(W)	C_C(F)
5	12	4.7μ	1.2M	100k	1n
5	12	4.7μ	1.2M	51k	1n
5	12	4.7μ	600k	100k	1n
5	12	2.2μ	1.2M	180k	680p
5	12	2.2μ	600k	180k	680p
3.3	12	4.7μ	1.2M	180k	680p
3.3	12	4.7μ	600k	180k	680p
3.3	12	2.2μ	1.2M	180k	680p
3.3	12	2.2μ	600k	180k	680p
3.3	13.6	3.6μ	1.2M	56k	330p
3.3	5	1.5μ	1.2M	60k	220p
3.3	5	2.2μ	600k	40k	680p

Table 1. Recommended Components

Function Description

Main Control Loop

The APW7272 is a constant frequency and current-mode switching regulator. In normal operation, the internal N-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch, and then turned off when an internal comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP node which is the output of the error amplifier (EAMP). An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slightly to decrease in V_{FB} associated with the 1.24V reference, which in turn, it causes the COMP voltage to increase until the average inductor current matches the new load current.

VIN Under-Voltage Lockout (UVLO)

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VDD with the UVLO threshold to ensure the input voltage is high enough for reliable operation. The 200mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the converter.

Soft-Start

The APW7272 provides the programmed soft-start function to limit the inrush current. The soft-start time can be programmed by the external capacitor between SS and GND. Typical charge current is 4uA, and the soft-start time is about 15ms with 47nF capacitor.

Current-Limit Protection

The APW7272 monitors the inductor current, flows through the N-channel MOSFET, and limits the current peak at current-limit level to prevent loads and the APW7272 from damaging during overload or short-circuit conditions.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7272. When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFET allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and regulates the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature (T_J) during continuous thermal overload conditions increasing the lifetime of the device.

Enable/Shutdown

Driving EN to the ground places the APW7272 in shutdown mode. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down, and the quiescent supply current reduces to 10μA maximum.

Frequency Selection

When VRT is above the RT high threshold (1.8V, minimum), the frequency is for 1.2MHz operation. When VRT is below the RT low threshold (0.8V, maximum), the frequency is for 1.2MHz operation. The internal pull low resistance is connected between RT and GND.

Application Information

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the ripple of the input current drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller when an input capacitor with larger capacitance is used. For reliable operation, it is recommended to select the capacitor with maximum voltage rating at least 1.2 times of the maximum input voltage. The capacitors should be placed close to the VIN and the GND.

Inductor Selection

Selecting an inductor with low dc resistance reduces conduction losses and achieves high efficiency. The efficiency is moderated whilst using small chip inductor which operates with higher inductor core losses. Therefore, it is necessary to take further consideration while choosing an adequate inductor. Mainly, the inductor value determines the inductor ripple current: larger inductor value results in smaller inductor ripple current and lower conduction losses of the converter. However, larger inductor value generates slower load transient response. A reasonable design rule is to set the ripple current, ΔI_L, to be 30% to 50% of the maximum average inductor current, $I_{L(AVG)}$. The inductor value can be obtained as below,

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT}-V_{IN}}{F_{SW}\cdot I_{OUT(MAX)}} \times \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

V_{IN} = input voltage

V_{OUT} = output voltage

F_{SW} = switching frequency in MHz

I_{OUT} = maximum output current in amp.

η = Efficiency

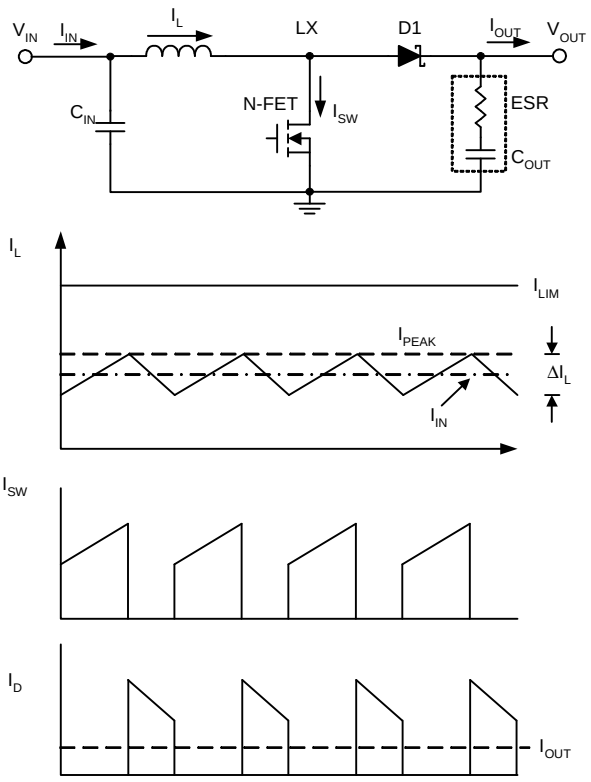
$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)}\cdot V_{OUT}}{V_{IN}\cdot \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2}\cdot\frac{V_{IN}\cdot(V_{OUT}-V_{IN})}{V_{OUT}\cdot L\cdot F_{SW}}$$



Output Capacitor Selection

The current-mode control scheme of the APW7272 allows the usage of tiny ceramic capacitors. The higher capacitor value provides good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{COUT} \approx \frac{I_{OUT}}{C_{OUT}}\cdot\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}\cdot F_{SW}}\right)$$

$$\Delta V_{ESR} \approx I_{PEAK}\cdot R_{ESR}$$

where I_{PEAK} is the peak inductor current.

Application Information (Cont.)

Output Capacitor Selection (Cont.)

For ceramic capacitor application, the output voltage ripple is dominated by the ΔV_{COUT}. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

Output Voltage Setting

The output voltage is set by a resistive divider. The external resistive divider is connected to the output which allows remote voltage sensing as shown in "Typical Application Circuits". A suggestion of the maximum value of R1 is 2MΩ and R2 is 200kΩ for keeping the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R1}{R2}\right) = 1.24\left(1 + \frac{R1}{R2}\right)$$

Diode Selection

To achieve the high efficiency, a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter.

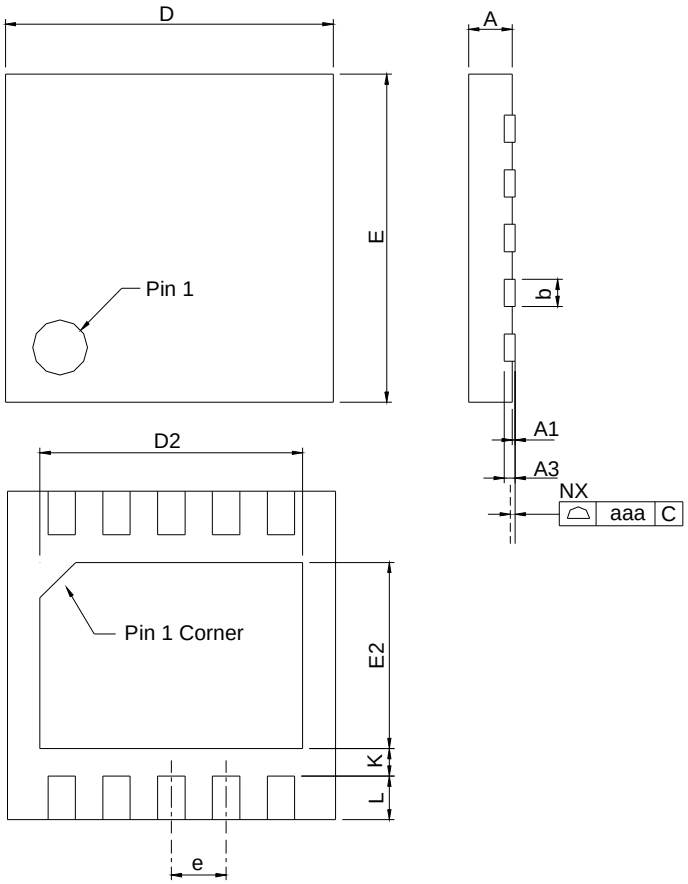
Layout Consideration

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and the GND without any via holes for good input voltage filtering.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. Since the feedback pin and network is a high impedance circuit the feedback network should be routed away from the inductor. The feedback pin and feedback network should be shielded with a ground plane or trace to minimize noise coupling into this circuit.
4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

Package Information

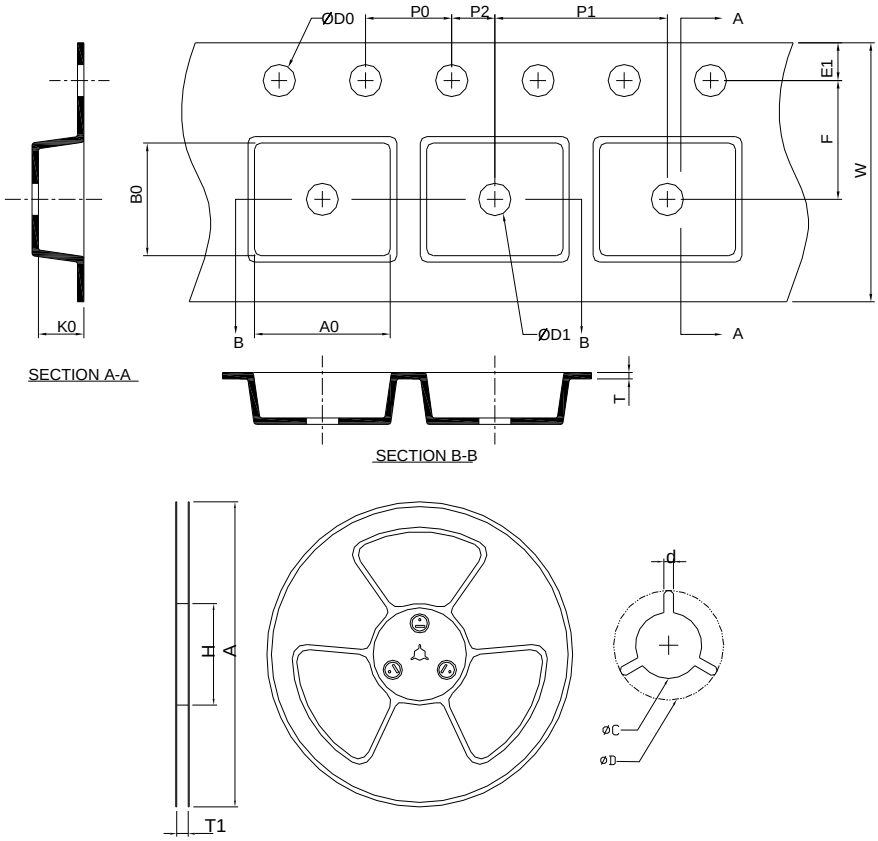
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

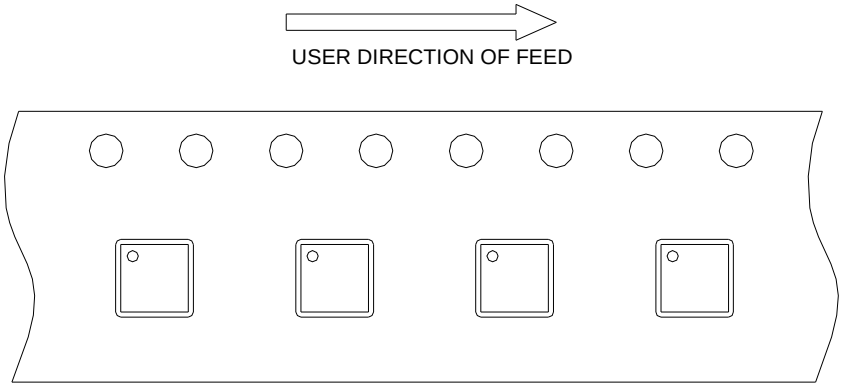
(mm)

Devices Per Unit

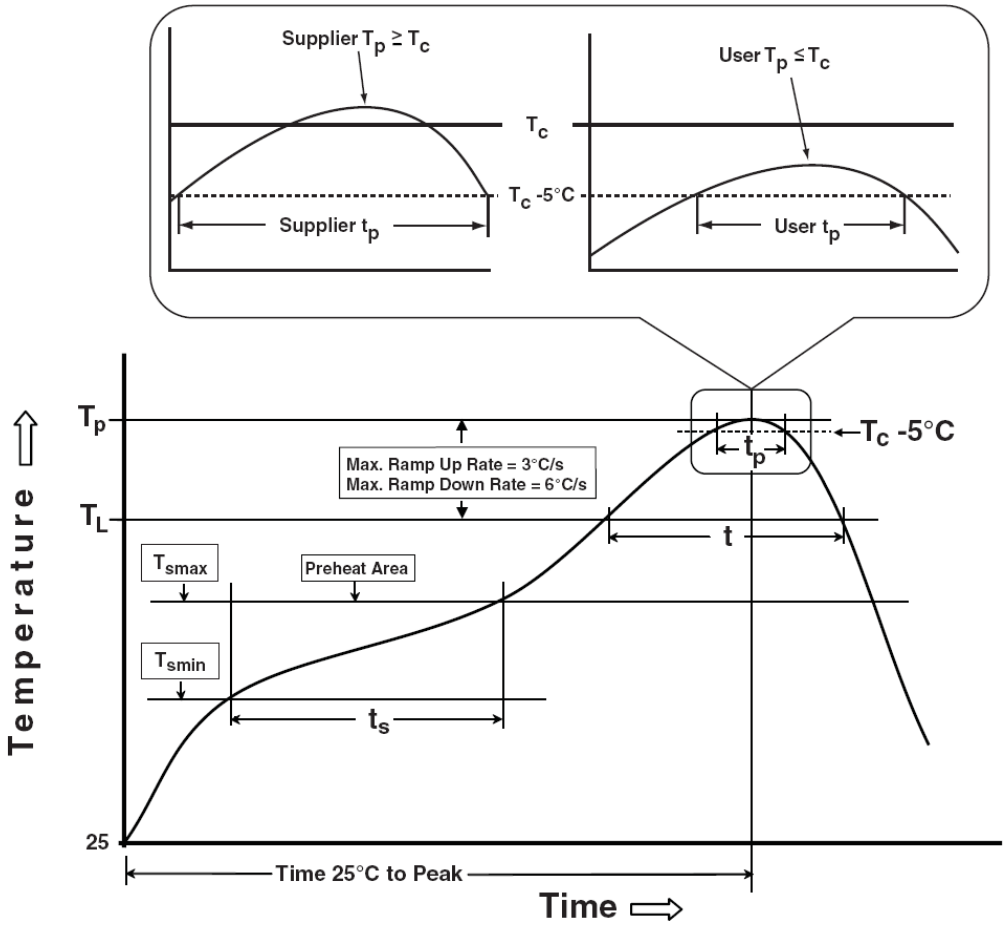
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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