OMAP-L137
Low-Power Applications Processor
Silicon Revision 1.0

Silicon Errata

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OMAP-L137
Silicon Revision 1.0

1 Introduction

This document describes the known exceptions to the functional specifications for the *OMAP-L137 Low-Power Applications Processor*. For more detailed information, see the *OMAP-L137 Low-Power Applications Processor* data manual (literature number SPRS563).

1.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all OMAP processors and support tools. Each commercial OMAP platform member has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

X	Experimental device that is not necessarily representative of the final device's electrical specifications
P	Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
NULL	Fully-qualified production device

Support tool development evolutionary flow:

TMDX	Development-support product that has not yet completed Texas Instruments internal qualification testing
TMDS	Fully-qualified development-support product

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

1.2 Revision Identification

Figure 1 shows an example of the device markings.

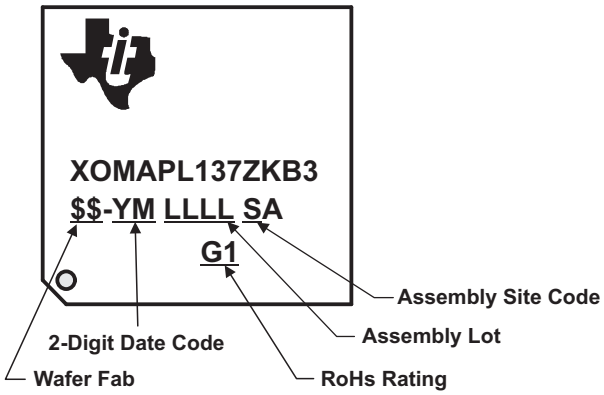

Figure 1. Example, Device Revision Codes for OMAP-L137 (ZKB Package)

NOTES:

A. Non-qualified devices are marked with the letters "X" or "P" at the beginning of the device name.

Each silicon revision uses a specific revision of the CPU and the C674x Megamodule. The CPU revision ID identifies the silicon revision of the CPU. Table 1 lists the CPU and C674x Megamodule revision associated with each silicon revision. The CPU revision can be read from the REVISION_ID field of the CPU Control Status Register (CSR). The C674x Megamodule revision can be read from the REVISION field of the Megamodule Revision ID register (MM_REVID) located at address 0181 2000h.

The ROM code revision can be read from address location 0x1170 0008h. Table 1 shows the ROM code revision for each revision of the device.

Table 1. Silicon Revision Variables

SILICON REVISION	CPU REVISION	C674x MEGAMODULE REVISION	ROM CODE REVISION
1.0	1.0 CPU ID + CPU REV ID (CSR.[31:16] = 1400h)	Revision 1 (MM_REVID.[15:0] = 0000h)	D800K001 (ASCII format)

2 Silicon Revision 1.0 Usage Notes and Known Design Exceptions to Functional Specifications

This section describes the usage notes and advisories that apply to silicon revision 1.0 of the *OMAP-L137* device.

2.1 Usage Notes for Silicon Revision 1.0

There are currently no known usage notes for silicon revision 1.0.

2.2 Silicon Revision 1.0 Known Design Exceptions to Functional Specifications

Table 2.3. Silicon Revision 1.0 Advisory List

Title	Page
Advisory 1.0.1 ARM Data Cache in Write-Back Mode is Not Functional: Must Use Write-Through or Non-Cached Mode	5

Advisory 1.0.1 *ARM Data Cache in Write-Back Mode is Not Functional: Must Use Write-Through or Non-Cached Mode*

Revision(s) Affected 1.0

Details The ARM926 subsystem allows data memory regions to be write-back cachable, write-through cachable, or non-cached. On this device revision, the *Write-Back* mode is not functional; therefore, *Write-Through* or *Non-Cached* mode must always be used.

Workaround(s) Only the *Write-Through* or *Non-Cached* mode can be used. *Write-Through* mode is preferred for better performance. The cache operation is controlled using the C and B bits in page or section descriptors. For operation in *Write-Through* mode, the C and B bits (bits 3:2 in the descriptor) must be set to a value of 10b.

The following is example code using a section descriptor to create a table entry for the first 1MB of external SDRAM on EMIFB as write-through cachable:

```
LDR  r1,  SDRAM0_ADDR            ; table offset for SDRAM0 region
LDR  r2,  SDRAM0_DATA            ; descriptor pattern for SDRAM0 region
STR  r2,  [r0, r1, LSL#2]        ; store the table entry at TTB base + table
offset * 4
SDRAM0_ADDR        .word    0x00000C00
SDRAM0_DATA        .word    0xC0000CFA
```

For more information on ARM data cache modes and how to configure them, refer to the *ARM926EJ-S™ Technical Reference Manual* available at www.arm.com/documentation. Chapter 4 of the *ARM926EJ-S™ Technical Reference Manual* provides details about cache operations on the ARM926EJ-S processor.

Section descriptor: A section descriptor provides the base address of a 1MB block of memory. Figure 2 shows the format of a section descriptor.

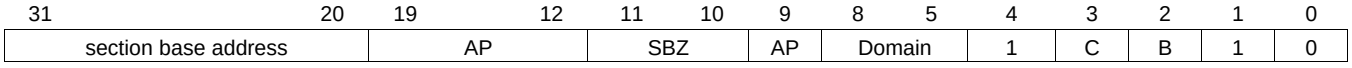

Figure 2. Section Descriptor

Table 2 shows the Section Descriptor bit assignments. Table 3 shows the Page Table C and B bit settings for the DCache.

Table 2. Section Descriptor Bits

BITS	DESCRIPTION
31:20	Form the corresponding bits of the physical address for a section.
19:12	Always written as 0.
11:10	Specify the access permissions for this section.
9	Always written as 0.
8:5	Specify one of the 16 possible domains, held in the domain access control register, that contain the primary access controls.
4	Should be written as 1, for backwards compatibility.
3:2	Indicate if the area of memory mapped by this section is treated as write-back cacheable, write-through cacheable, noncached buffered, or noncached nonbuffered.
1:0	These bits must be 10 to indicate a section descriptor

Table 3. Page Table C and B Bit Settings for the DCache

C BIT	B BIT	DESCRIPTION	ARM926EJ-S BEHAVIOR
0	0	Noncacheable, nonbufferable	DCache disabled. Read from external memory. Write as a nonbuffered store(s) to external memory. DCache is not updated.
0	1	Noncacheable, bufferable	DCache disabled. Read from external memory. Write as a buffered store(s) to external memory. DCache is not updated.
1	0	Write-through	DCache enabled: • Read hit - Read from DCache • Read miss - Linefill • Write hit - Write to the DCache, and buffered store to external memory • Write miss - Buffered store to external memory
1	1	Write-back	DCache enabled: • Read hit - Read from DCache • Read miss - Linefill • Write hit - Write to the DCache only • Write miss - Buffered store to external memory

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265