10 MHz, Four-Quadrant Multiplier/Divider

AD734

FEATURES

High accuracy
- **0.1% typical error**

High speed
- **10 MHz full power bandwidth**
- **450 V/µs slew rate**
- **200 ns settling to 0.1% at full power**

Low distortion
- **−80 dBc from any input**
- **Third-order IMD typically −75 dBc at 10 MHz**

Low noise
- **94 dB SNR, 10 Hz to 20 kHz**
- **70 dB SNR, 10 Hz to 10 MHz**

Direct division mode
- **2 MHz BW at gain of 100**

APPLICATIONS

High performance replacement for AD534
Multiply, divide, square, square root
Modulators, demodulators
Wideband gain control, rms-to-dc conversion
Voltage-controlled amplifiers, oscillators, and filters
Demodulator with 40 MHz input bandwidth

FUNCTIONAL BLOCK DIAGRAM

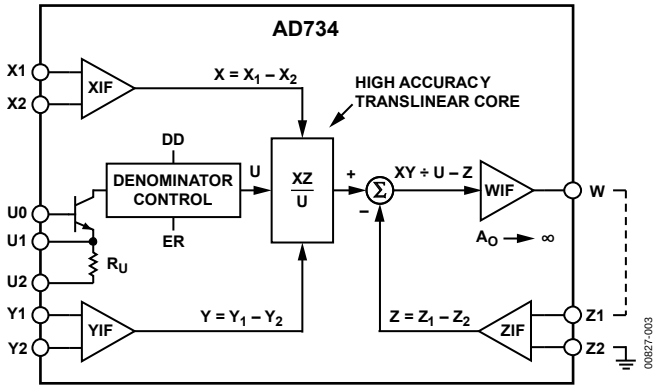

Figure 1.

GENERAL DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low impedance voltage output with a full power (20 V p-p) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of full scale. Distortion is typically less than −80 dBc and guaranteed. The low capacitance X, Y, and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage, U, is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB, and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process, and a novel approach to laser trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of −40°C to +85°C and come in a 14-lead CERDIP and a 14-lead PDIP package. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of −55°C to +125°C, is available in a 14-lead CERDIP.

Rev. E
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REVISION HISTORY

2/11—Rev. D to Rev. E

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Changes to Figure 22 and Figure 23 ... 12
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1/11—Rev. C to Rev. D

Updated Format ... Universal
Changes to Figure 1 and General Description Section ... 1
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SPECIFICATIONS

T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2$ kΩ, unless otherwise noted.

Generalized transfer function: $W = A_O\left\{\frac{(X_1 - X_2)(Y_1 - Y_2)}{U_1 - U_2} - (Z_1 - Z_2)\right\}$

Table 1.

		A			B			S		
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X, Y ≤ 10 V		0.1	0.4		0.1	0.25		0.1	0.4	%
Over T_{MIN} to T_{MAX}				1			0.6			1.25	%
vs. Temperature	T_{MIN} to T_{MAX}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	0.05		0.01	0.05		0.01	0.05	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			−58			−66			−58	dBc
	T_{MIN} to T_{MAX}			−55			−63			−55	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			−60			−80			−60	dBc
	T_{MIN} to T_{MAX}			−57			−74			−57	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	−60		−85	−70		−85	−60	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	−66		−85	−76		−85	−66	dBc
Noise (RTO)	X = Y = 0 V										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		µV/√Hz
Total Output Noise	10 Hz to 20 kHz		−94	−88		−94	−88		−94	−88	dBc
	T_{MIN} to T_{MAX}			−85			−85			−85	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1		1			1			%
X Input Clipping Level	Y ≤ 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				0.3			0.15			0.3	%
	T_{MIN} to T_{MAX}			0.8			0.65			1	%
Output to 1%	U = 1 V to 10 V step, X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, AND Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or common mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				15			5			15	mV
	T_{MIN} to T_{MAX}			25			15			25	mV
Y Input Offset Voltage				10			5			10	mV
	T_{MIN} to T_{MAX}			12			6			12	mV
Z Input Offset Voltage				20			10			20	mV
	T_{MIN} to T_{MAX}			50			50			90	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	54	70		66	70		54	70		dB
	T_{MIN} to T_{MAX}	50			56			50			dB

Parameter	Conditions	A			B			S			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CMRR	f = 5 kHz	70	85		70	85		70	85		dB
Input Bias Current (X, Y, Z Inputs)			50	300		50	150		50	300	nA
	T_{MIN} to T_{MAX}			400			300			500	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, AND U2)											
Operating Range			VN to VP − 3			VN to VP − 3			VN to VP − 3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{MIN} to T_{MAX}	±12			±12			±12			V
Open-Loop Voltage Gain	X = Y = 0, input to Z		72			72			72		dB
Dynamic Response	From X or Y input, $C_{LOAD} \leq 20$ pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/µs
Settling Time	+20 V or −20 V output step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{MIN} to T_{MAX}	20	50	80	20	50	80	20	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{MIN} to T_{MAX}	6	9	12	6	9	12	6	9	12	mA

[1] Figures given are percent of full scale (for example, 0.01% = 1 mV).
[2] dBc refers to decibels relative to the full-scale input (carrier) level of 7 V rms.
[3] See Figure 28 for test circuit.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V
Internal Power Dissipation	
for T_J max = 175°C	500 mW
X, Y, and Z Input Voltages	VN to VP
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
Q-14	−65°C to +150°C
N-14	−65°C to +150°C
Operating Temperature Range	
AD734A, AD734B (Industrial)	−40°C to +85°C
AD734S (Military)	−55°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	+300°C
Transistor Count	81
ESD Rating	500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
14-Lead PDIP (N-14)	150	°C/W
14-Lead CERDIP (Q-14)	110	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

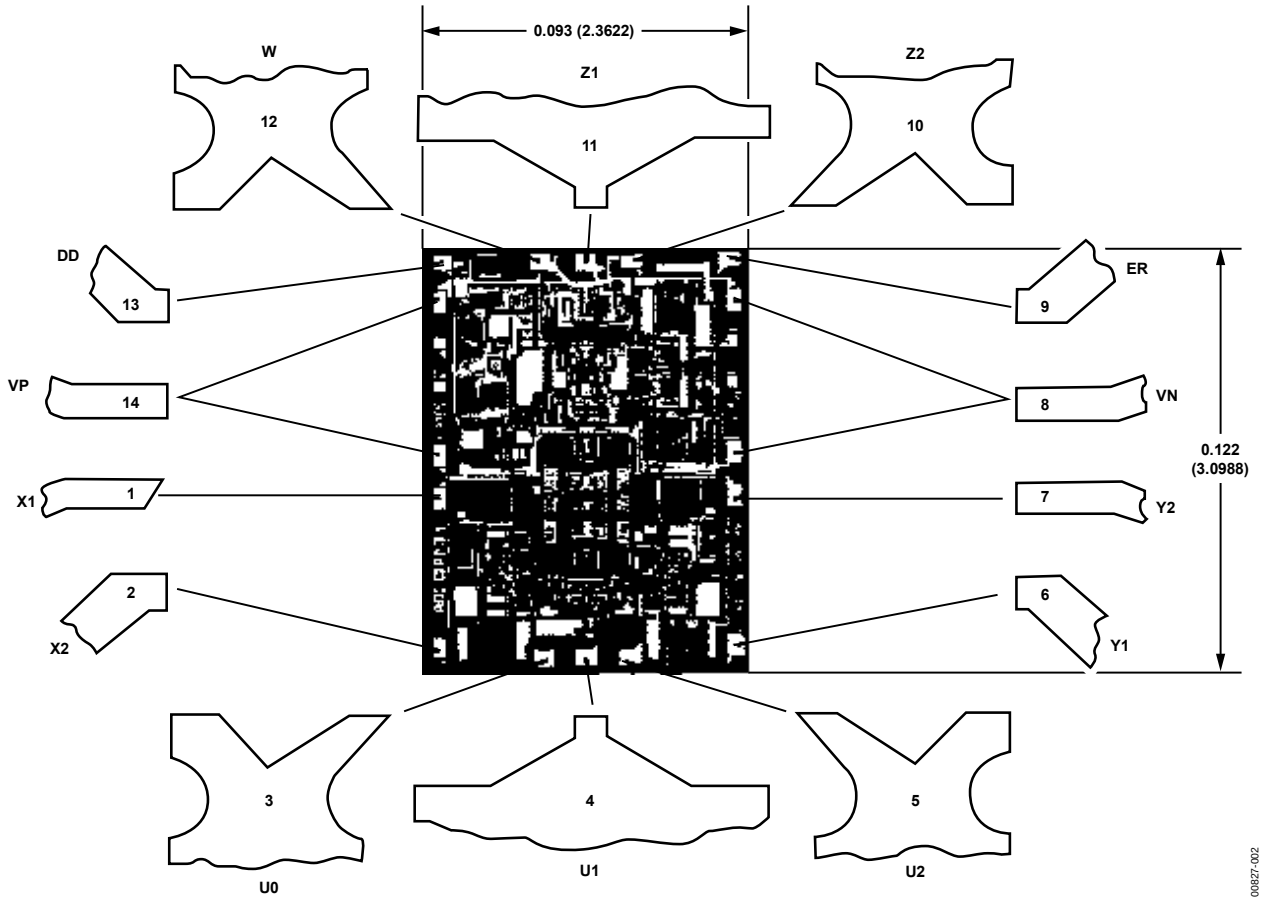


Figure 2. Chip Dimensions and Bonding Diagram, Dimensions shown in inches and (mm), (Contact factory for latest dimensions)

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

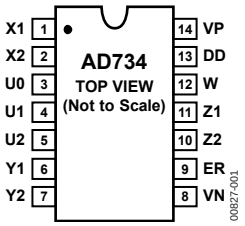


Figure 3. 14-Lead PDIP and 14-Lead CERDIP

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	X1	X Differential Multiplicand Input.
2	X2	X Differential Multiplicand Input.
3	U0	Denominator Current Source Enable Interface.
4	U1	Denominator Interface—see the Functional Description section.
5	U2	Denominator Interface—see the Functional Description section.
6	Y1	Y Differential Multiplicand Input.
7	Y2	Y Differential Multiplicand Input.
8	VN	Negative Supply.
9	ER	Reference Voltage.
10	Z2	Z Differential Summing Input.
11	Z1	Z Differential Summing Input.
12	W	Output.
13	DD	Denominator Disable.
14	VP	Positive Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

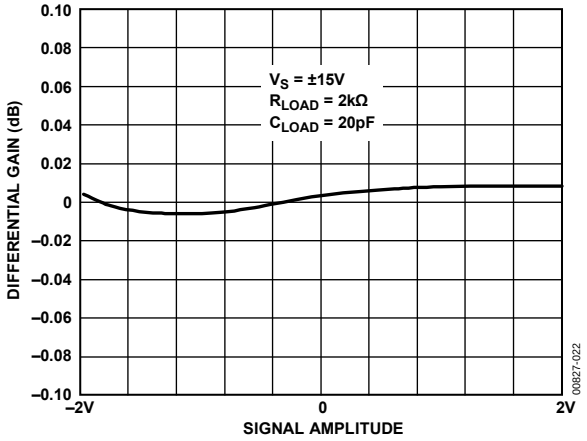


Figure 4. Differential Gain at 3.58 MHz and R_{LOAD} = 2 kΩ

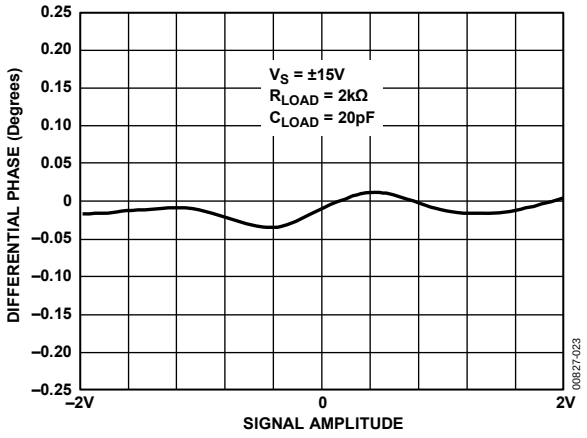


Figure 5. Differential Phase at 3.58 MHz and R_{LOAD} = 2 kΩ

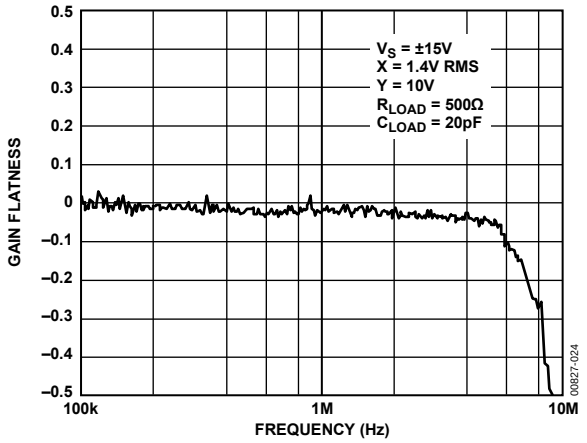


Figure 6. Gain Flatness, 300 kHz to 10 MHz, R_{LOAD} = 500 Ω

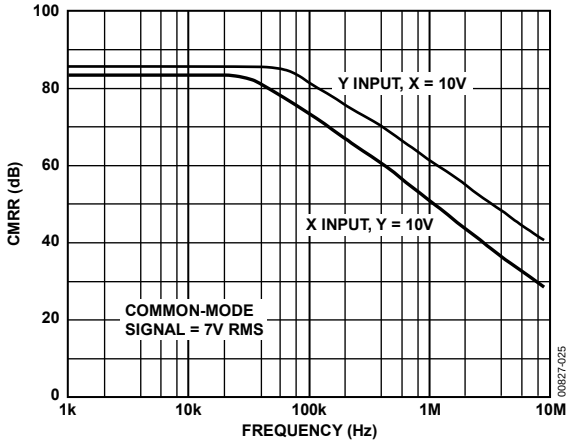


Figure 7. CMRR vs. Frequency

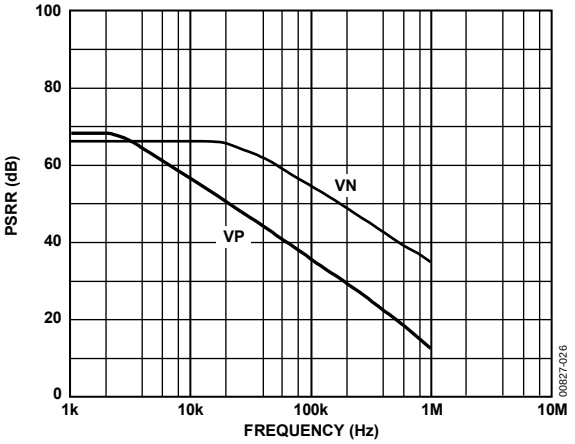


Figure 8. PSRR vs. Frequency

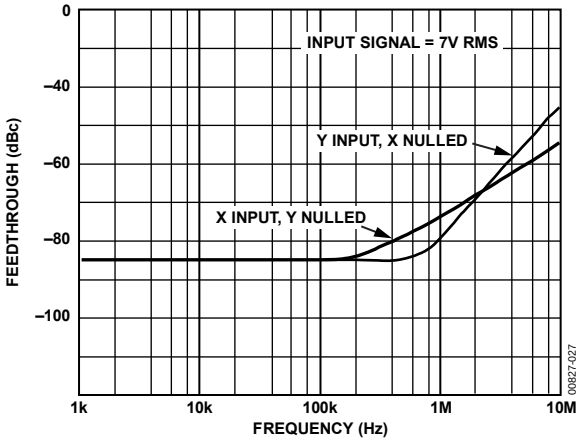


Figure 9. Feedthrough vs. Frequency

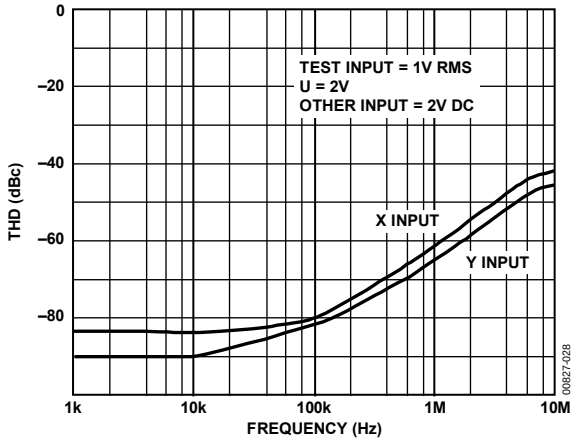


Figure 10. THD vs. Frequency, U = 2 V

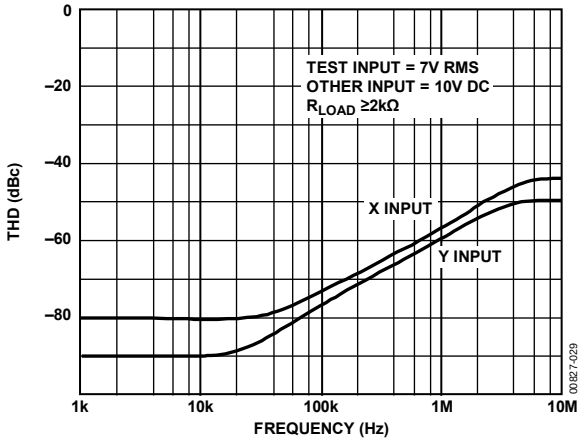


Figure 11. THD vs. Frequency, U = 10 V

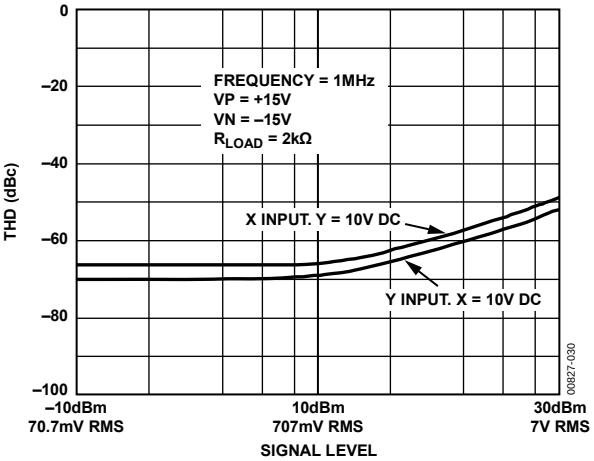


Figure 12. THD vs. Signal Level, f = 1 MHz

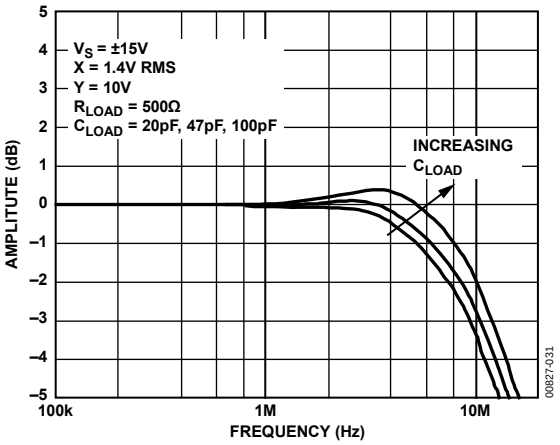


Figure 13. Gain vs. Frequency vs. C_{LOAD}

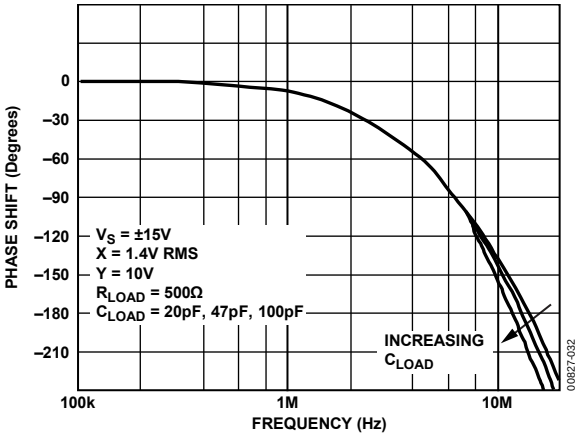


Figure 14. Phase vs. Frequency vs. C_{LOAD}

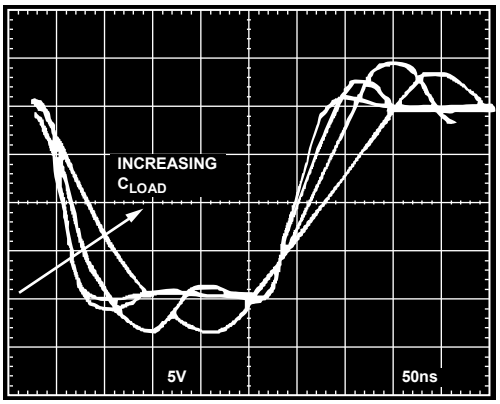


Figure 15. Pulse Response vs. C_{LOAD}, C_{LOAD} = 0 pF, 47 pF, 100 pF, 200 pF

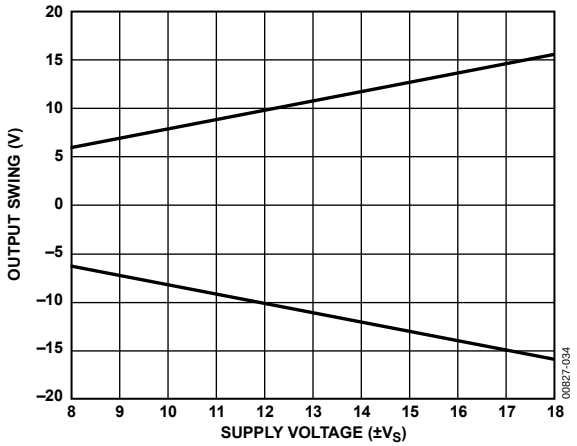


Figure 16. Output Swing vs. Supply Voltage

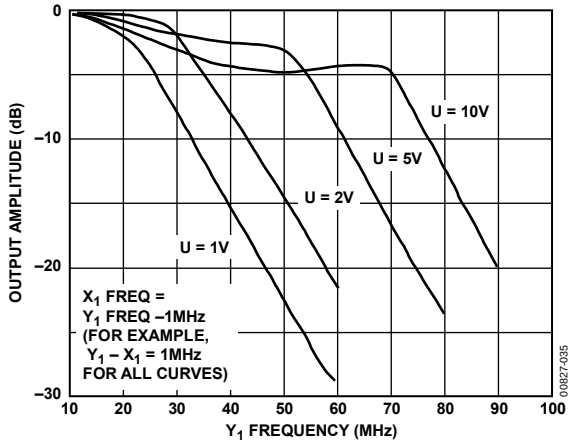


Figure 17. Output Amplitude vs. Input Frequency, When Used as Demodulator

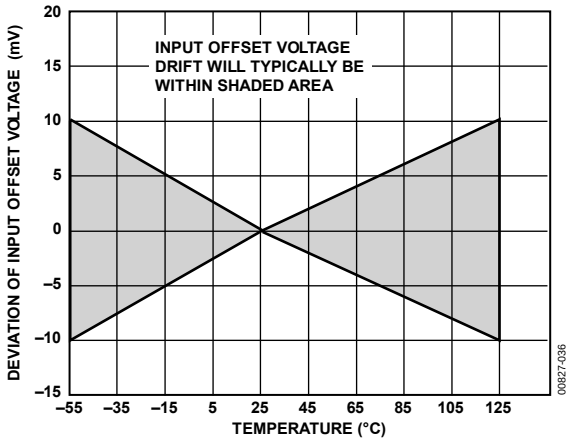


Figure 18. V_{OS} Drift, X Input

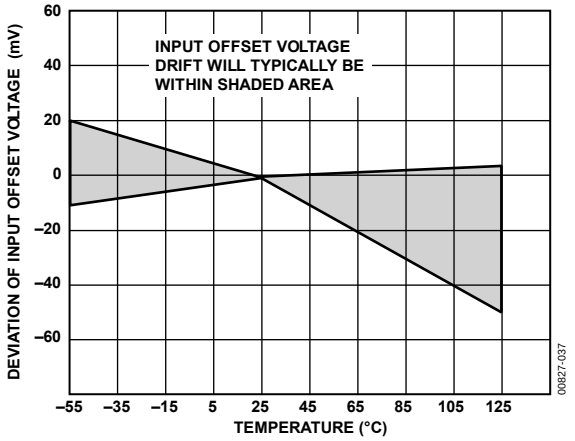


Figure 19. V_{OS} Drift, Z Input

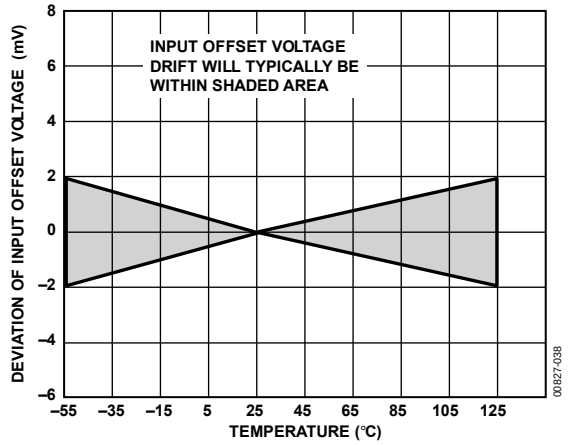


Figure 20. V_{OS} Drift, Y Input

FUNCTIONAL DESCRIPTION

The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers to provide:

- A new output amplifier design with more than 20 times the slew rate of the AD534 (450 V/µs vs. 20 V/µs) for a full power (20 V p-p) bandwidth of 10 MHz.
- Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
- Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
- Very clean transient response, achieved through the use of a novel input stage design and wideband output amplifier, which also ensure that distortion remains low even at high frequencies.
- Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.

Figure 3 shows the lead configuration of the 14-lead PDIP and CERDIP packages.

Figure 1 is a simplified block diagram of the AD734. Operation is similar to that of the industry-standard AD534, and in many applications, these parts are pin compatible. The main functional difference is the provision for direct control of the denominator voltage, U, explained fully in the Direct Denominator Control section. Internal signals are in the form of currents, but the function of the AD734 can be understood using voltages throughout, as shown in Figure 1.

The AD734 differential X, Y, and Z inputs are handled by wideband interfaces that have low offset, low bias current, and low distortion. The AD734 responds to the difference signals $X = X_1 - X_2$, $Y = Y_1 - Y_2$, and $Z = Z_1 - Z_2$, and rejects common-mode voltages on these inputs. The X, Y, and Z interfaces provide a nominal full-scale (FS) voltage of ±10 V, but, due to the special design of the input stages, the linear range of the differential input can be as large as ±17 V. Also, unlike previous designs, the response on these inputs is not clipped abruptly above ±15 V, but drops to a slope of one half.

The bipolar input signals X and Y are multiplied in a translinear core of novel design to generate the product XY/U. The denominator voltage, U, is internally set to an accurate, temperature-stable value of 10 V, derived from a buried-Zener reference. An uncalibrated fraction of the denominator voltage U appears between the voltage reference pin (ER) and the negative supply pin (VN), for use in certain applications where a temperature-compensated voltage reference is desirable. The internal denominator, U, can be disabled, by connecting the denominator disable Pin 13 (DD) to the positive supply pin (VP); the denominator can then be replaced by a fixed or variable external voltage ranging from 10 mV to more than 10 V.

The high gain output op amp nulls the difference between XY/U and an additional signal, Z, to generate the final output, W. The actual transfer function can take on several forms, depending on the connections used. The AD734 can perform all of the functions supported by the AD534, and new functions using the direct-division mode provided by the U interface.

Each input pair (X1 and X2, Y1 and Y2, Z1 and Z2) has a differential input resistance of 50 kΩ; this is formed by actual resistors (not a small-signal approximation) and is subject to a tolerance of ±20%. The common-mode input resistance is several megohms and the parasitic capacitance is about 2 pF.

The bias currents associated with these inputs are nulled by laser-trimming, such that when one input of a pair is optionally ac-coupled and the other is grounded, the residual offset voltage is typically less than 5 mV, which corresponds to a bias current of only 100 nA. This low bias current ensures that mismatches in the sources' resistances at a pair of inputs does not cause an offset error. These currents remain low over the full temperature range and supply voltages.

The common-mode range of the X, Y, and Z inputs does not fully extend to the supply rails. Nevertheless, it is often possible to operate the AD734 with one terminal of an input pair connected to either the positive or negative supply, unlike previous multipliers. The common-mode resistance is several megohms.

The full-scale output of ±10 V can be delivered to a load resistance of 1 kΩ (although the specifications apply to the standard multiplier load condition of 2 kΩ). The output amplifier is stable, driving capacitive loads of at least 100 pF, when a slight increase in bandwidth results from the peaking caused by this capacitance. The 450 V/µs slew rate of the AD734 output amplifier ensures that the bandwidth of 10 MHz can be maintained up to the full output of 20 V p-p. Operation at reduced supply voltages is possible, down to ±8 V, with reduced signal levels.

AVAILABLE TRANSFER FUNCTIONS

The uncommitted (open-loop) transfer function of the AD734 is

$$W = A_O\left\{\frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2)\right\} \quad (1)$$

where A_O is the open-loop gain of the output op amp, typically 72 dB. When a negative feedback path is provided, the circuit forces the quantity inside the brackets essentially to zero, resulting in the equation

$$(X_1 - X_2)(Y_1 - Y_2) = U\,(Z_1 - Z_2) \quad (2)$$

This is the most useful generalized transfer function for the AD734; it expresses a balance between the product XY and the product UZ. The absence of the output, W, in this equation only reflects the fact that the input to be connected to the op amp output is not specified.

Most of the functions of the AD734 (including division, unlike the AD534 in this respect) are realized with Z1 connected to W. Therefore, substituting W in place of Z_1 in Equation 2 results in an output.

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z_2 \quad (3)$$

The free input, Z2, can be used to sum another signal to the output; in the absence of a product signal, W simply follows the voltage at Z2 with the full 10 MHz bandwidth. When not needed for summation, Z2 should be connected to the ground associated with the load circuit. The allowable polarities can be shown in the following shorthand form:

$$(\pm W) = \frac{(\pm X)(\pm Y)}{(+U)} + \pm Z \quad (4)$$

In the recommended direct divider mode, the Y input is set to a fixed voltage (typically 10 V) and U is varied directly; it can have any value from 10 mV to 10 V. The magnitude of the ratio X/U cannot exceed 1.25; for example, the peak X input for U = 1 V is ±1.25 V. Above this level, clipping occurs at the positive and negative extremities of the X input. Alternatively, the AD734 can be operated using the standard (AD534) divider connections (see Figure 27), when the negative feedback path is established via the Y2 input. Substituting W for Y_2 in Equation 2,

$$W = U\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1 \quad (5)$$

In this case, note that the variable X is now the denominator, and the previous restriction (X/U ≤ 1.25) on the magnitude of the X input does not apply. However, X must be positive for the feedback polarity to be correct. Y_1 can be used for summing purposes or connected to the load ground if not needed. The shorthand form in this case is

$$(\pm W) = (+U)\frac{(\pm Z)}{(+X)} + (\pm Y) \quad (6)$$

In some cases, feedback can be connected to two of the available inputs. This is true for the square-rooting connections (see Figure 28), where W is connected to both X1 and Y2. Set X_1 = W and Y_2 = W in Equation 2, and anticipating the possibility of again providing a summing input, set X_2 = S and Y_1 = S, so that, in shorthand form,

$$(\pm W) = \sqrt{(+U)(+Z)} + (\pm S) \quad (7)$$

This is seen more generally to be the geometric-mean function, because both U and Z can be variable; operation is restricted to one quadrant. Feedback can also be taken to the U interface. Full details of the operation in these modes is provided in the Wideband RMS-to-DC Converter Using U Interface section.

DIRECT DENOMINATOR CONTROL

A valuable new feature of the AD734 is the provision to replace the internal denominator voltage, U, with any value from 10 mV to 10 V. This can be used

- To simply alter the multiplier scaling, thus improve accuracy and achieve reduced noise levels when operating with small input signals.
- To implement an accurate two-quadrant divider, with a 1000:1 gain range and an asymptotic gain-bandwidth product of 200 MHz.
- To achieve certain other special functions, such as AGC or rms.

Figure 21 shows the internal circuitry associated with denominator control. Note, first, that the denominator is actually proportional to a current, Iu, having a nominal value of 356 μA for U = 10 V, whereas the primary reference is a voltage, generated by a buried-Zener circuit and laser-trimmed to have a very low temperature coefficient. This voltage is nominally 8 V with a tolerance of ±10%.

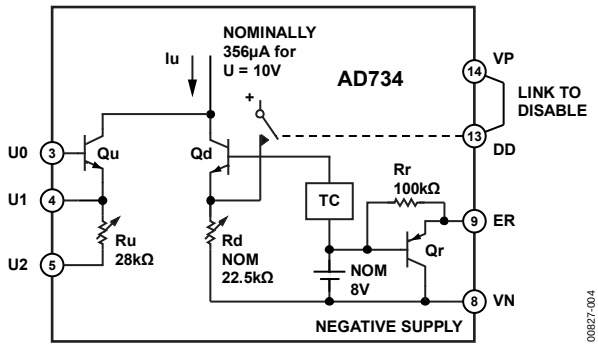


Figure 21. Denominator Control Circuitry

After temperature-correction (block TC), the reference voltage is applied to Transistor Qd and trimmed Resistor Rd, which generate the required reference current. Transistor Qu and Resistor Ru are not involved in setting up the internal denominator, and their associated control pins, U0, U1, and U2, are normally grounded. The reference voltage is also made available, via the 100 kΩ resistor, Rr, at Pin 9 (ER).

When the control pin, DD (denominator disable), is connected to VP, the internal source of Iu is shut off, and the collector current of Qu must provide the denominator current. The resistor Ru is laser-trimmed such that the multiplier denominator is exactly equal to the voltage across it (that is, across Pin U1 and Pin U2). Note that this trimming only sets up the correct internal ratio; the absolute value of Ru (nominally 28 kΩ) has a tolerance of ±20%. Also, the alpha of Qu (typically 0.995), which may be seen as a source of scaling error, is canceled by the alpha of other transistors in the complete circuit.

In the simplest scheme (see Figure 22), an externally provided control voltage, V_G, is applied directly to U0 and U2 and the resulting voltage across Ru is therefore reduced by one V_{BE}. For example, when V_G = 2 V, the actual value of U is about 1.3 V.

This error is not important in some closed-loop applications, such as automatic gain control (AGC), but clearly is not acceptable where the denominator value must be well-defined. When it is required to set up an accurate, fixed value of U, the on-chip reference can be used. The transistor Qr is provided to cancel the V_{BE} of Qu, and is biased by an external resistor, R2, as shown in Figure 23. R1 is chosen to set the desired value of U and consists of a fixed and adjustable resistor.

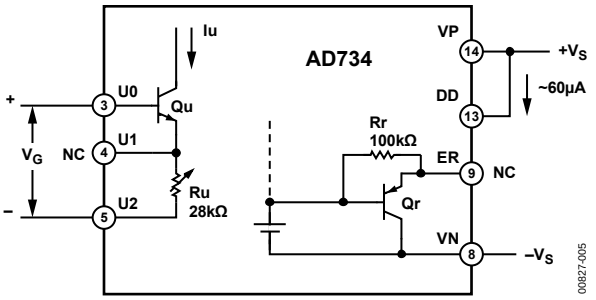


Figure 22. Low Accuracy Denominator Control

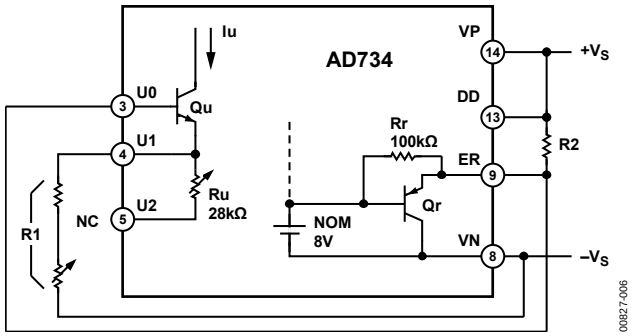


Figure 23. Connections for a Fixed Denominator

Table 5 shows useful values of the external components for setting up nonstandard denominator values.

Table 5. Component Values for Setting Up Nonstandard Denominator Values

Denominator	R1 (Fixed)	R1 (Variable)	R2
5 V	34.8 kΩ	20 kΩ	120 kΩ
3 V	64.9 kΩ	20 kΩ	220 kΩ
2 V	86.6 kΩ	50 kΩ	300 kΩ
1 V	174 kΩ	100 kΩ	620 kΩ

The denominator can also be current controlled, by grounding Pin 3 (U0) and withdrawing a current of Iu from Pin 4 (U1). The nominal scaling relationship is U = 28 × Iu, where u is expressed in volts and Iu is expressed in milliamps. Note, however, that while the linearity of this relationship is very good, it is subject to a scale tolerance of ±20%. Note that the common-mode range on Pin 3 through Pin 5 actually extends from 4 V to 36 V below VP; therefore, it is not necessary to restrict the connection of U0 to ground to use some other voltage.

The output ER can also be buffered, rescaled, and used as a general-purpose reference voltage. It is generated with respect to the negative supply line, Pin 8 (VN), but this is acceptable when driving one of the signal interfaces. An example is shown in Figure 31, where a fixed numerator of 10 V is generated for a divider application. Y2 is tied to VN, but Y1 is 10 V above this; therefore, the common-mode voltage at this interface is still 5 V above VN, which satisfies the internal biasing requirements (see Table 1).

OPERATION AS A MULTIPLIER

All of the connection schemes used in this section are essentially identical to those used for the AD534, with which the AD734 is pin compatible. The only precaution to be noted in this regard is that in the AD534, Pin 3, Pin 5, Pin 9, and Pin 13 are not internally connected, and Pin 4 has a slightly different purpose. In many cases, an AD734 can be directly substituted for an AD534 with immediate benefits in static accuracy, distortion, feedthrough, and speed. Where Pin 4 was used in an AD534 application to achieve a reduced denominator voltage, this function can now be much more precisely implemented with the AD734 using alternative connections (see the Direct Denominator Control section).

Operation from supplies down to ±8 V is possible. The supply current is essentially independent of voltage. As is true of all high speed circuits, careful power supply decoupling is important in maintaining stability under all conditions of use. The decoupling capacitors should always be connected to the load ground, because the load current circulates in these capacitors at high frequencies. Note the use of the special symbol (a triangle with the letter L inside it) to denote the load ground (see Figure 24).

Standard Multiplier Connections

Figure 24 shows the basic connections for multiplication. The X and Y inputs are shown as optionally having their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs can be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both can be driven.

The AD734 has an input resistance of 50 kΩ ± 20% at the X, Y, and Z interfaces, which allows ac coupling to be achieved with moderately good control of the high-pass (HP) corner frequency; a capacitor of 0.1 µF provides a HP corner frequency of 32 Hz. When a tighter control of this frequency is needed, or when the HP corner is above about 100 kHz, an external resistor should be added across the pair of input nodes.

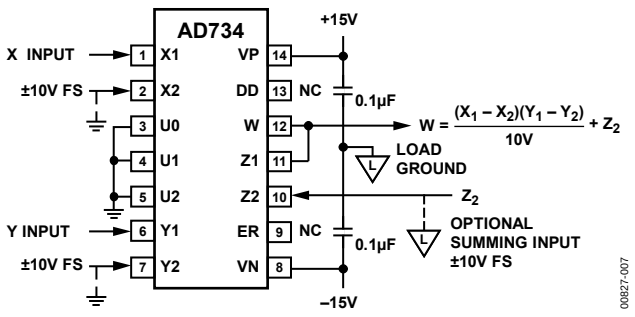


Figure 24. Basic Multiplier Circuit

At least one of the two inputs of any pair must be provided with a dc path (usually to ground). The careful selection of ground returns is important in realizing the full accuracy of the AD734. The Z2 pin is normally connected to the load ground, which can be remote in some cases. It can also be used as an optional summing input (see Equation 3 and Equation 4) having a nominal FS input of ±10 V and the full 10 MHz bandwidth.

In applications where high absolute accuracy is essential, the scaling error caused by the finite resistance of the signal source(s) may be troublesome; for example, a 50 Ω source resistance at just one input introduces a gain error of −0.1%; if both the X and Y inputs are driven from 50 Ω sources, the scaling error in the product is −0.2%. If the source resistances are known, this gain error can be completely compensated by including the appropriate resistance (50 Ω or 100 Ω, respectively, in the preceding cases) between the output, W (Pin 12), and the Z1 feedback input (Pin 11). If Rx is the total source resistance associated with the X1 and X2 inputs, and Ry is the total source resistance associated with the Y1 and Y2 inputs, and neither Rx nor Ry exceeds 1 kΩ, a resistance of Rx + Ry in series with Pin Z1 provides the required gain restoration.

Pin 9 (ER) and Pin 13 (DD) should be left unconnected in this application. The U inputs (Pin 3, Pin 4, and Pin 5) are shown connected to ground; they can alternatively be connected to VN, if desired. In applications where Pin 2 (X2) happens to be driven with a high amplitude, high frequency signal, the capacitive coupling to the denominator control circuitry via an ungrounded Pin 3 can cause high frequency distortion. However, the AD734 can be operated without modification in an AD534 socket and these three pins left unconnected with the preceding caution noted.

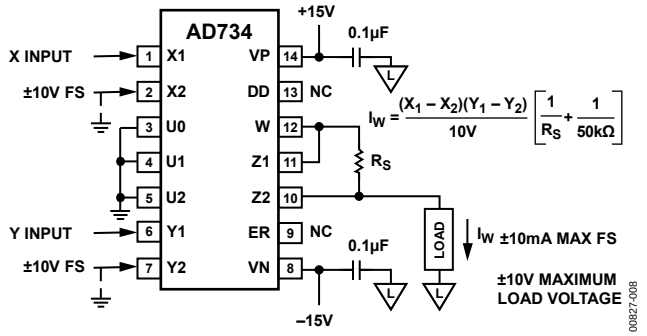


Figure 25. Conversion of Output to a Current

Current Output

It may occasionally be desirable to convert the output voltage to a current. In correlation applications, for example, multiplication is followed by integration; if the output is in the form of a current, a simple grounded capacitor can perform this function. Figure 25 shows how this can be achieved. The op amp forces the voltage across Z1 and Z2, and thus across the resistor, RS, to be the product XY/U. Note that the input resistance of the Z interface is in shunt with RS, which must be calculated accordingly.

The smallest FS current is simply ±10 V/50 kΩ, or ±200 µA, with a tolerance of about 20%. To guarantee a 1% conversion tolerance without adjustment, R_S must be less than 2.5 kΩ. The maximum full-scale output current should be limited to about ±10 mA (thus, R_S = 1 kΩ). This concept can be applied to all connection modes, with the appropriate choice of terminals.

Squaring and Frequency-Doubling

Squaring of an input signal, E, is achieved by connecting the X and Y inputs in parallel; the phasing can be chosen to produce an output of E^2/U or $-E^2/U$ as desired. The input can have either polarity, but the basic output is either always positive or negative; as for multiplication, the Z2 input can be used to add a further signal to the output.

When the input is a sine wave, a squarer behaves as a frequency doubler, because

$$(Esinwt)^2 = E^2\,(1 - cos2wt)/2 \tag{8}$$

Equation 8 shows a dc term at the output, which varies strongly with the amplitude of the input, E. This dc term can be avoided using the connection shown in Figure 26, where an RC network is used to generate two signals whose product has no dc term. The output is

$$W = 4\left\{\frac{E}{\sqrt{2}}\sin\left(wt + \frac{\pi}{4}\right)\right\}\left\{\frac{E}{\sqrt{2}}\sin\left(wt - \frac{\pi}{4}\right)\right\}\left(\frac{1}{10\text{ V}}\right) \tag{9}$$

for w = 1/CR1, which is just

$$W = E^2(cos2wt)/(10\ V) \tag{10}$$

which has no dc component. To restore the output to ±10 V when E = 10 V, a feedback attenuator with an approximate ratio of 4 is used between W and Z1; this technique can be used wherever it is desired to achieve a higher overall gain in the transfer function.

The values of R3 and R4 include additional compensation for the effects of the 50 kΩ input resistance of all three interfaces; R2 is included for a similar reason. These resistor values should not be altered without careful calculation of the consequences. With the values shown, the center frequency f_0 is 100 kHz for C = 1 nF. The amplitude of the output is only a weak function of frequency; the output amplitude is 0.5% too low at f = 0.9f_0 and f = 1.1f_0. The cross-connection is simply to produce the cosine output with the sign shown in Equation 10; however, the sign in this case is rarely important.

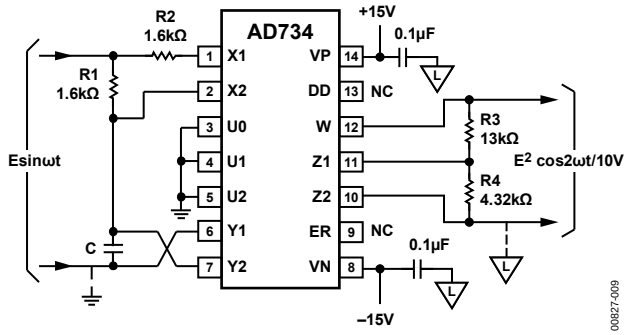


Figure 26. Frequency Doubler

OPERATION AS A DIVIDER

The AD734 supports two methods for performing analog division. The first is based on the use of a multiplier in a feedback loop. This is the standard mode recommended for multipliers having a fixed scaling voltage, such as the AD534, and is described in this section. The second uses the AD734's unique capability for externally varying the scaling (denominator) voltage directly, and is described in the Division by Direct Denominator Control section.

Feedback Divider Connections

Figure 27 shows the connections for the standard (AD534) divider mode. Feedback from the output, W, is now taken to the Y2 (inverting) input, which, if the X input is positive, establishes a negative feedback path. Y1 should normally be connected to the ground associated with the load circuit, but can optionally be used to sum a further signal to the output. If desired, the polarity of the Y input connections can be reversed, with W connected to Y1 and Y2 used as the optional summation input. In this case, either the polarity of the X input connections must be reversed or the X input voltage must be negative.

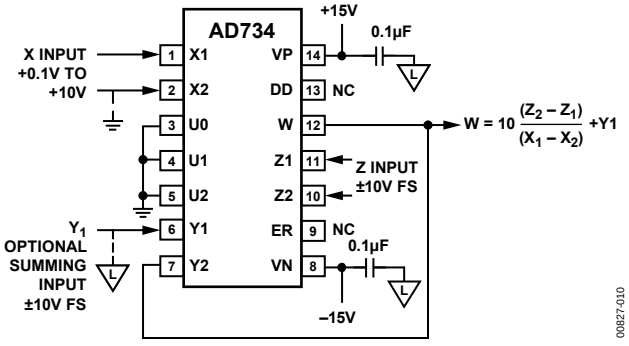


Figure 27. Standard (AD534) Divider Connection

The numerator input, which is differential and can have either polarity, is applied to Pin Z1 and Pin Z2. As with all dividers based on feedback, the bandwidth is directly proportional to the denominator, being 10 MHz for X = 10 V and reducing to 100 kHz for X = 100 mV. This reduction in bandwidth, and the increase in output noise (which is inversely proportional to the denominator voltage) preclude operation much below a denominator of 100 mV. Division using direct control of the denominator (see Figure 29) does not have these shortcomings.

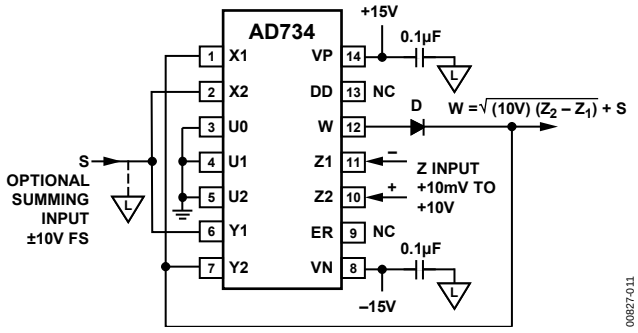


Figure 28. Connection for Square Rooting

Connections for Square-Rooting

The AD734 can be used to generate an output proportional to the square root of an input using the connections shown in Figure 28. Feedback is now via both the X and Y inputs, and is always negative because of the reversed polarity between these two inputs. The Z input must have the polarity shown, but because it is applied to a differential port, either polarity of input can be accepted with reversal of Z1 and Z2, if necessary. The diode, D, which can be any small-signal type (1N4148 being suitable), is included to prevent a latching condition, which can occur if the input is momentarily of the incorrect polarity of the input. The output is always negative.

Note that the loading on the output side of the diode is provided by the 25 kΩ of input resistance at X1 and Y2, and by the user's load. In high speed applications, it may be beneficial to include further loading at the output (to 1 kΩ minimum) to speed up response time. As in previous applications, a further signal, shown in Figure 28 as S, can be summed to the output; if this option is not used, this node should be connected to the load ground.

DIVISION BY DIRECT DENOMINATOR CONTROL

The AD734 can be used as an analog divider by directly varying the denominator voltage. In addition to providing much higher accuracy and bandwidth, this mode also provides greater flexibility, because all inputs remain available. Figure 29 shows the connections for the general case of a three-input multiplier divider, providing the function

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} + Z_2 \qquad (11)$$

where the *X*, *Y*, and *Z* signals can all be positive or negative, but the difference $U = U_1 - U_2$ must be positive and in the range 10 mV to 10 V. If a negative denominator voltage must be used, simply ground the noninverting input of the op amp. As previously noted, the X input must have a magnitude of less than 1.25U.

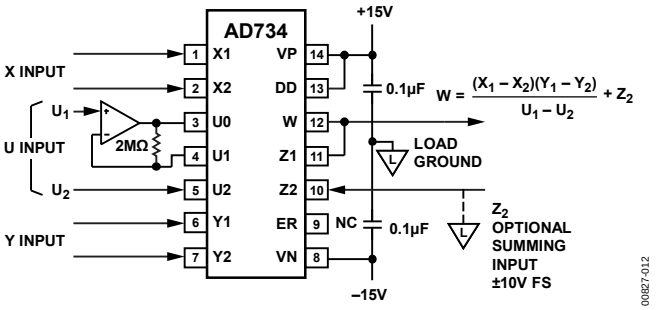


Figure 29. Three-Variable Multiplier/Divider Using Direct Denominator Control

This connection scheme can also be viewed as a variable-gain element, whose output, in response to a signal at the X input, is controllable by both the Y input (for attenuation, using Y less than U) and the U input (for amplification, using U less than Y). The ac performance is shown in Figure 30; for these results, Y was maintained at a constant 10 V. At U = 10 V, the gain is unity and the circuit bandwidth is a full 10 MHz. At U = 1 V, the gain is 20 dB and the bandwidth is essentially unaltered. At U = 100 mV, the gain is 40 dB and the bandwidth is 2 MHz. Finally, at U = 10 mV, the gain is 60 dB and the bandwidth is 250 kHz, corresponding to a 250 MHz gain-bandwidth product.

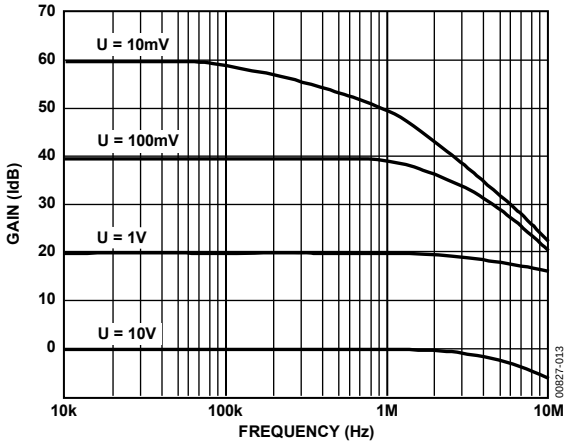


Figure 30. Three-Variable Multiplier/Divider Performance

The 2 MΩ resistor is included to improve the accuracy of the gain for small denominator voltages. At high gains, the X input offset voltage can cause a significant output offset voltage. To eliminate this problem, a low-pass feedback path can be used from W to X2; see Figure 32 for details.

Where a numerator of 10 V is needed, to implement a two-quadrant divider with fixed scaling, the connections shown in Figure 31 can be used. The reference voltage output appearing between Pin 9 (ER) and Pin 8 (VN) is amplified and buffered by the second op amp, to impose 10 V across the Y1/Y2 input. Note that Y2 is connected to the negative supply in this application. This is permissible because the common-mode voltage is still high enough to meet the internal requirements.

The transfer function is

$$W = 10\,V\left(\frac{X_1 - X_2}{U_1 - U_2}\right) + Z_2 \qquad (12)$$

The ac performance of this circuit remains as shown in Figure 30.

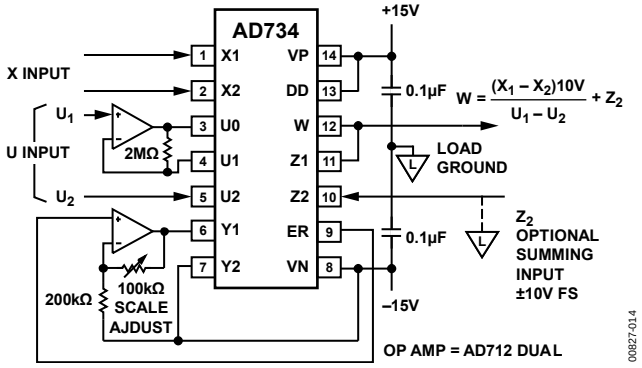


Figure 31. Two-Quadrant Divider with Fixed 10 V Scaling

A PRECISION AGC LOOP

The variable denominator of the AD734 and its high gain bandwidth product make it an excellent choice for precise automatic gain control (AGC) applications. Figure 32 shows a suggested method. The input signal, E_{IN}, which can have a peak amplitude from 10 mV to 10 V at any frequency from 100 Hz to 10 MHz, is applied to the X input and a fixed positive voltage E_C to the Y input. Op Amp A2 and Capacitor C2 form an integrator with a current summing node at its inverting input. (The AD712 dual op amp is a suitable choice for this application.) In the absence of an input, the current in D2 and R2 causes the integrator output to ramp negative, clamped by Diode D3, which is included to reduce the time required for the loop to establish a stable, calibrated, output level after the circuit has received an input signal. With no input to the denominator (U0 and U2), the gain of the AD734 is very high (about 70 dB), and thus even a small input causes a substantial output.

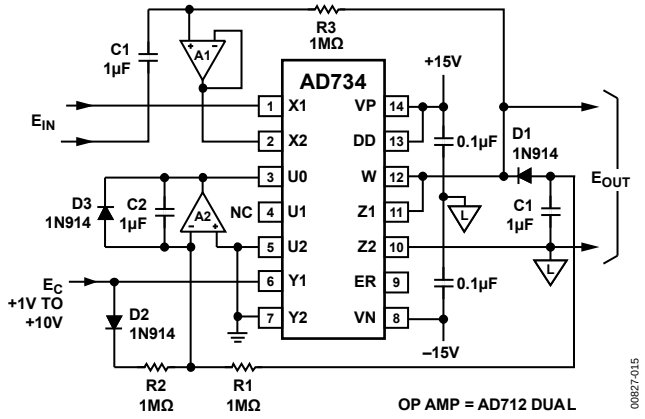


Figure 32. Precision AGC Loop

Diode D1 and C1 form a peak detector, which rectifies the output and causes the integrator to ramp positive. When the current in R1 balances the current in R2, the integrator output holds the denominator output at a constant value. This occurs when there

is sufficient gain to raise the amplitude of E_{IN} to that required to establish an output amplitude of E_C over the range of 1 V to 10 V. The X input of the AD734, which has finite offset voltage, can be troublesome at the output at high gains. The output offset is reduced to that of the X input (1 mV or 2 mV) by the offset loop comprising R3, C3, and Buffer A1. The low-pass corner frequency of 0.16 Hz is transformed to a high-pass corner that is multiplied by the gain (for example, 160 Hz at a gain of 1000).

In applications not requiring operation down to low frequencies, Amplifier A1 can be eliminated, but the AD734's input resistance of 50 kΩ between X1 and X2 reduces the time constant and increases the input offset. Using a nonpolar 20 mF tantalum capacitor for C1 results in the same unity-gain high-pass corner; in this case, the offset gain increases to 20, which is still acceptable.

Figure 33 shows the error in the output for sinusoidal inputs at 100 Hz, 100 kHz, and 1 MHz, with E_C set to 10 V. The output error for any frequency between 300 Hz and 300 kHz is similar to that for 100 kHz. At low signal frequencies and low input amplitudes, the dynamics of the control loop determine the gain error and distortion; at high frequencies, the 200 MHz gain-bandwidth product of the AD734 limits the available gain.

The output amplitude tracks E_C over the range of 1 V to slightly more than 10 V.

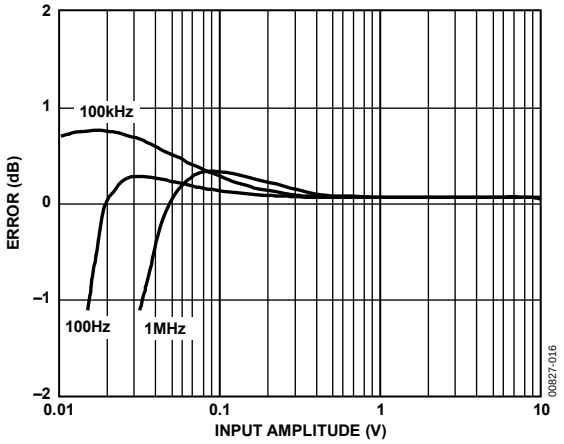


Figure 33. AGC Amplifier Output Error vs. Input Voltage

WIDEBAND RMS-TO-DC CONVERTER USING U INTERFACE

The AD734 is well-suited to such applications as implicit rms-to-dc conversion, where the AD734 implements the function

$$V_{RMS} = \frac{\text{avg}[V_{IN}{}^2]}{V_{RMS}} \quad (13)$$

using its direct divide mode. Figure 34 shows the circuit.

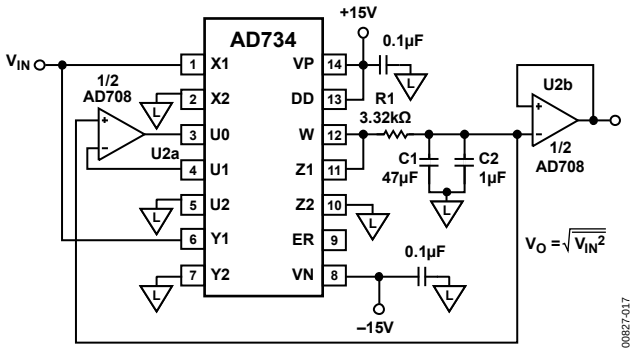


Figure 34. A Two-Chip, Wideband RMS-to-DC Converter

In this application, the AD734 and an AD708 dual op amp serve as a two-chip rms-to-dc converter with a 10 MHz bandwidth. Figure 35 shows the circuit's performance for square-, sine-, and triangle-wave inputs. The circuit accepts signals as high as 10 V p-p with a crest factor of 1 or 1 V p-p with a crest factor of 10. The circuit's response is flat to 10 MHz with an input of 10 V, flat to almost 5 MHz for an input of 1 V, and to almost 1 MHz for inputs of 100 mV. For accurate measurements of input levels below 100 mV, the AD734's output offset (Z interface) voltage, which contributes a dc error, must be trimmed out.

In the circuit shown in Figure 34, the AD734 squares the input signal, and its output ($V_{IN}{}^2$) is averaged by a low-pass filter that consists of R1 and C1 and has a corner frequency of 1 Hz. Because of the implicit feedback loop, this value is both the output value, V_{RMS}, and the denominator in Equation 13. U2a and U2b, an AD708 dual dc precision op amp, serve as unity-gain buffers, supplying both the output voltage and driving the U interface.

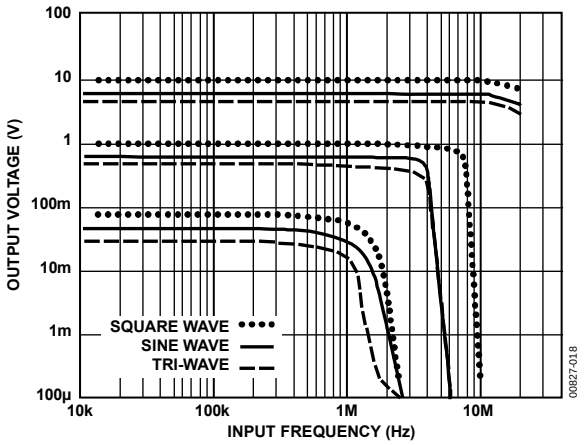


Figure 35. RMS-to-DC Converter Performance

LOW DISTORTION MIXER

The AD734's low noise and distortion make it especially suitable for use as a mixer, modulator, or demodulator. Although the AD734's −3 dB bandwidth is typically 10 MHz and is established by the output amplifier, the bandwidth of its X and Y interfaces and the multiplier core are typically in excess of 40 MHz. Thus, provided that the desired output signal is less than 10 MHz, as is typically the case in demodulation, the AD734 can be used with both its X and Y input signals as high as 40 MHz. One test of mixer performance is to linearly combine two closely spaced, equal-amplitude sinusoidal signals and then mix them with a third signal to determine the mixer's two-tone, third-order intermodulation products.

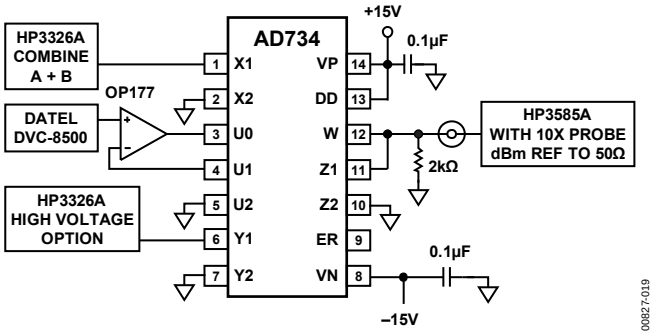


Figure 36. AD734 Mixer Test Circuit

Figure 36 shows a test circuit for measuring the AD734's performance in this regard. In this test, two signals, at 10.05 MHz and 9.95 MHz, are summed and applied to the AD734 X interface. A second 9 MHz signal is applied to the AD734 Y interface. The voltage at the U interface is set to 2 V to use the full dynamic range of the AD734; that is, by connecting the W and Z1 pins together, grounding the Y2 and X2 pins, and setting U = 2 V, the overall transfer function is

$$W = \frac{X_1 Y_1}{2V} \tag{14}$$

and W can be as high as 20 V p-p when X1 = 2 V p-p and Y1 = 10 V p-p. The 2 V p-p signal level corresponds to 10 dBm into a 50 Ω input termination resistor connected from X1 or Y1 to ground.

If the two X1 inputs are at Frequency f_1 and Frequency f_2 and the frequency at the Y1 input is f_0, then the two-tone third-order intermodulation products should appear at Frequency $2f_1 - f_2 \pm f_0$ and Frequency $2f_2 - f_1 \pm f_0$. Figure 37 and Figure 38 show the output spectra of the AD734 with f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz for a signal level of $f_1 = f_2$ = 6 dBm and f_0 = +24 dBm in Figure 37 and $f_1 = f_2$ = 0 dBm and f_0 = +24 dBm in Figure 38. This performance is without external trimming of the AD734 X and Y input offset voltages.

The possible two-tone intermodulation products are at 2 × 9.95 MHz − 10.05 MHz ± 9.00 MHz and 2 × 10.05 − 9.95 MHz ± 9.00 MHz; of these, only the third-order products at 0.850 MHz and 1.150 MHz are within the 10 MHz bandwidth of the AD734; the desired output signals are at 0.950 MHz and 1.050 MHz. Note that the difference between the desired outputs and third-order products (see Figure 37) is approximately 78 dB, which corresponds to a computed third-order intercept point of +46 dBm.

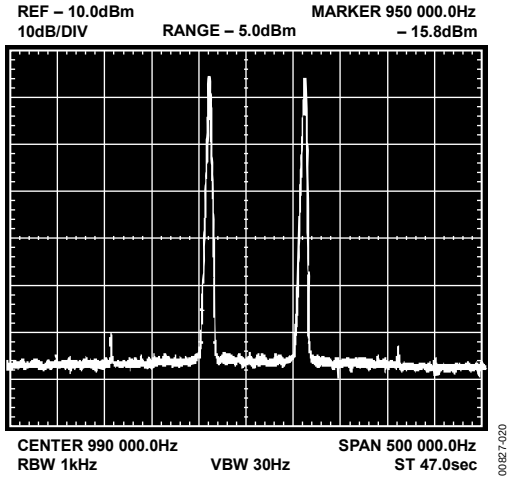


Figure 37. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of $f_1 = f_2$ = 6 dBm and f_0 = +24 dBm (All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output)

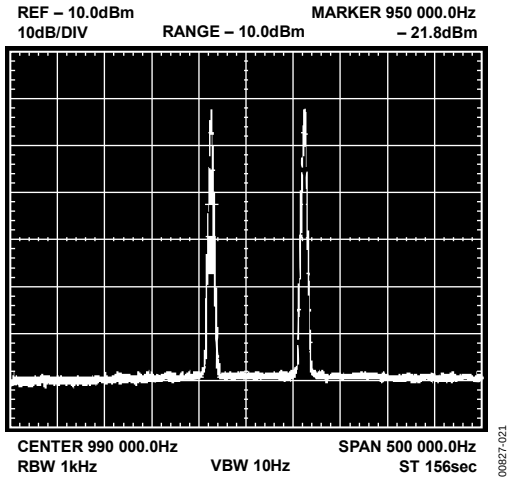
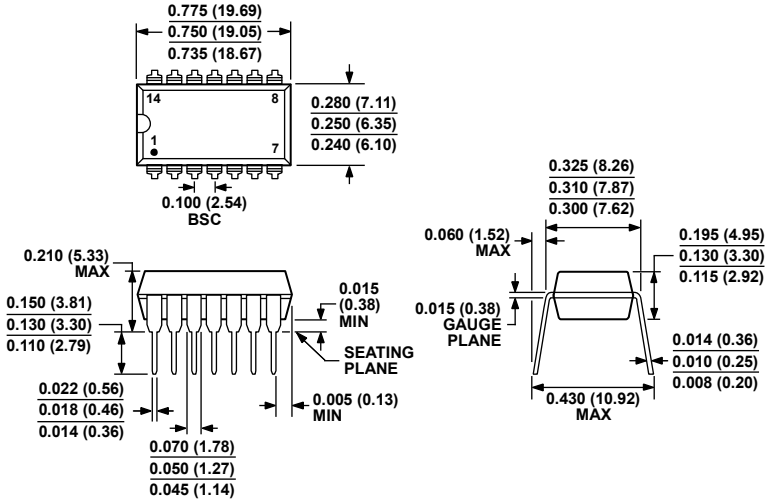


Figure 38. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of $f_1 = f_2$ = 0 dBm and f_0 = +24 dBm (All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output)

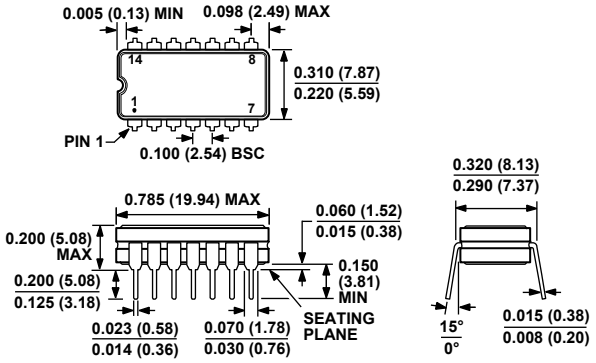
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

070606-A

Figure 39. 14-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-14)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 40. 14-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-14)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD734AN	−40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD734ANZ	−40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD734BN	−40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD734BNZ	−40°C to +85°C	14-Lead Plastic Dual In-Line Package [PDIP]	N-14
AD734AQ	−40°C to +85°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD734BQ	−40°C to +85°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD734SQ/883B	−55°C to +125°C	14-Lead Ceramic Dual In-Line Package [CERDIP]	Q-14
AD734SCHIPS	−55°C to +125°C	Die	

[1] Z = RoHS Compliant Part.

NOTES

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