National Semiconductor Corporation

DM54259/DM74259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

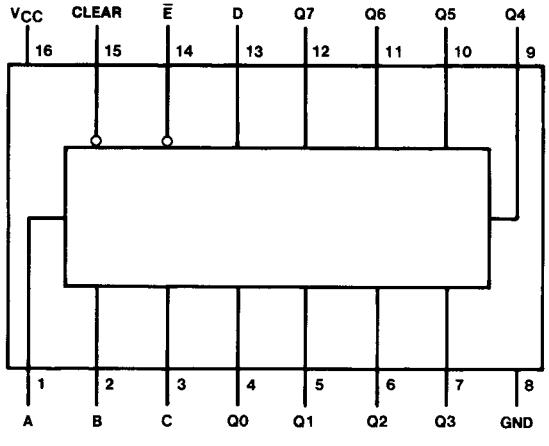
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
  - Enable-to-output 18 ns
  - Data-to-output 21 ns
  - Address-to-output 22 ns
  - Clear-to-output 21 ns
- Fan-Out
  - I_{OL} (sink current) 16 mA
  - I_{OH} (source current) −0.8 mA
- Typical I_{CC} 60 mA

Connection Diagram

Dual-In-Line Package



TL/F/6569–1

Order Number DM54259J or DM74259N
See NS Package Number J16A or N16A

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Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54259			DM74259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width (Note 6)	Enable	19	13		19	13		ns
		Clear	19	13		19	13		
t_{SU}	Setup Time (Notes 1, 2, 3 & 6)	Data	20	13		20	13		ns
		Select	10	5		10	5		
t_H	Hold Time (Notes 1 & 6)	Data	0	−10		0	−10		ns
		Select	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−55	mA
			DM74	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)				90	mA

Note 1: Setup and hold times are with reference to the enable input.

Note 2: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

Note 5: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		31	ns

Function Tables

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level

D = The level of the data input

Q_{i0} = The level of Q_i (i = 0, 1, ... 7, as appropriate) before the indicated steady-state input conditions were established.