FAIRCHILD SEMICONDUCTOR®

October 2007

FSAL200 — Wide Bandwidth Quad 2:1 Analog Multiplexer / De-multiplexer Switch

Features

- Typical 6Ω Switch Connection Between Two Ports
- Minimal Propagation Delay Through the Switch
- Low I_{CC}
- Zero Bounce in Flow-Through Mode
- Control Inputs Compatible with TTL Level
- Rail-to-Rail Signal Handling
- Route Communications Signals Include:
  - 10/100 Ethernet
  - 100VG—AnyLAN
  - ATM25
  - SONET OCI 51.8Mbps
  - USB1.1
  - T1/E1
  - Token Ring 4/16Mbps

Description

The Fairchild Switch FSAL200 is a rail-to-rail quad 2:1 high-speed CMOS TTL-compatible analog multiplexer / de-multiplexer switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When OE is low, the select pin connects the A Port to the selected B Port output. When OE is high, the switch is open and a high-impedance state exists between the two ports.

Ordering Information

Part Number	Package Description	Packing Method
FSAL200MTC	16-Lead Thin Shrink Small Outline Package(TSSOP), JEDEC MO-153, 4.4mm Wide	Rails
FSAL200MTCX	16-Lead Thin Shrink Small Outline Package(TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel
FSAL200QSC	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide	Rails
FSAL200QSCX	16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide	Tape and Reel

All packages are Pb-free per JEDEC standard J-SDD-020B.

© 2002 Fairchild Semiconductor Corporation

Pin Configurations

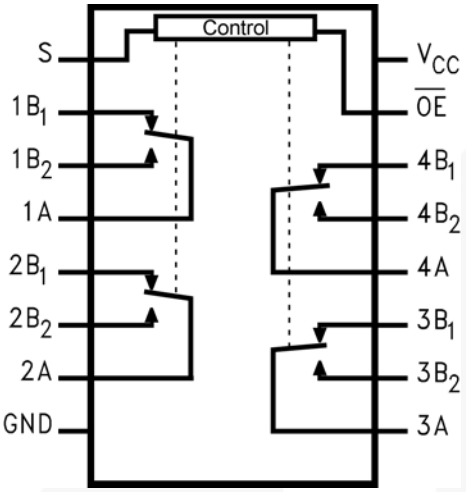


Figure 1. Analog Symbol

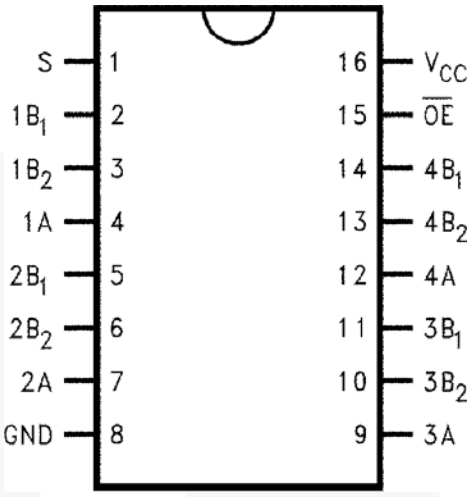


Figure 2. Connection Diagram

Control Input(s)	$\overline{OE}$	Function
X	High	Disconnected
Low	Low	A=B1
High	Low	A=B2

Pin Descriptions

Pin Names	Function
$\overline{OE}$	Switch Enable
S	Select Input
A, B1, B2	Data Ports

© 2002 Fairchild Semiconductor Corporation

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	7.0	V
V_{SW}	DC Switch Voltage[1]	-0.5	0.5	V
V_{IN}	DC Input Voltage[1]	-0.5	7.0	V
I_{IK}	DC Input Diode Current at (I_{IK}) V_{IN} < 0V		-50	mA
I_{OUT}	DC Output Current		120	mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current		±100	mA
P_D	Power Dissipation at 85°C		0.5	W
T_{STG}	Storage Temperature Range	-65	+150	°C
T_A	Ambient Temperature with Power Applied	-40	+85	°C

Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		3.0	5.5	V
V_{IN}	Control Input Voltage[2]		0	V_{CC}	V
V_{SW}	Switch Input Voltage			V_{CC}	V
V_{OUT}	Output Voltage			V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r,t_f	Input Rise and Fall Time	Control Input V_{CC}=2.3V -3.6V	0	10	ns/V
		Control Input V_{CC}=4.5V -5.5V	0	5	
θ_{JA}	Thermal Resistance in Still Sir				°C/W

Note:

2. Control input must be held HIGH or LOW and it must not float.

© 2002 Fairchild Semiconductor Corporation

DC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}(V)	T_A=-40°C to +85°C			Units
				Min.	Typ.	Max.	
V_{IH}	Input Voltage High		4.5 to 5.5	2.0			V
			3.0 to 3.6	2.0			
V_{IL}	Input Voltage Low		4.5 to 5.5	-0.5		0.8	V
			3.0 to 3.6	-0.5		0.8	
I_{OZ}	Off State Leakage Current	$0 \le V_{IN} \le 5.5V$	0 to 5.5			100	µA
R_{ON}	Switch On Resistance(3)	I_{ON}=10 -30mA	4.5 to 5.5		6	12	Ω
		I_{ON}=10 -30mA	3.0 to 3.6		15	22	
I_{IN}	Control Input Leakage	$V_{IN}=V_{CC}$ or GND	5.5			±1	µA
		$V_{IN}=V_{CC}$ or GND	3.6			±1	
I_{CC}	Quiescent Supply Current, All Channels Off	$V_{IN}=V_{CC}$ or GND, I_{OUT}=0	5.5			1	µA
	Analog Signal Range		V_{CC}	0		V_{CC}	V
ΔR_{ON}	On Resistance Matching Between Channels(3)(4)	I_A=-30 mA, V_{BN}=3.15	4.5 to 5.5		0.4	2.0	Ω
		I_A=-10 mA, V_{BN}=2.1	3.0 to 3.6		1.0	3.0	
I_O	Output Current	B_n, B_n, S-0V to 5V	4.5 to 5.5	100			mA
			3.0 to 3.6	80			
$R_{FLAT(ON)}$	On Resistance Flatness(3)(5)	A_1, B_1, B_2=0V to 5V	4.5 to 5.5		3		Ω
		A_1, B_1, B_2=0V to 5V	3.0 to 3.6		7		

Notes:

3. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B ports).
4. $\Delta R_{ON} = R_{ON}$ maximum – R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

© 2002 Fairchild Semiconductor Corporation

AC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}(V)	Min.	Typ.	Max.	Units	Figure
t_{ON}	Turn-On Time	VB_n=3V	4.5 to 5.5		10	20	ns	Figure 3
		VB_n=1.5V	3.0 to 3.6		28	40		Figure 4
t_{OFF}	Turn-Off Time	VB_n-3V	4.5 to 5.5		5	10	ns	Figure 3
		VB_n=1.5V	3.0 to 3.6		4	20		Figure 4
Q	Charge Injection	C_L=0.1nF,V_{GEN}=0 R_{GEN}=0Ω	5.0		7		pC	Figure 5
			3.3		3			
OIRR	Off Isolation	R_L=100Ω ,f=30MHz	4.5 to 5.5		-55		dB	Figure 6
		R_L=50Ω, f=1MHz	3.0 to 3.6		-75			
Xtalk	Crosstalk	R_L=100Ω ,f=30MHz	4.5 to 5.5		-70		dB	Figure 7
		R_L=50Ω, f=1MHz	3.0 to 3.6		-75			
BW	-3db Bandwidth	R_L=100Ω	4.5 to 5.5		137		MHz	Figure 9
		R_L=50Ω	3.0 to 3.6		110			
D	$\Delta R_{ON/RL}$	R_L=100Ω	4.5 to 5.5		2		%	Figure 9
			3.0 to 3.6		3			

Notes:
6. Guaranteed by design.
7. Off Isolation =20 $\log_{10}$ [V_A / V_{Bn}].

Capacitance

T_A=+25°C, f=1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typ.	Units	Figure
C_{IN}	Control Pin Input Capacitance	V_{CC}=0V	2.3	pF	
C_{IO-B}	B Port Off Capacitance	V_{CC}=5.0V and 3.0V	8	pF	Figure 10
	A Port Off Capacitance	V_{CC}=5.0V and 3.0V	13		Figure 10
C_{ON}	Channel On Capacitance	V_{CC}=5.0V and 3.0V	15	pF	Figure 7

© 2002 Fairchild Semiconductor Corporation

AC Loadings and Waveforms

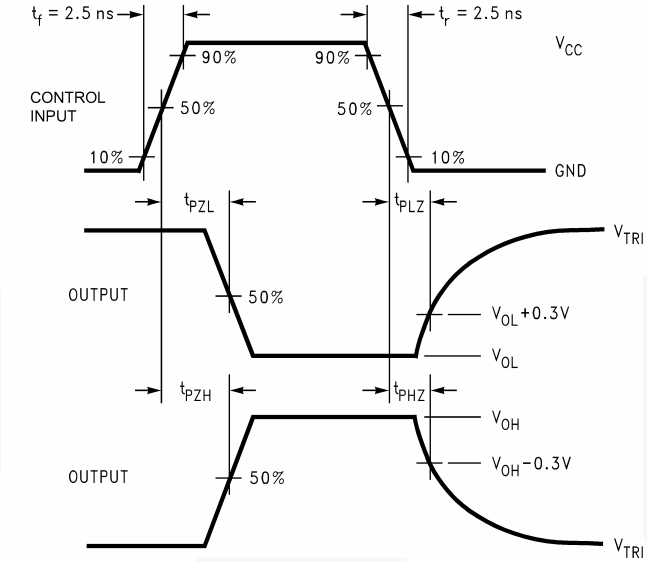


Figure 3. AC Waveforms

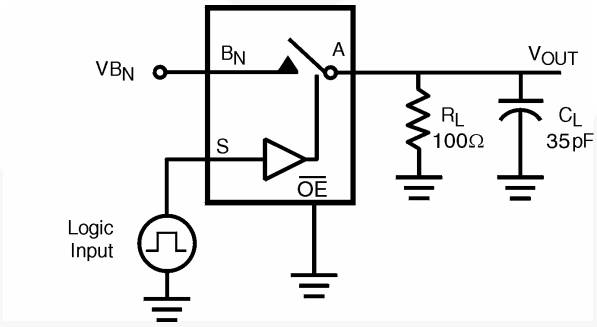
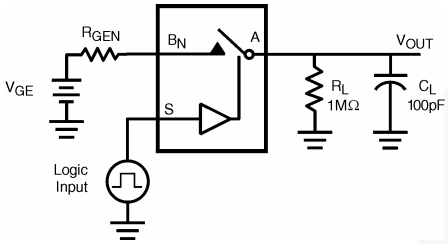


Figure 4. t_{on}, t_{off} Loading

© 2002 Fairchild Semiconductor Corporation

AC Loadings and Waveforms (Continued)



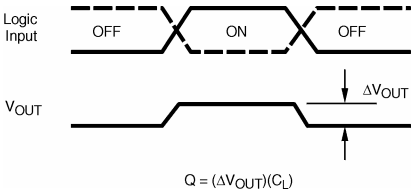


Figure 5. Charge Injection Test

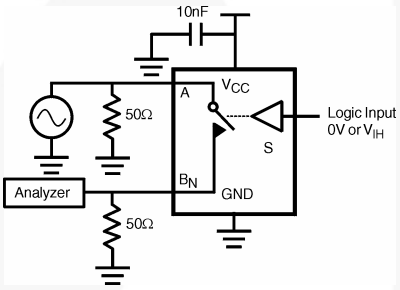


Figure 6. Off Isolation

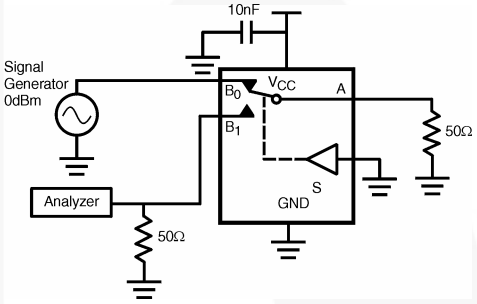


Figure 7. Channel On Capacitance

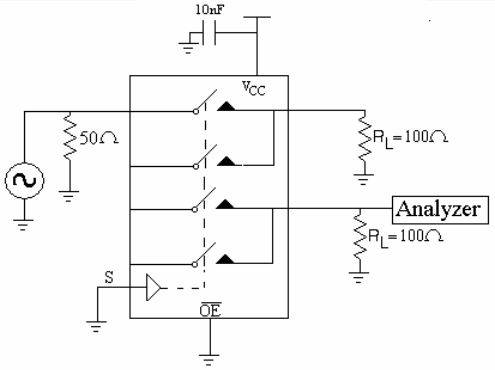


Figure 8. Crosstalk

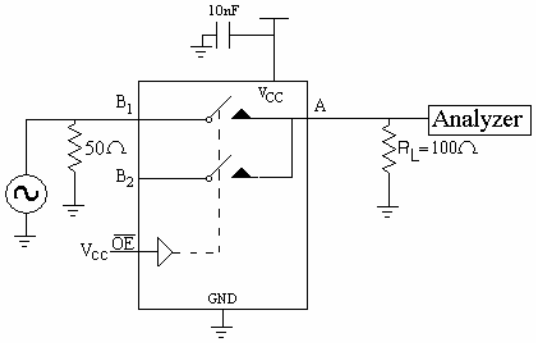


Figure 9. Bandwidth

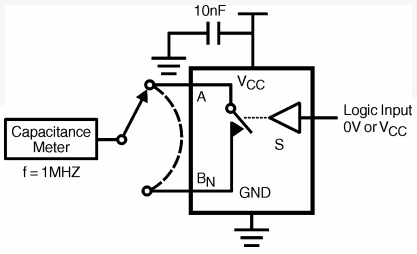


Figure 10. Channel Off Capacitance

Physical Dimensions

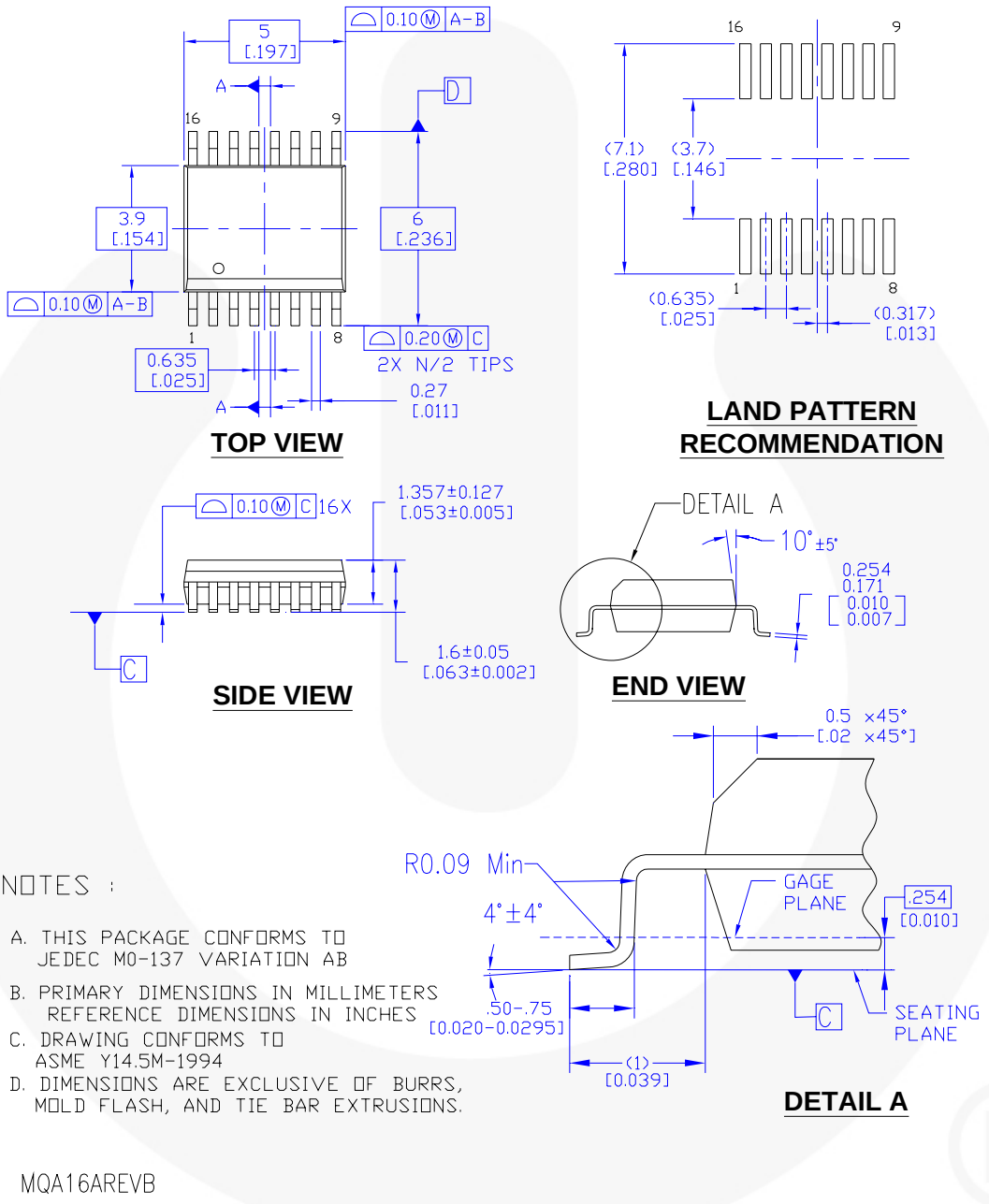
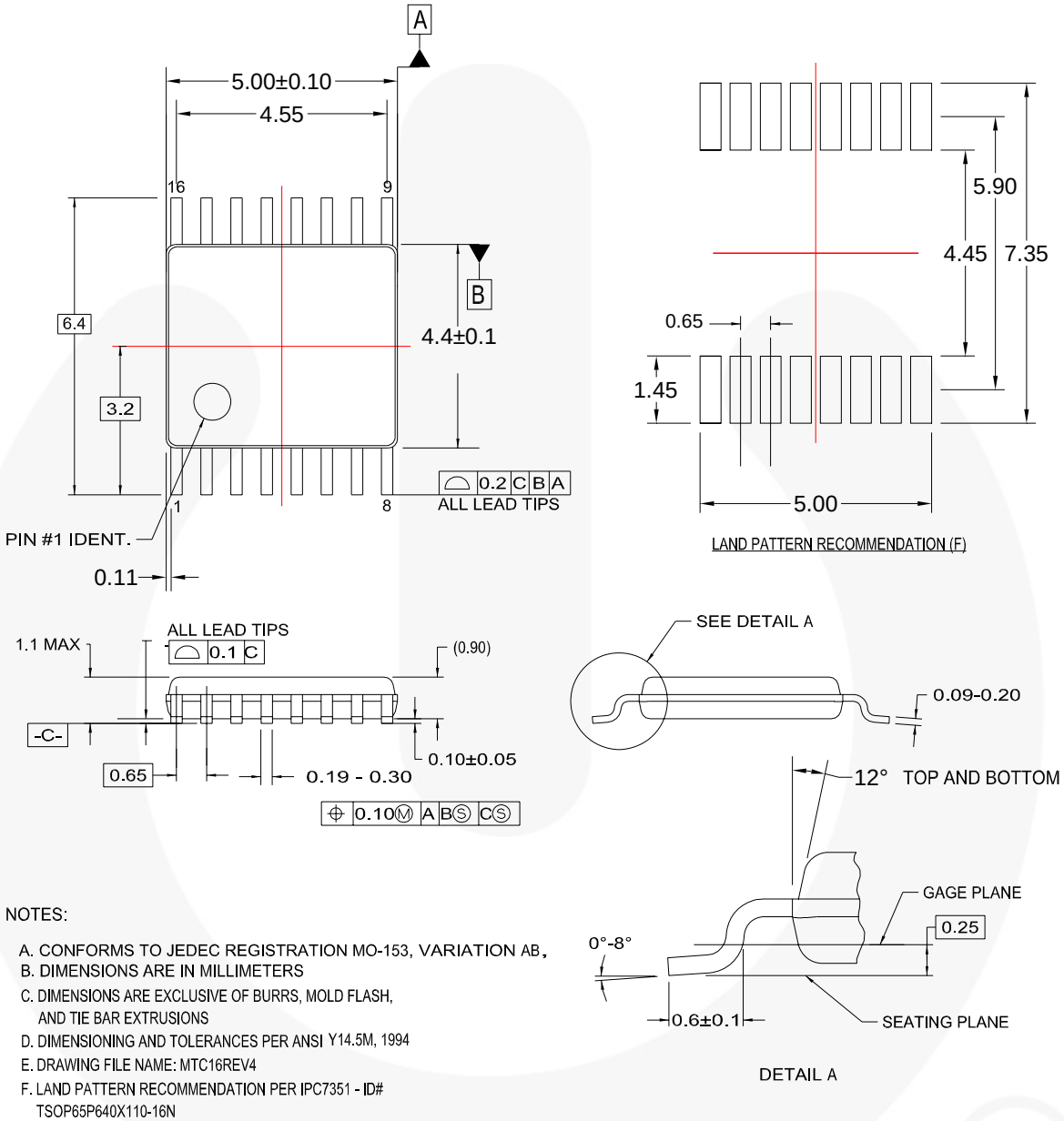


Figure 11. 16-lead, Quarter Size Outline Package (QSOP), JEDEC MO-137. 0.150" wide

Click here for tape and reel specifications, available at:

http://www.fairchildsemi.com/products/analog/pdf/qsop16_tr.pdf

Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1994
E. DRAWING FILE NAME: MTC16REV4
F. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N

MTC16rev4

Figure 12. 16-lead, Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm wide

Click here for tape and reel specifications, available at:

http://www.fairchildsemi.com/products/analog/pdf/tssop16_tr.pdf

© 2002 Fairchild Semiconductor Corporation

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following are registered and unregistered trademarks and service marks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx®
Build it Now™
CorePLUS™
CROSSVOLT™
CTL™
Current Transfer Logic™
EcoSPARK®
ƒ®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FPS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
GTO™
i-Lo™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
®
PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
UniFET™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I31

© 2002 Fairchild Semiconductor Corporation

© 2002 Fairchild Semiconductor Corporation