

MAX14760/MAX14762/MAX14764

Above- and Below-the-Rails Low-Leakage Analog Switches

General Description

The MAX14760/MAX14762/MAX14764 analog switches are capable of passing bipolar signals that are beyond their supply rails. These devices operate from a single +3.0V to +5.5V supply, and support signals in the -25V to +25V range.

The MAX14760 is a single-pole/single-throw (SPST) analog switch, while the MAX14762 is a dual-SPST analog switch. The MAX14764 is a single-pole/double-throw (SPDT) analog switch.

The MAX14760/MAX14762/MAX14764 feature 20Ω (max) on-resistance with a ±10nA (max) on-leakage current for MAX14760/MAX14762.

The MAX14760/MAX14764 are available in 8-pin (3mm x 3mm) TDFN packages. The MAX14762 is available in a 10-pin (3mm x 3mm) TDFN package. These devices are specified over the -40°C to +85°C extended operating temperature range.

Ordering Information/Selector Guide appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maxim-ic.com/MAX14760.related.

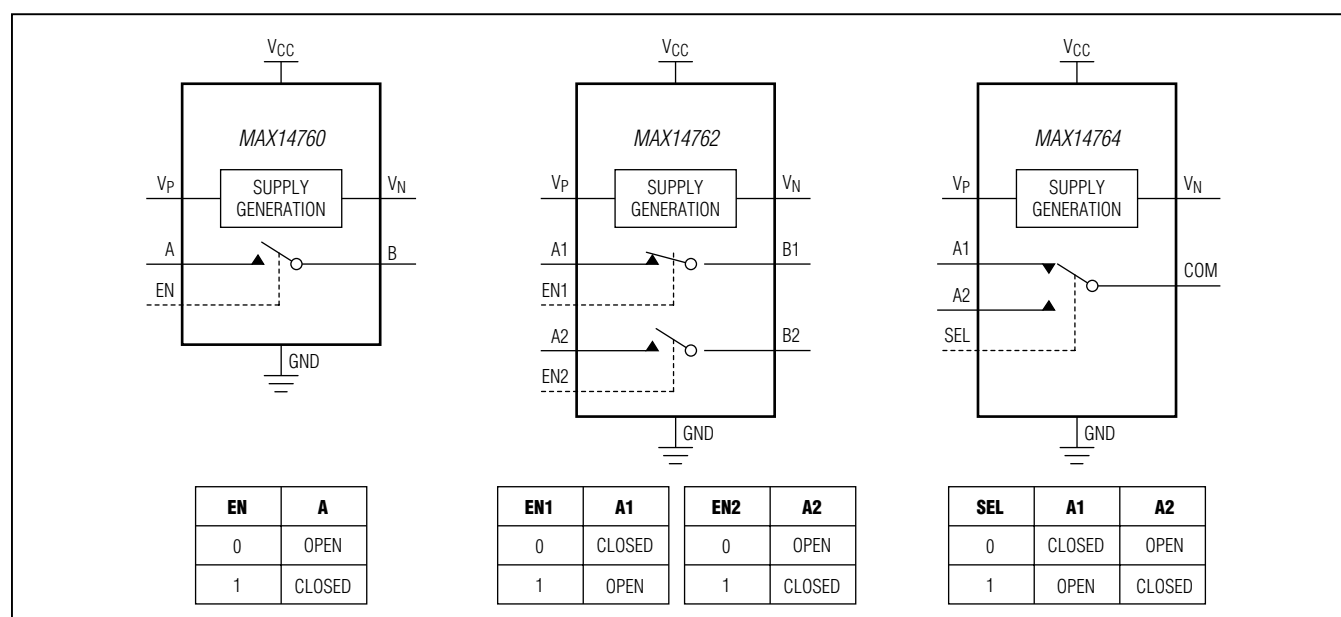
Benefits and Features

- ◆ **Simplify Power-Supply Requirements**
 - ◇ 3.0V to 5.5V Supply Range
 - ◇ -25V to +25V Signal Range
- ◆ **High Performance**
 - ◇ ±10nA (max) On-Leakage Current (MAX14760/MAX14762)
 - ◇ 20Ω (max) On-Resistance
 - ◇ Low On-Resistance Flatness, 58mΩ (typ)
 - ◇ Thermal Shutdown Protection
 - ◇ -40°C to +85°C Operating Temperature Range
 - ◇ High Bandwidth: 115MHz (typ)
- ◆ **Save Space on Board**
 - ◇ Small 8-Pin and 10-Pin TDFN Packages

Applications

Industrial Measurement Systems
Instrumentation Systems
Opto-Relay Replacement
Medical Systems
ATE Systems
Audio Signal Routing and Switching

Functional Diagrams/Truth Tables



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ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

V_{CC}-0.3V to +6V
EN, EN1, EN2, SEL-0.3V to $+(V_{CC} + 0.3V)$
A, A1, A2, B, B1, B2, COM $(V_N - 0.3V)$ to Lesser of
 $(V_P + 0.3V)$ or $(V_N + 52V)$
 V_P -0.3V to Lesser of $(+52V)$ or $(V_N + 70V)$
 V_N Greater of $(V_{CC} - 40V)$ or $(V_P - 70V)$ to $+0.3V$
 V_P to V_N-0.3V to 70V
Continuous Current $\pm 25mA$

Continuous Power Dissipation ($T_A = +70^\circ C$)

8-Pin TDFN Package (derate 24.4mW/ $^\circ C$
above $+70^\circ C$)..... 1951.2mW
10-Pin TDFN Package (derate 24.4mW/ $^\circ C$
above $+70^\circ C$)..... 1951.2mW
Operating Temperature Range..... $-40^\circ C$ to $+85^\circ C$
Storage Temperature Range..... $-65^\circ C$ to $+160^\circ C$
Lead Temperature (soldering, 10s) $+300^\circ C$
Soldering Temperature (reflow) $+260^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

8 TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA})..... $41^\circ C/W$
Junction-to-Case Thermal Resistance (θ_{JC})..... $8^\circ C/W$

10 TDFN

Junction-to-Ambient Thermal Resistance (θ_{JA})..... $41^\circ C/W$
Junction-to-Case Thermal Resistance (θ_{JC})..... $9^\circ C/W$

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $5.5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$, and $T_A = +25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Power Supply Range	V _{CC}			3.0		5.5	V
Continuous Current Through Switch	I _A			-25		+25	mA
Supply Current	I _{CC}	V _{CC} ≤ 4.7V	V _{EN_} = V _{CC}		4.1	10	mA
			V _{EN_} = V _{CC} /2		4.1	10	
		V _{CC} > 4.7V	V _{EN_} = V _{CC}		2.5	6	
			V _{EN_} = V _{CC} /2		2.5	6	
Analog Signal Range	V _{COM} , V _{A_} , V _{B_}	Switch open or closed		-25		+25	V
On-Resistance	R _{ON}	I _{COM} or I _{B_} = ±25mA, V _{A_} = ±25V			8	20	Ω
On-Resistance Flatness	ΔR _{ON}	-25V < V _{A_} < +25V, I _{COM} or I _{B_} = ±25mA			58		mΩ
A, A1, A2 Off-Leakage Current	I _{A_(OFF)}	V _{A_} = +25V, V _{COM} or V _{B_} = 0V, Figure 1		-30		+30	nA
COM, B, B1, B2 Off-Leakage Current	I _{COM(OFF)} , I _{B_(OFF)}	V _{COM} or V _{B_} = 15V, V _{A_} = 0V, Figure 1 (MAX14764)		-10		+10	nA
		V _{B_} = 15V, V _{A_} = 0V, Figure 1 (MAX14760/MAX14762)		-10		+10	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3.0V$ to $5.5V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = 5V$, and $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Leakage Current	I _{ON}	V _{A_} = ±25V, B/COM is unconnected, Figure 1 (MAX14760/MAX14762)	-10		+10	nA
		V _{A_} = ±25V, B/COM is unconnected, Figure 1 (MAX14764)	-30		+30	
DIGITAL LOGIC						
Input-Voltage Logic-Low	V _{IL}	V _{CC} = 3.0V			0.7	V
		V _{CC} = 3.6V			0.7	
		V _{CC} = 4.5V			0.8	
		V _{CC} = 5.5V			0.8	
Input-Voltage Logic-High	V _{IH}	V _{CC} = 3.0V	1.7			V
		V _{CC} = 3.6V	1.9			
		V _{CC} = 4.5V	2.0			
		V _{CC} = 5.5V	2.1			
Input Current	I _L		-1		+1	μA
AC CHARACTERISTICS						
Power-On Time	t _{PWRON}	C _{VP} = C _{VN} = 100nF (Note 3)		50		ms
Enable Turn-On Time	t _{ON}	V _{A_} = ±10V, R _L = 10kΩ, Figure 2 (MAX14760/MAX14762)		100	200	μs
		V _{A_} = ±10V, R _L = 10kΩ, Figure 2 (MAX14764)		1.04	1.6	ms
Enable Turn-Off Time	t _{OFF}	(Figure 2)		110	400	μs
Break-Before-Make Interval	t _{BBM}	V _{A_} = 1V _{RMS} , R _L = 10kΩ, Figure 3 (MAX14764)		740		μs
Off-Isolation	V _{ISO}	V _{A_} = 1V _{RMS} , f = 100kHz, R _L = 50Ω, C _L = 15pF, Figure 4		-77		dB
Crosstalk	V _{CT}	R _S = R _L = 50Ω, f = 100kHz, V _{COM} = 1V _{RMS} , Figure 5 (MAX14764)		-92		dB
-3dB Bandwidth	BW	R _S = 50Ω, R _L = 1kΩ , V _{A_} = 1V _{P-P} , Figure 6		115		MHz
Total Harmonic Distortion	THD+N	R _S = R _L = 1kΩ, f = 20Hz to 20kHz		0.005		%
Charge Injection	Q	V _{A_} = GND, C _L = 1nF, Figure 7		19		pC
Input Capacitance	C _{IN}	At A, A1, A2, B, B1, B2, and COM pins		32		pF
THERMAL PROTECTION						
Thermal Shutdown Temperature	t _{HYST}			+154		°C
Shutdown Temperature Hysteresis	t _{SHUT}			24		°C
ESD PROTECTION						
All Pins		Human Body Model		±2		kV

Note 2: All devices are 100% production tested at $T_A = +25^{\circ}C$. Specifications over operating temperature range are guaranteed by design.

Note 3: The power-on time is defined as the settling time for the charge pump's output to reach steady-state value within 1%.

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Test Circuits/Timing Diagrams

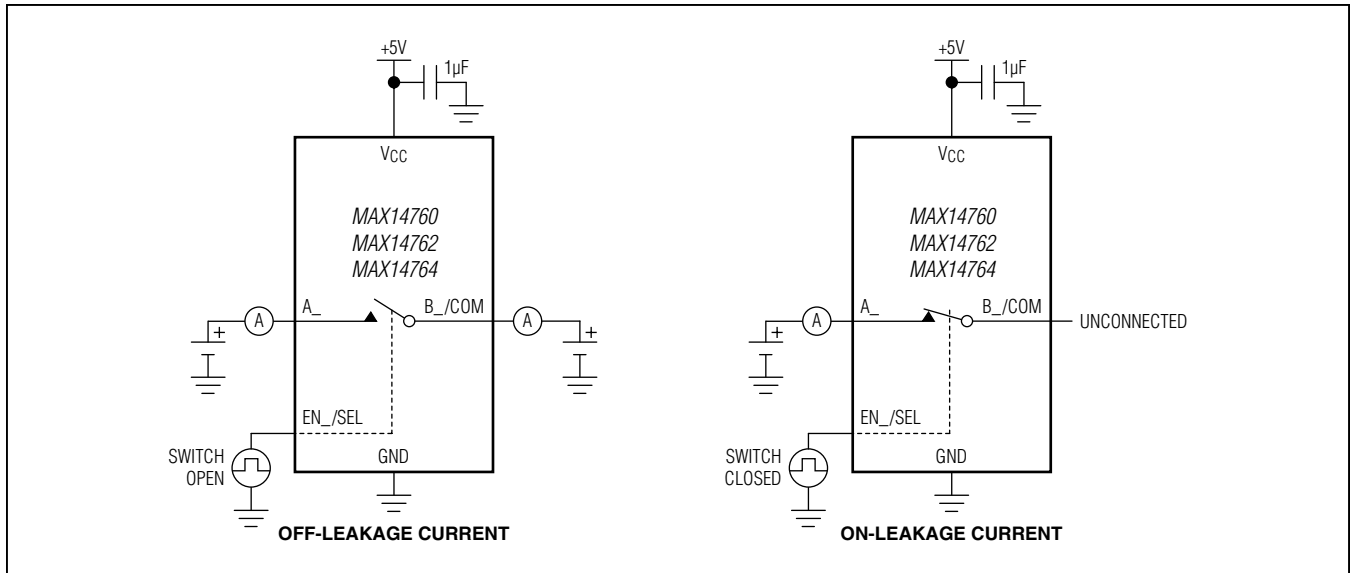


Figure 1. Leakage Current Measurement

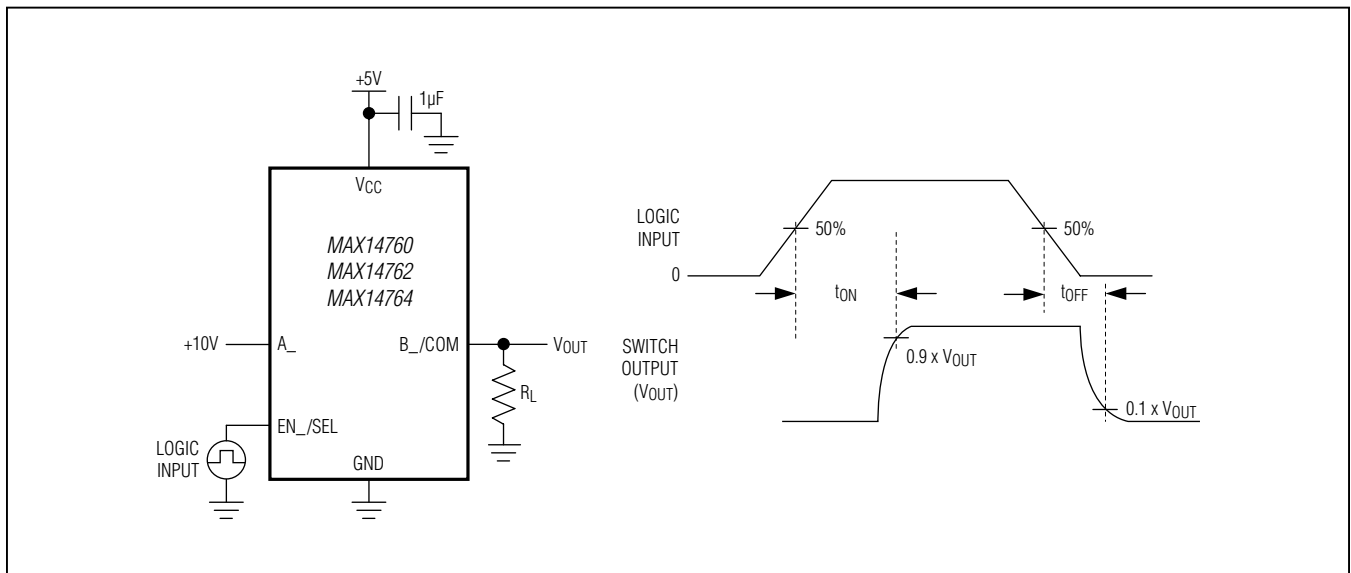


Figure 2. Switching Time

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Test Circuits/Timing Diagrams (continued)

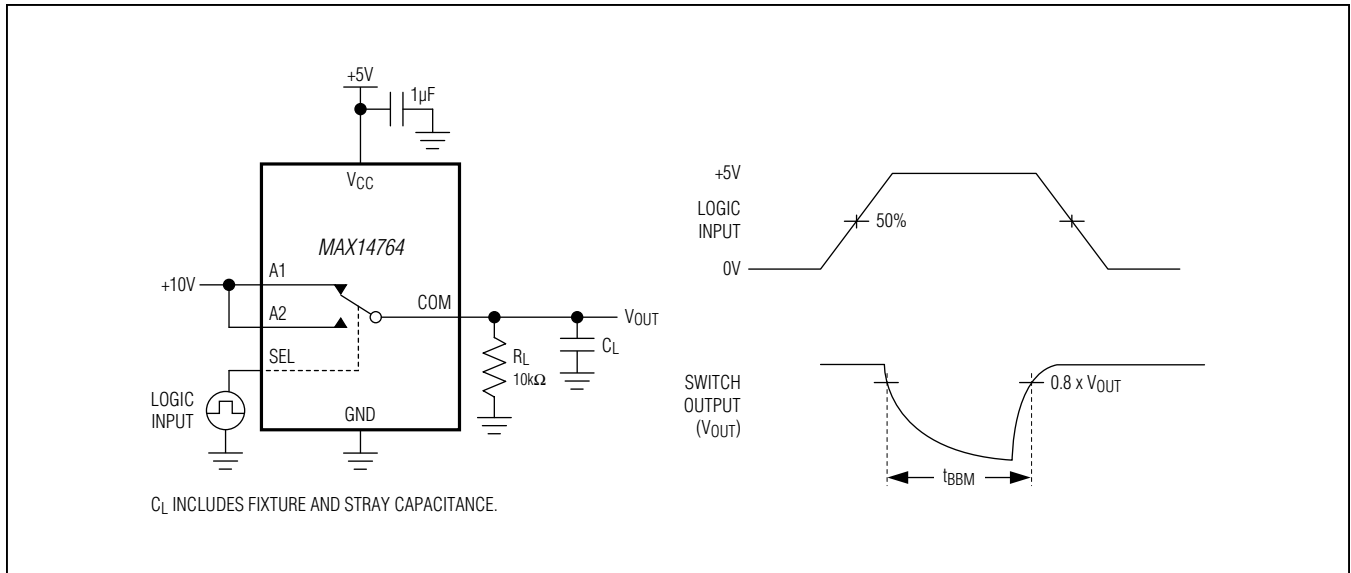


Figure 3. Break-Before-Make

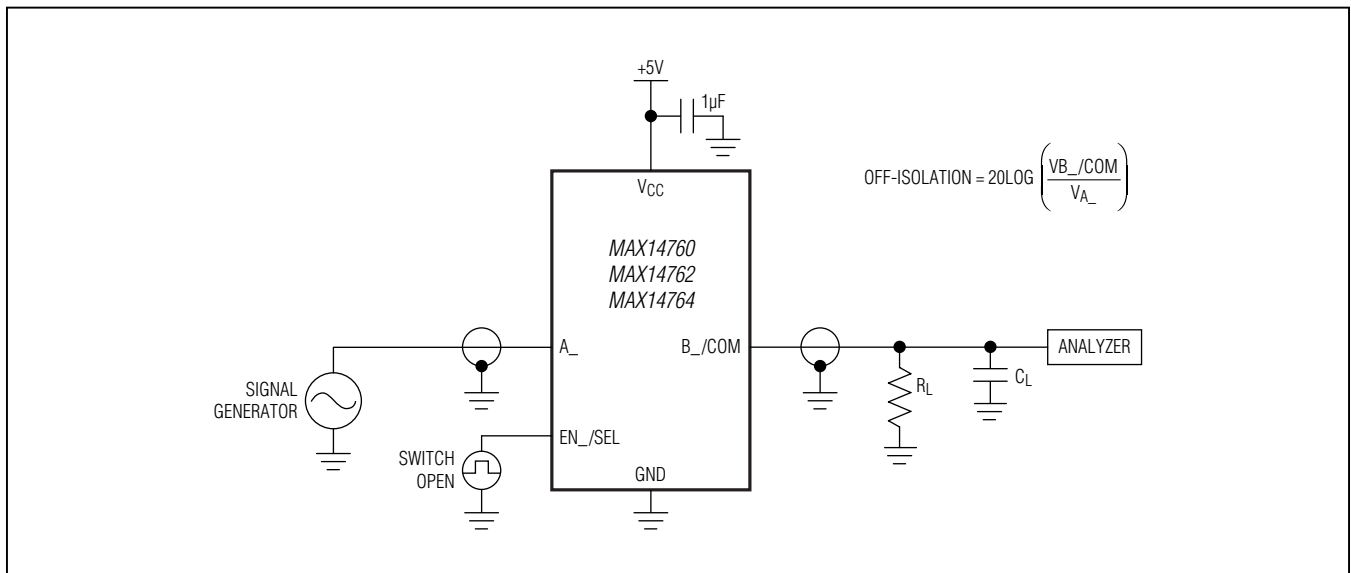


Figure 4. Off-Isolation

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Test Circuits/Timing Diagrams (continued)

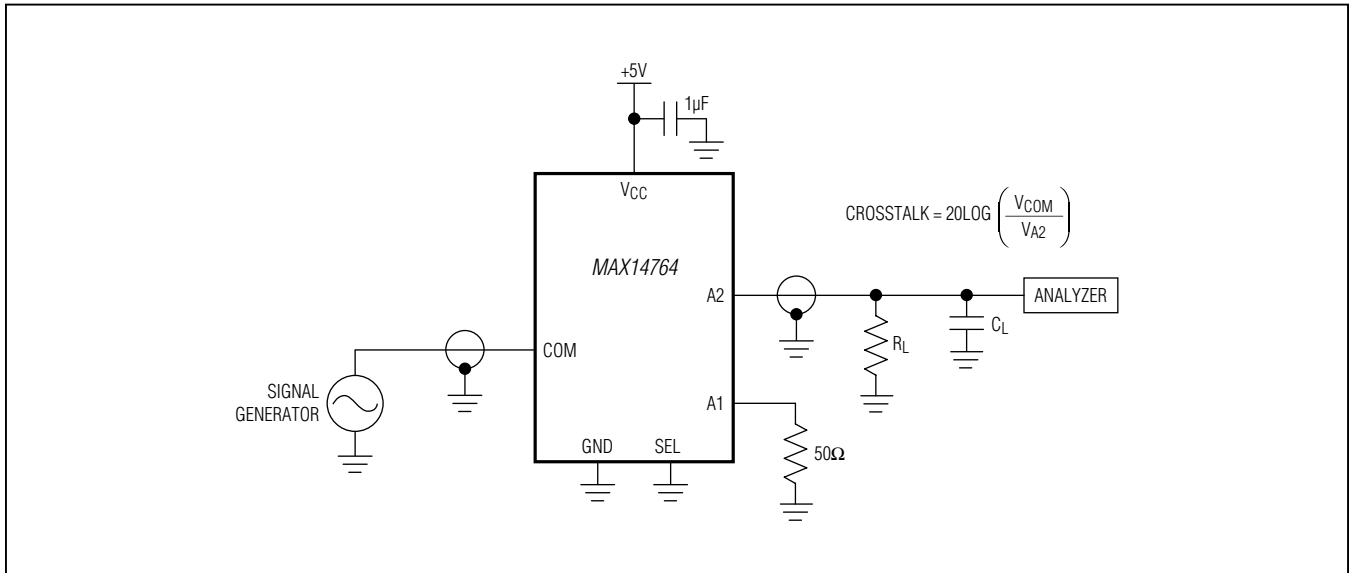


Figure 5. Crosstalk

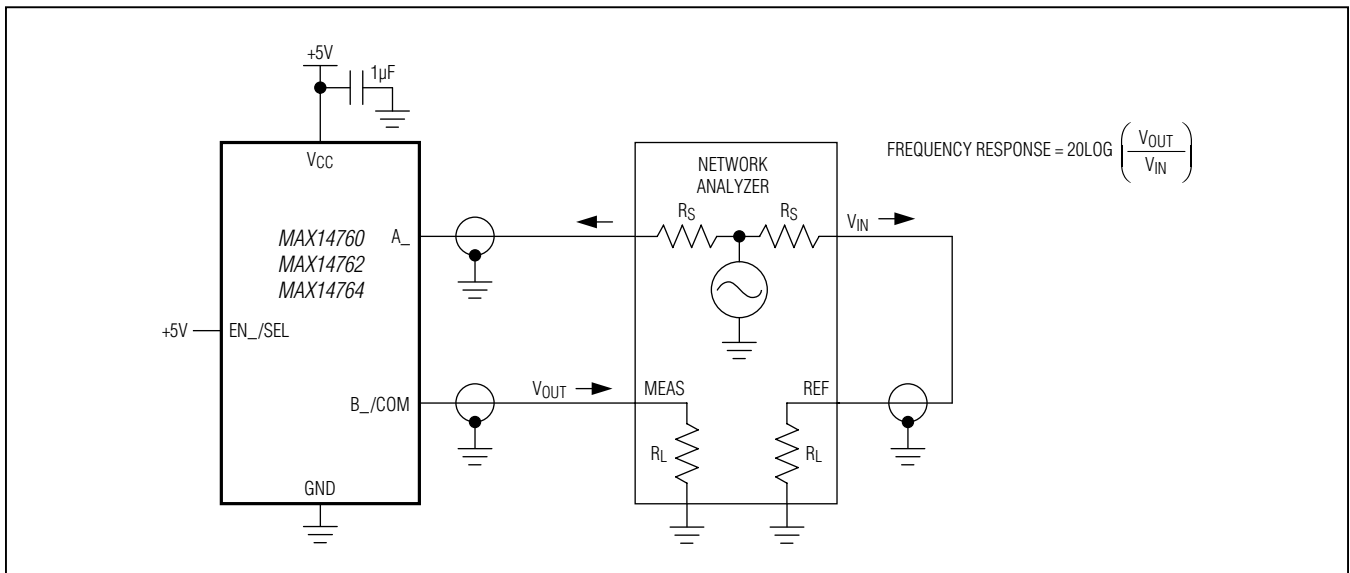


Figure 6. Insertion Loss

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Test Circuits/Timing Diagrams (continued)

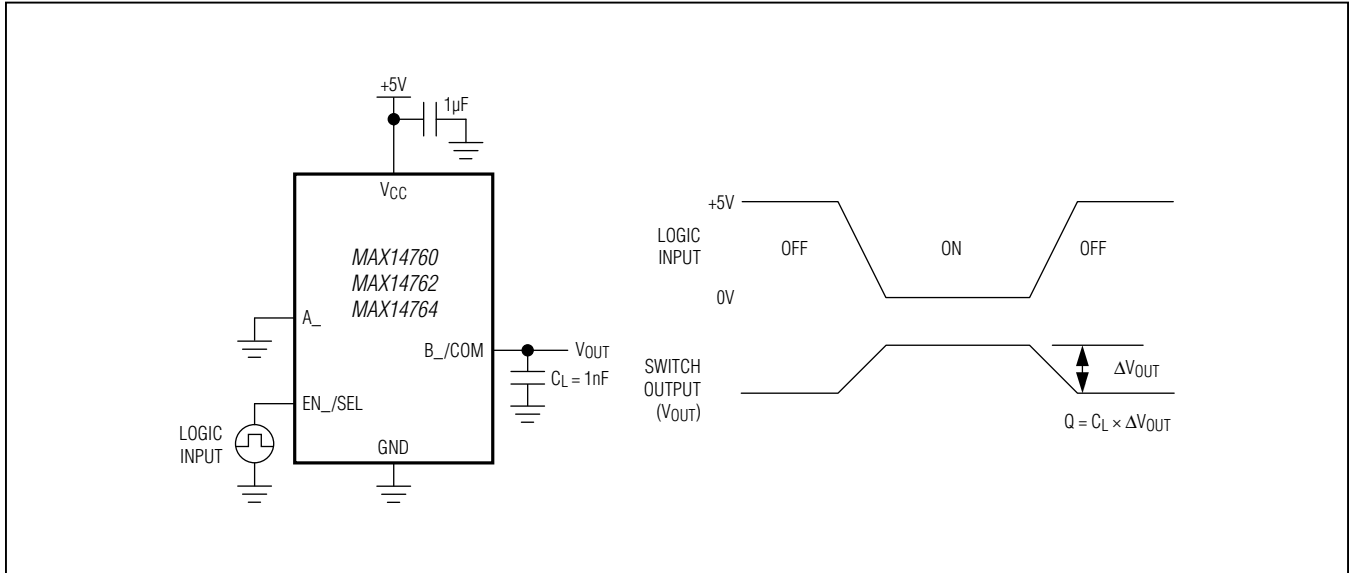
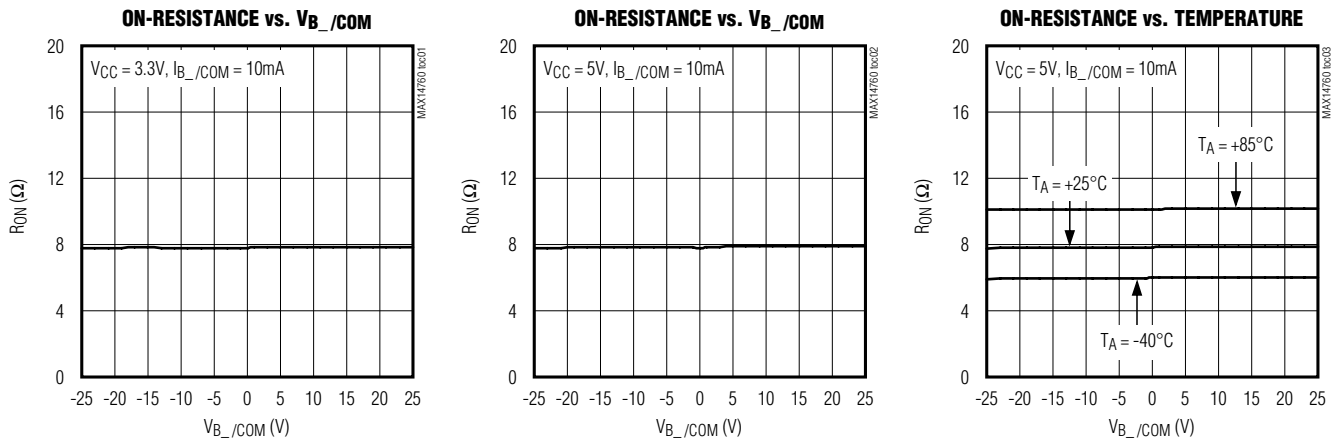


Figure 7. Charge Injection

Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

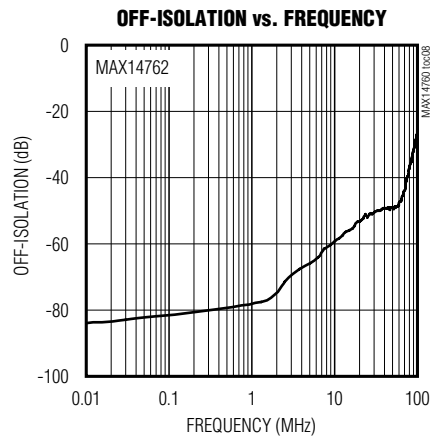
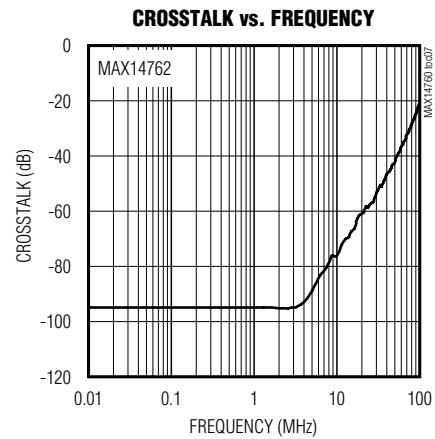
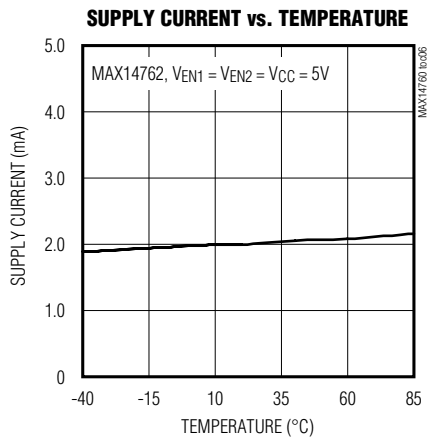
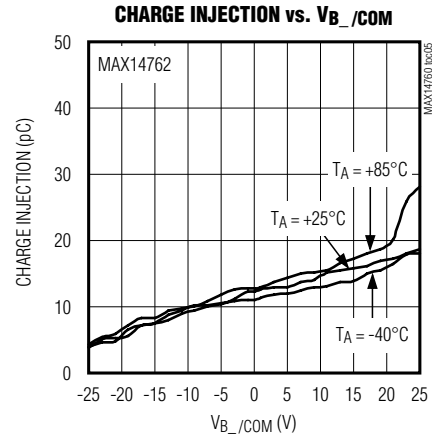
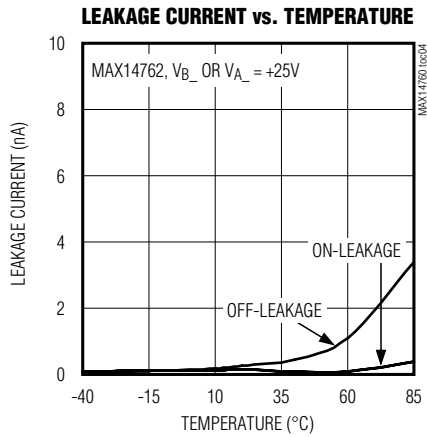


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Typical Operating Characteristics (continued)

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

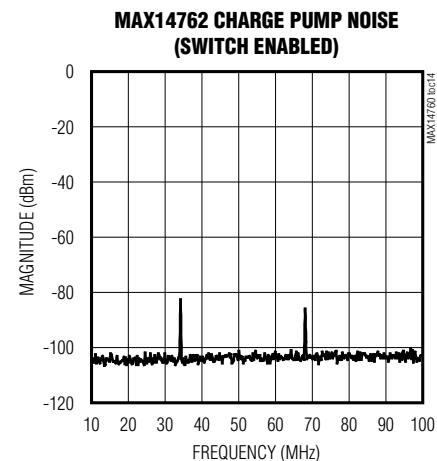
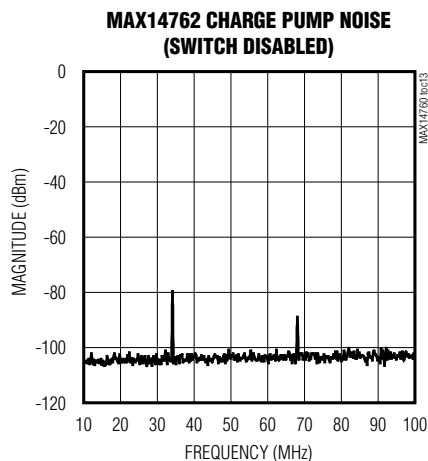
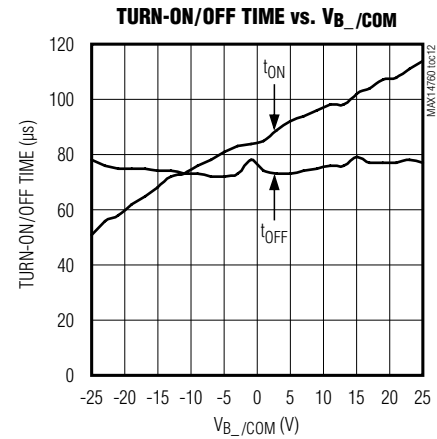
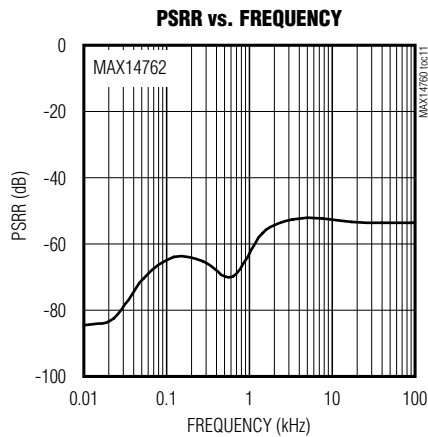
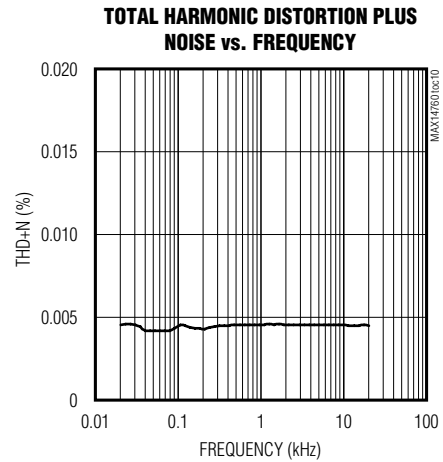
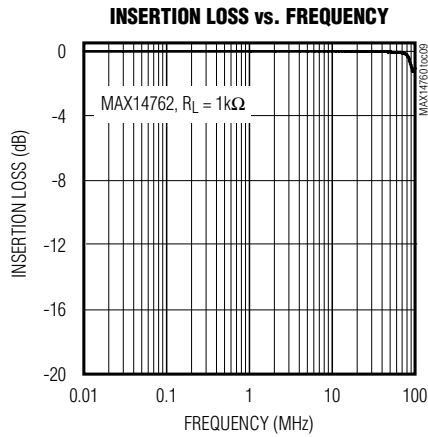


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Typical Operating Characteristics (continued)

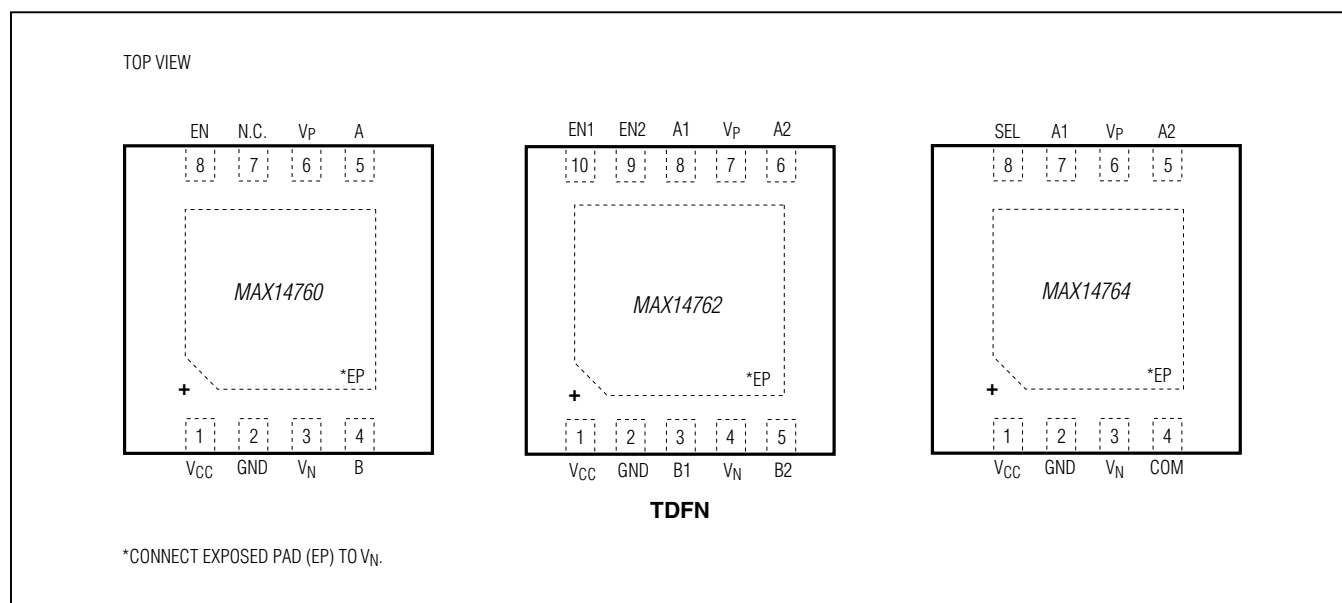
($T_A = +25^\circ\text{C}$, unless otherwise noted.)



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Pin Configurations



Pin Description

PIN			NAME	FUNCTION
MAX14760	MAX14762	MAX14764		
1	1	1	V_{CC}	Positive-Supply Voltage Input. Bypass V_{CC} to GND with a 1 μ F ceramic capacitor placed as close as possible to the device.
2	2	2	GND	Ground
3	4	3	V_N	Negative Voltage Output. Bypass V_N to GND with a 0.1 μ F 50V ceramic capacitor placed as close as possible to the device.
4	—	—	B	Analog Switch Common Terminal
—	—	4	COM	Analog Switch Common Terminal
5	—	—	A	Analog Switch Normally Open Terminal
6	7	6	V_P	Positive Voltage Output. Bypass V_P to GND with a 0.1 μ F 50V ceramic capacitor placed as close as possible to the device.
7	—	—	N.C.	No Connection. Leave unconnected.
8	—	—	EN	Switch Control Input. Drive EN high to close the switch or drive EN low to open the switch.
—	8	7	A1	Analog Switch 1 Normally Closed Terminal

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Pin Description (continued)

PIN			NAME	FUNCTION
MAX14760	MAX14762	MAX14764		
—	3	—	B1	Analog Switch 1 Common Terminal
—	6	5	A2	Analog Switch 2 Normally Open Terminal
—	5	—	B2	Analog Switch 2 Common Terminal
—	10	—	EN1	Switch 1 Control Input. Drive EN1 high to open switch 1 or drive EN1 low to close switch 1.
—	9	—	EN2	Switch 2 Control Input. Drive EN2 high to close switch 2 or drive EN2 low to open switch 2.
—	—	8	SEL	Switch Control Input. Drive SEL low to connect the COM terminal to A1 or drive SEL high to connect the COM terminal to A2.
—	—	—	EP	Exposed Pad. Connect EP to V_N ; EP is not intended as an electrical connection.

Detailed Description

The MAX14760/MAX14762/MAX14764 analog switches are capable of handling signals above and below their rails. These devices operate from a single +3.0V to +5.5V supply and support signals in the -25V to +25V range.

Integrated Bias Generation

The MAX14760/MAX14762/MAX14764 contain a total of three charge pumps to generate bias voltages for the internal switches: a 5V regulated charge pump, a positive high-voltage (+35V) charge pump, and a negative high-voltage (-27V) charge pump. When V_{DD} is above 4.7V (typ), the 5V regulated charge pump is bypassed, and V_{DD} provides the input for the high-voltage charge pumps, reducing overall supply current. An external 0.1 μ F capacitor is required for each high-voltage charge pump between V_P/V_N and GND.

Analog Signal Range

The devices switch signals in the range from -25V to +25V that are above and below their rails. The on-resistance for these devices exhibits a high degree of flatness (58m Ω) over the whole input voltage range of -25V to +25V. The analog switches allow bidirectional current flow, so A, A1, A2, B, B1, B2, and COM, can be used as either inputs or outputs.

Bypass Capacitors

Bias-stabilizing capacitors are required on the V_P and V_N pins. 1 μ F ceramic capacitors are suggested for effective operation. V_P and V_N are not intended as a power supply for other circuitry.

Applications Information

Nonpowered Condition

The MAX14760/MAX14762/MAX14764 can tolerate input voltages on the A, B, or COM pins in the ± 25 V range when it is not powered. When $V_{DD} = 0$ V, the DC input leakage current into the A, B, or COM pins is typically below 1 μ A. Some devices can have a larger leakage current up to the mA range due to technology spread.

With V_{DD} not powered, internal diodes between the analog pins and the V_P and V_N will charge up the external capacitors on V_P and V_N when positive and/or negative voltages are applied to these pins. This causes transient input current flow.

Large dv/dt on the inputs causes large capacitive charging currents, which have to be limited to 300mA to avoid destroying the internal diodes. Hence, the 100nF capacitors on V_P and V_N , the dv/dt must be limited to 3V/ μ s. Once the capacitors reach their final voltage the input current decays to the leakage current levels mentioned above.

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Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	FUNCTION	R _{ON} (MAX) (Ω)
MAX14760ETA+	-40°C to +85°C	8 TDFN-EP*	1 x SPST	20
MAX14762ETB+	-40°C to +85°C	10 TDFN-EP*	2 x SPST	20
MAX14764ETA+	-40°C to +85°C	8 TDFN-EP*	1 x SPDT	20

+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO
8 TDFN	T833+2	21-0137	90-0059
10 TDFN	T1033+1	21-0137	90-0003

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/11	Initial release	—
1	8/12	Updated <i>Electrical Characteristics</i> table, updated Figures 1–7, added TOCs 13 and 14, updated <i>Pin Configuration</i> table, added <i>Integrated Bias Generation</i> and <i>Nonpowered Condition</i> sections	3–7, 9–11

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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