3A, 23V, 340kHz Synchronous Step-Down Converter

General Description

The RT8293A is a high efficiency, monolithic synchronous step-down DC/DC converter that can deliver up to 3A output current from a 4.5V to 23V input supply. The RT8293A's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. The RT8293A also provides output under voltage protection and thermal shutdown protection. The low current (<3μA) shutdown mode provides output disconnection, enabling easy power management in battery-powered systems. The RT8293A is available in an SOP-8 (Exposed Pad) package.

Ordering Information

RT8293A □□□

- Package Type
  SP : SOP-8 (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)
- H : UVP Hiccup
  L : UVP Latch-Off

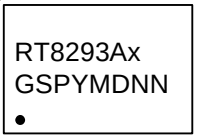
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

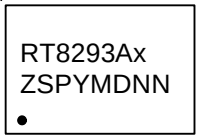
Marking Information

RT8293AxGSP



RT8293AxGSP : Product Number
x : H or L
YMDNN : Date Code

RT8293AxZSP



RT8293AxZSP : Product Number
x : H or L
YMDNN : Date Code

Features

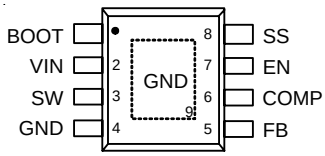
- **±1.5% High Accuracy Feedback Voltage**
- **4.5V to 23V Input Voltage Range**
- **3A Output Current**
- **Integrated N-MOSFET Switches**
- **Current Mode Control**
- **Fixed Frequency Operation : 340kHz**
- **Output Adjustable from 0.8V to 20V**
- **Up to 95% Efficiency**
- **Programmable Soft-Start**
- **Stable with Low-ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Over Current Protection**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Thermal Shutdown Protection**
- **RoHS Compliant and Halogen Free**

Applications

- Wireless AP/Router
- Set-Top-Box
- Industrial and Commercial Low Power Systems
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation of High-Performance DSPs

Pin Configurations

(TOP VIEW)



SOP-8 (Exposed Pad)

Typical Application Circuit

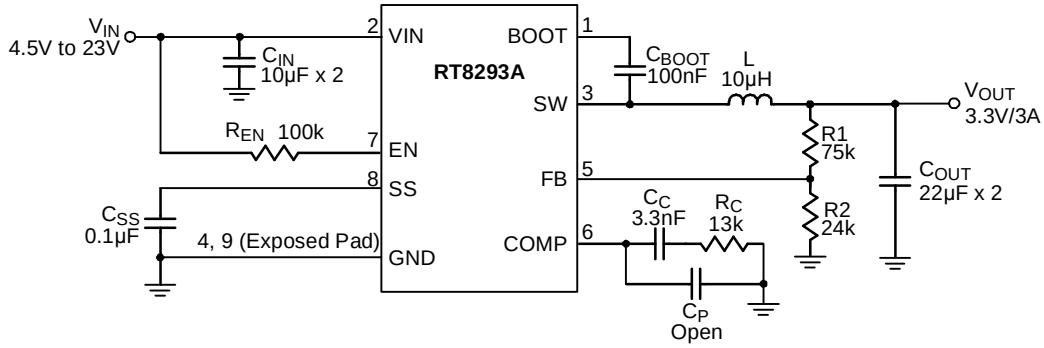


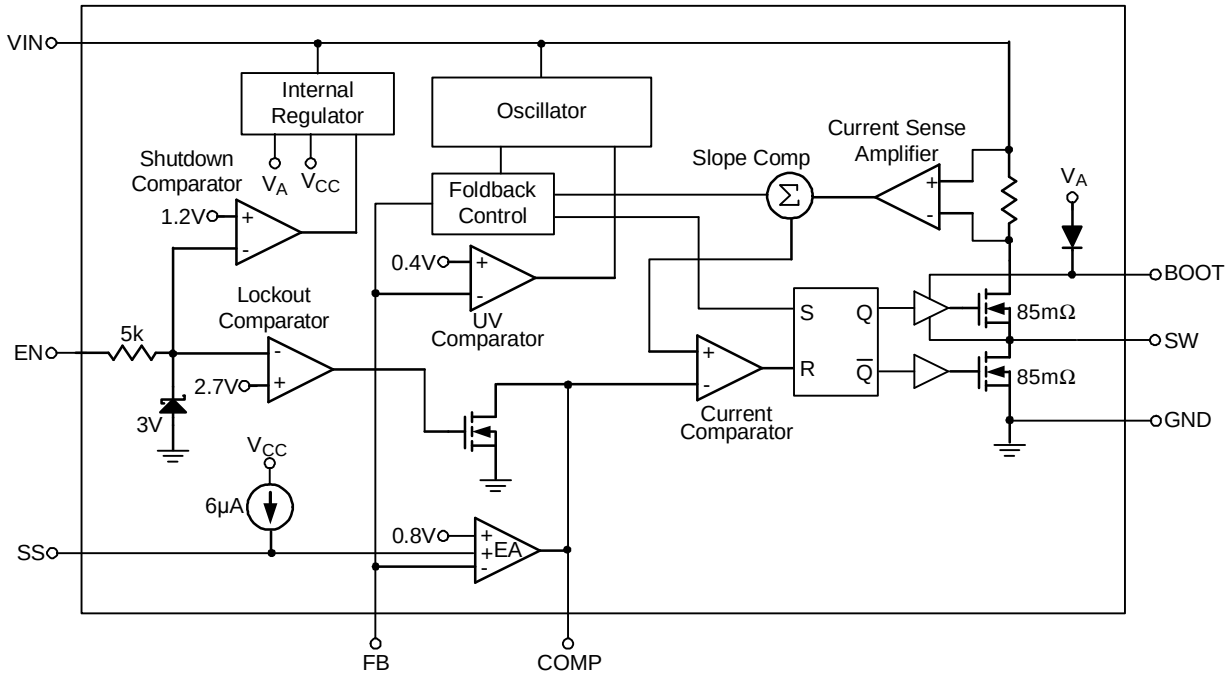
Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_C (kΩ)	C_C (nF)	L (µH)	C_{OUT} (µF)
8	27	3	33	3.3	22	22 x 2
5	62	11.8	20	3.3	15	22 x 2
3.3	75	24	13	3.3	10	22 x 2
2.5	25.5	12	9.1	3.3	6.8	22 x 2
1.5	10.5	12	5.6	3.3	3.6	22 x 2
1.2	12	24	4.3	3.3	3.6	22 x 2
1	3	12	3.6	3.3	2	22 x 2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap for high side gate driver. Connect a 0.1µF or greater ceramic capacitor from BOOT to SW pins.
2	VIN	Input Supply Voltage, 4.5V to 23V. Must bypass with a suitably large ceramic capacitor.
3	SW	Phase Node. Connect to external L-C filter.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	FB	Feedback Input pin. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via an internal resistive voltage divider. For an adjustable output, an external resistive voltage divider is connected to this pin.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input Pin. A logic high enables the converter; a logic low forces the RT8293A into shutdown mode reducing the supply current to less than 3µA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 13.5ms.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{IN} ---------- –0.3V to 25V
- Input Voltage, SW ---------- –0.3V to (V_{IN} + 0.3V)
- $V_{BOOT} – V_{SW}$ ---------- –0.3V to 6V
- Other Pins Voltage ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 4.5V to 23V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current		V_{EN} = 0V	--	0.5	3	µA
Supply Current		V_{EN} = 3 V, V_{FB} = 0.9V	--	0.8	1.2	mA
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 23V	0.788	0.8	0.812	V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ± 10µA	--	940	--	µA/V
High Side Switch On-Resistance	$R_{DS(ON)1}$		--	85	--	mΩ
Low Side Switch On-Resistance	$R_{DS(ON)2}$		--	85	--	mΩ
High Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V	--	0	10	µA
Upper Switch Current Limit		Min. Duty Cycle, $V_{BOOT} – V_{SW}$ = 4.8V	--	5.1	--	A
Lower Switch Current Limit		From Drain to Source	--	1.5	--	A
COMP to Current Sense Transconductance	G_{CS}		--	5.4	--	A/V
Oscillation Frequency	f_{OSC1}		300	340	380	kHz
Short Circuit Oscillation Frequency	f_{OSC2}	V_{FB} = 0V	--	100	--	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V	--	93	--	%
Minimum On Time	t_{ON}		--	100	--	ns

To be continued

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Threshold Voltage	Logic-High	V_{IH}		2.7	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	
Input Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	3.8	4.2	4.5	V
Input Under Voltage Lockout Threshold Hysteresis		ΔV_{UVLO}		--	320	--	mV
Soft-Start Current		I_{SS}	V_{SS} = 0V	--	6	--	μA
Soft-Start Period		t_{SS}	C_{SS} = 0.1μF	--	13.5	--	ms
Thermal Shutdown		T_{SD}		--	150	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

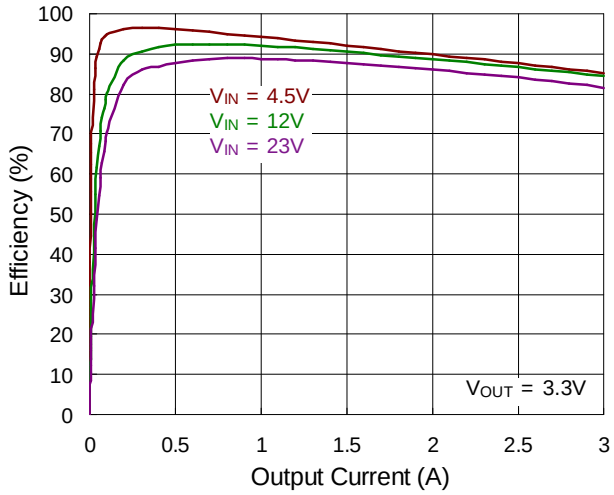
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

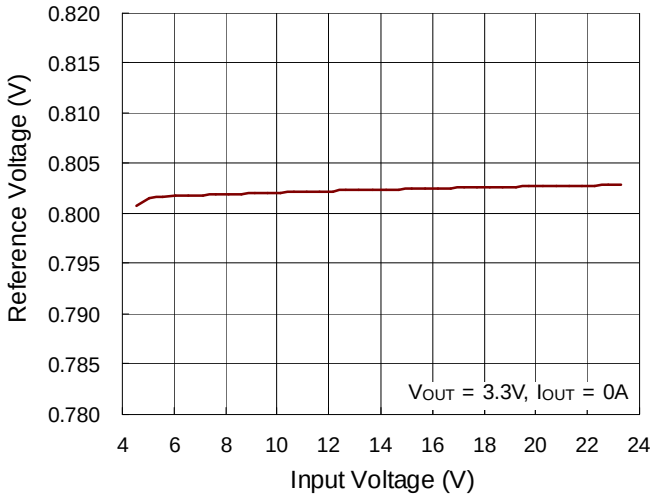
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

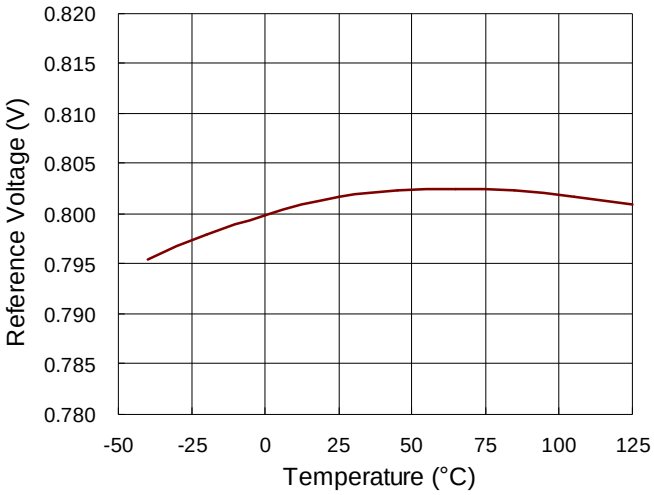
Efficiency vs. Output Current



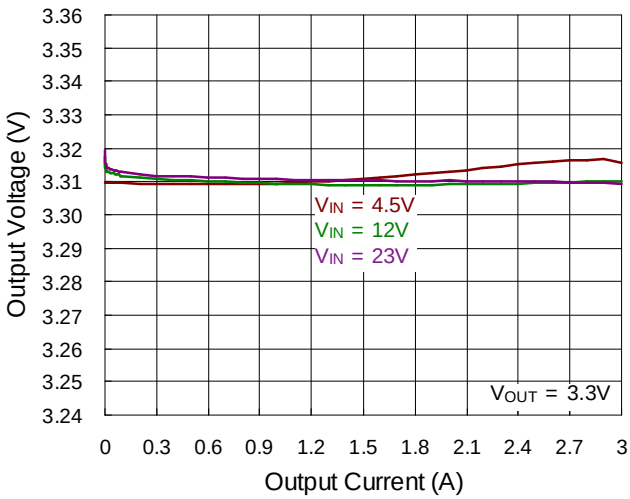
Reference Voltage vs. Input Voltage



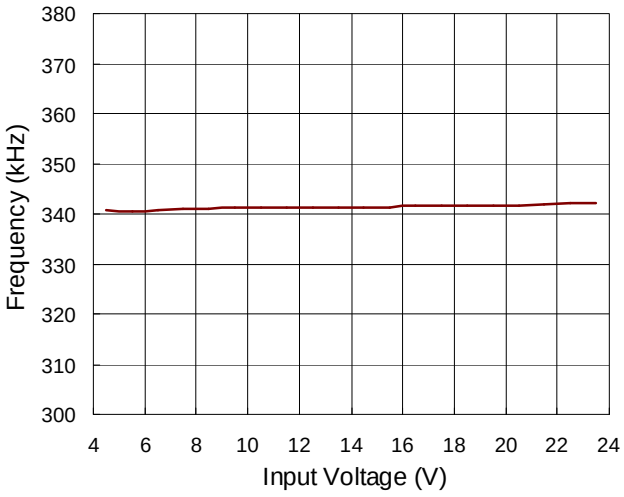
Reference Voltage vs. Temperature



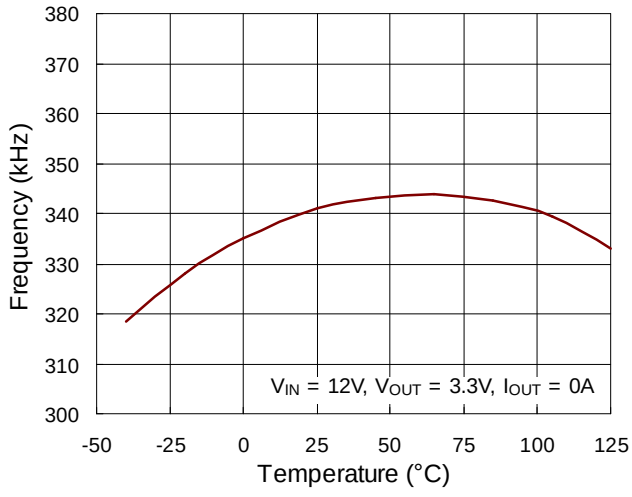
Output Voltage vs. Output Current



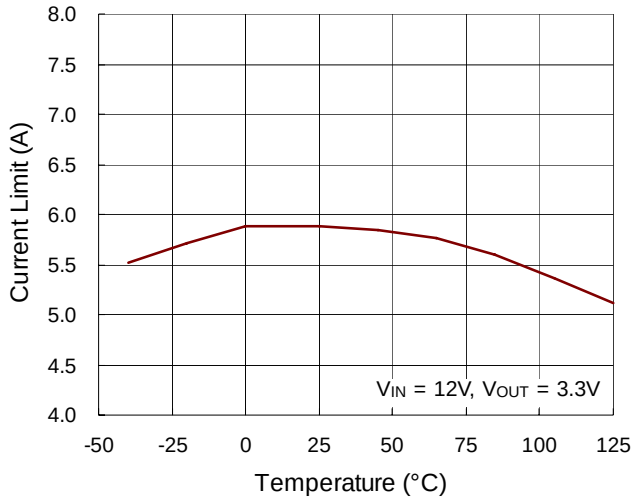
Frequency vs. Input Voltage



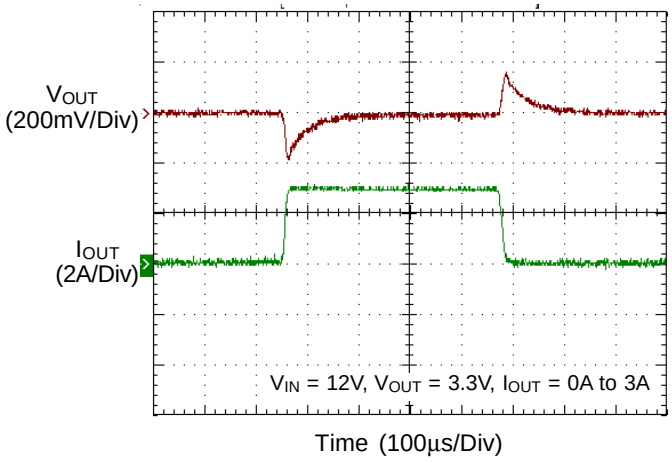
Frequency vs. Temperature



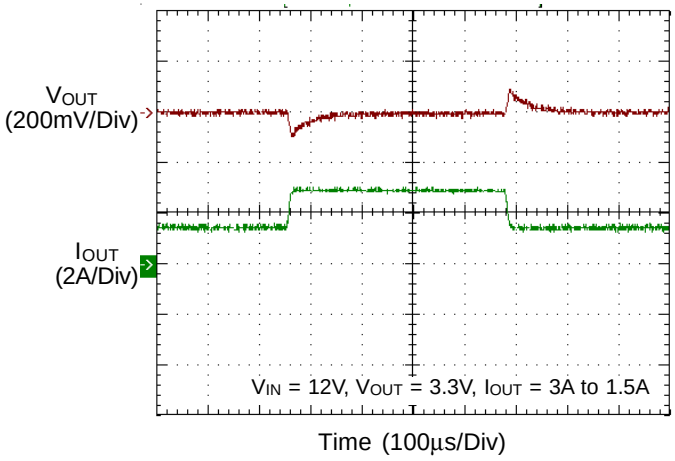
Current Limit vs. Temperature



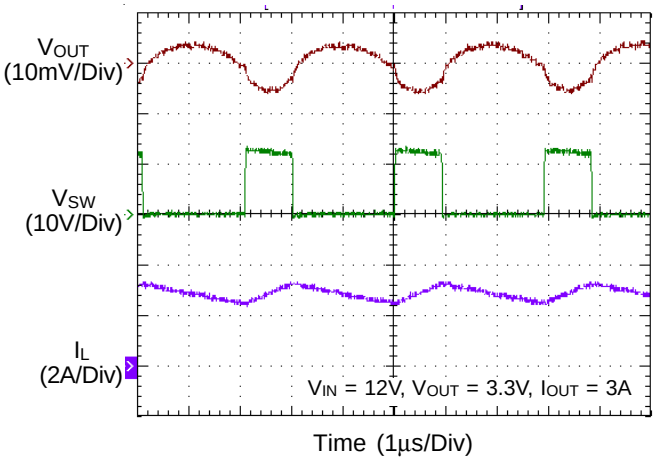
Load Transient Response



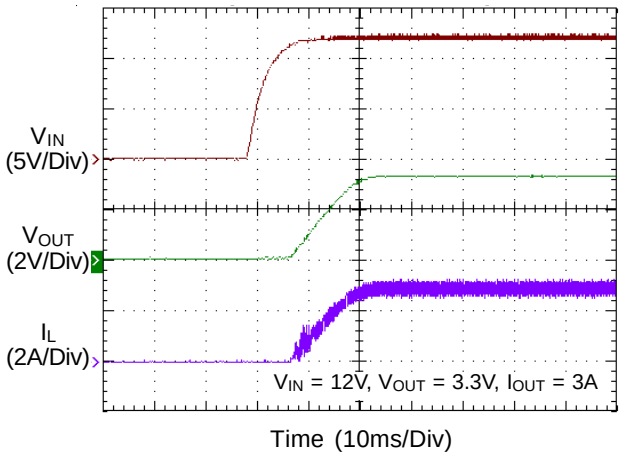
Load Transient Response



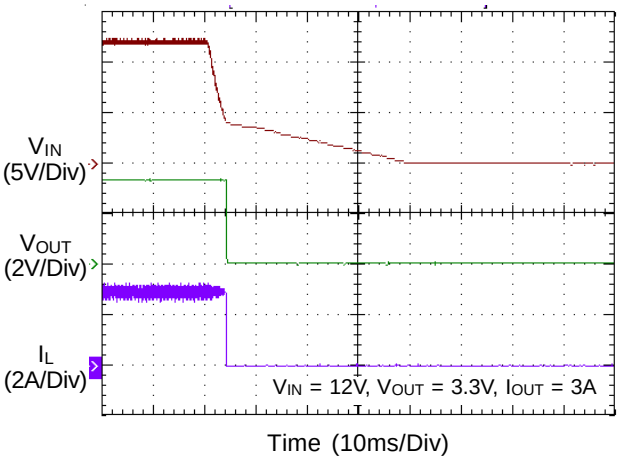
Switching



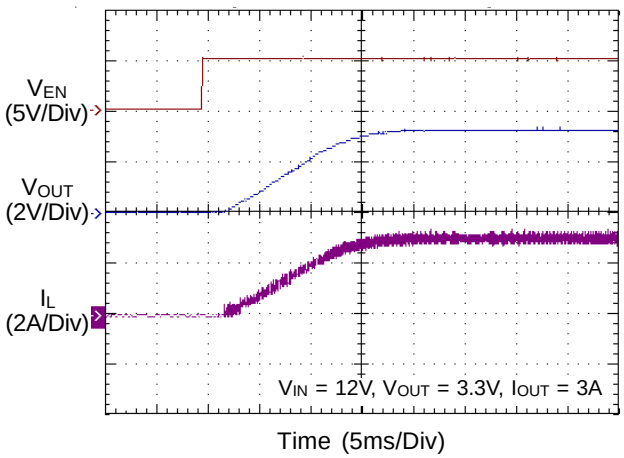
Power On from V_{IN}



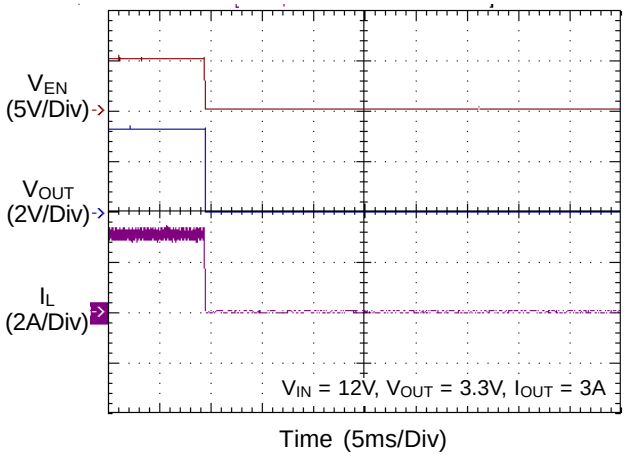
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

The RT8293A is a synchronous high voltage buck converter that can support the input voltage range from 4.5V to 23V and the output current can be up to 3A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

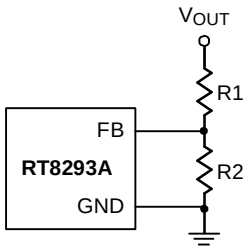


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT8293A. Note that the external boot voltage must be lower than 5.5V.

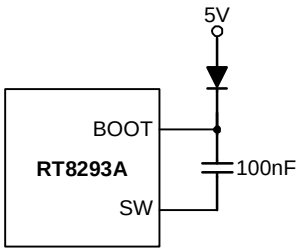


Figure 2. External Bootstrap Diode

Soft-Start

The RT8293A contains an external soft-start clamp that gradually raises the output voltage. The soft-start timing can be programmed by the external capacitor between SS pin and GND. The chip provides a 6μA charge current for the external capacitor. If 0.1μF capacitor is used to set the soft-start, the period will be 13.5ms(typ.).

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shut down the device. During shutdown mode, the RT8293A quiescent current drops to lower than 3μA. Driving the EN pin high (>2.7V, < 5.5V) will turn on the device again. For external timing control (e.g.RC), the EN pin can also be externally pulled high by adding a R_{EN}* resistor and C_{EN}* capacitor from the VIN pin (see Figure 5).

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 3. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

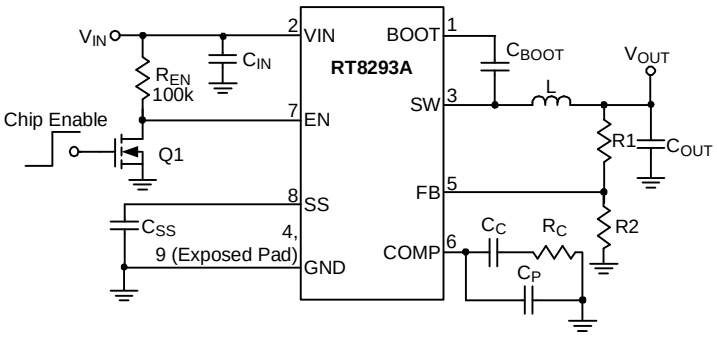


Figure 3. Enable Control Circuit for Logic Control with Low Voltage

To prevent enabling circuit when V_{IN} is smaller than the V_{OUT} target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 4. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor, R_{EN2}, can be selected to set input lockout threshold larger than 8V.

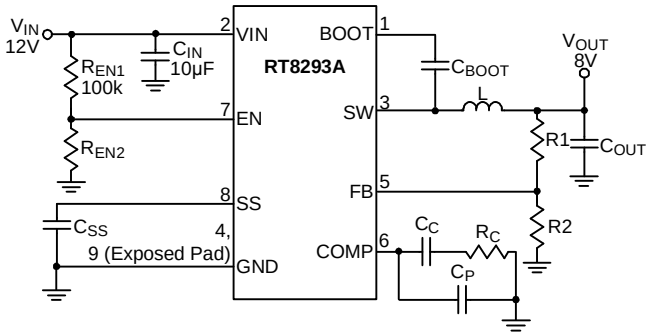


Figure 4. The Resistors can be Selected to Set IC Lockout Threshold

Under Voltage Protection

Hiccup Mode

For the RT8293AH, Hiccup Mode Under Voltage Protection (UVP) is provided. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the RT8293AH will shut down for a period of time and then recover automatically. The Hiccup Mode UVP can reduce input current in short-circuit conditions.

Latch-Off Mode

For the RT8293AL, Latch-Off Mode Under Voltage Protection (UVP) is provided. When the FB voltage drops below half of the feedback reference voltage, V_{FB}, UVP will be triggered and the RT8293AL will shutdown in Latch-Off Mode. In shutdown condition, the RT8293AL can be reset via the EN pin or power input VIN.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

C_{IN} and C_{OUT} Selection

The input capacitance, $C_{IN,}$ is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor,two 10µF low ESR ceramic capacitors are recommended. For the recommended capacitor, please refer to table 3 for more detail.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT} , is determined by :

$$\Delta V_{OUT} \le \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) and C_{OUT} also begins to be charged or discharged to generate a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One way is to by placing an R-C snubber between SW and GND and locating them as close as possible to the SW pin (see Figure 5). Another method is by adding a resistor in series with the bootstrap capacitor, C_{BOOT}, but this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section Layout Considerations.

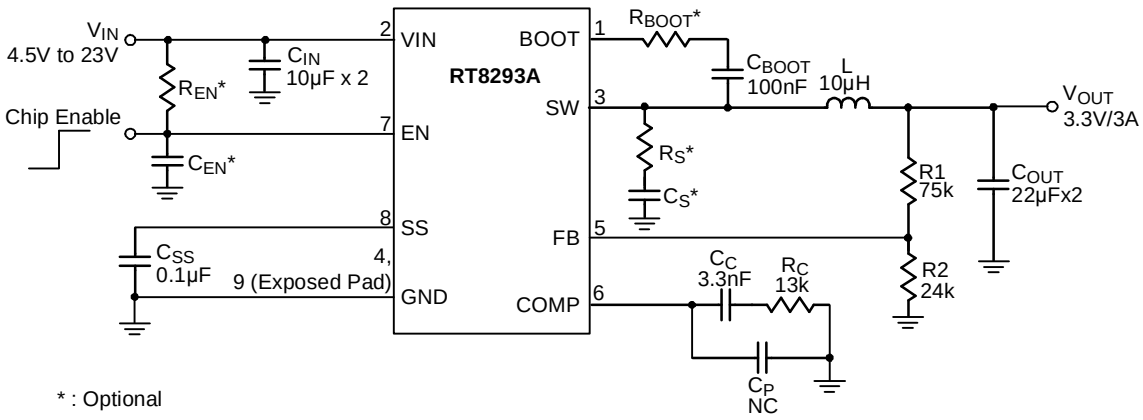


Figure 5. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT8293A, the maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance θ_{JA} is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W (min.copper area PCB layout)

$P_{D(MAX)}$ = (125°C – 25°C) / (49°C/W) = 2.04W ($70mm^2$copper area PCB layout)

The thermal resistance θ_{JA} of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance θ_{JA} can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 6, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 6.a), θ_{JA} is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 6.b) reduces the θ_{JA} to 64°C/W. Even further increasing the copper area of pad to $70mm^2$ (Figure 6.e) reduces the θ_{JA} to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT8293A packages, the derating curves in Figure 7 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

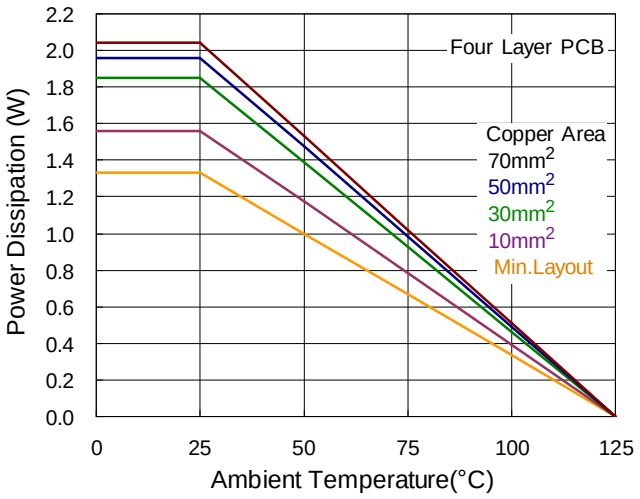
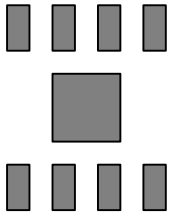
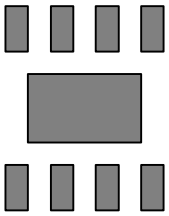


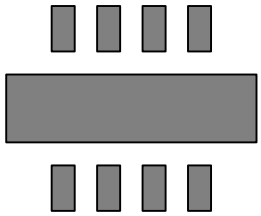
Figure 7. Derating Curves for RT8293A Package



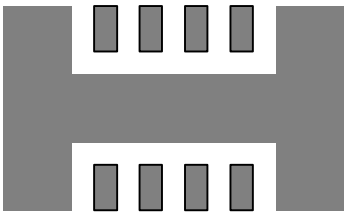
(a) Copper Area = (2.3 x 2.3) mm^2, θ_{JA} = 75°C/W



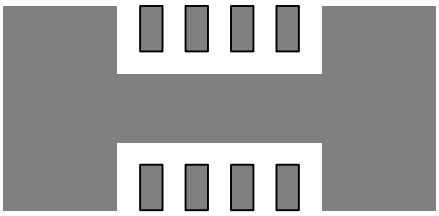
(b) Copper Area = $10mm^2$, θ_{JA} = 64°C/W



(c) Copper Area = $30mm^2$, θ_{JA} = 54°C/W



(d) Copper Area = 50mm^2, θ_{JA} = 51°C/W



(e) Copper Area = 70mm^2, θ_{JA} = 49°C/W

Figure 6. Themal Resistance vs. Copper Area Layout Design

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8293A.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8293A.
- Connect all analog grounds to a command node and then connect the command node to the power ground behind the output capacitors.
- An example of PCB layout guide is shown in Figure 8 for reference.

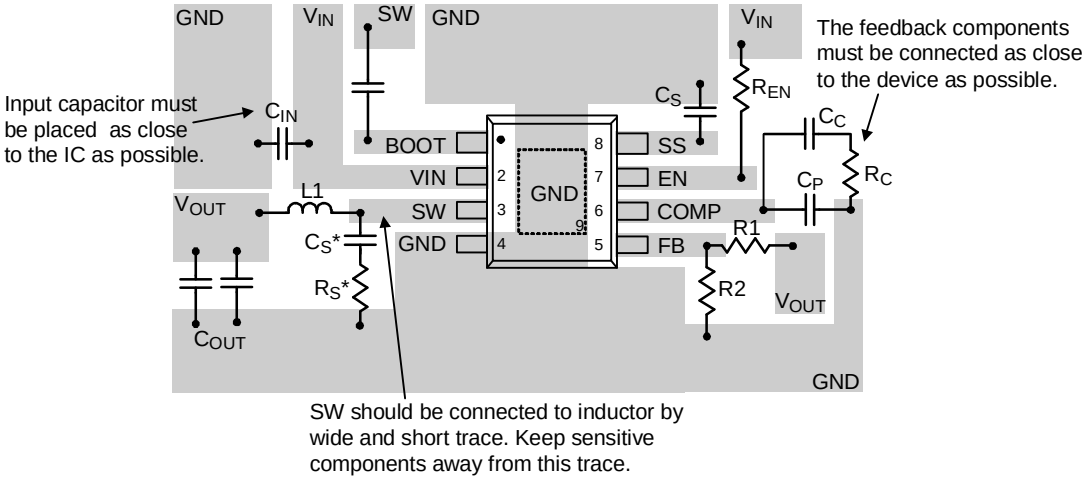
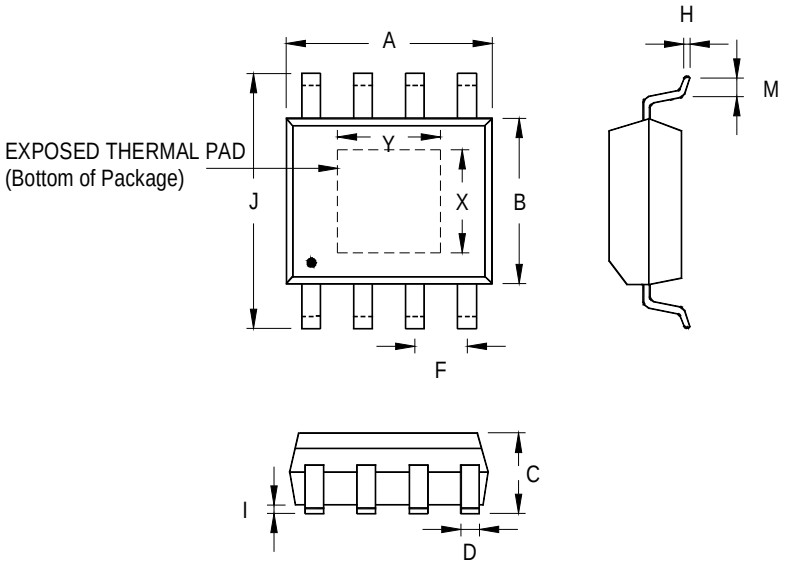


Figure 8. PCB Layout Guide

Table 3. Suggested Capacitors for C_{IN} and C_{OUT}

Location	Component Supplier	Part No.	Capacitance (mF)	Case Size
C_{IN}	MURATA	GRM31CR61E106K	10	1206
C_{IN}	TDK	C3225X5R1E106K	10	1206
C_{IN}	TAIYO YUDEN	TMK316BJ106ML	10	1206
C_{OUT}	MURATA	GRM31CR60J476M	47	1206
C_{OUT}	TDK	C3225X5R0J476M	47	1210
C_{OUT}	MURATA	GRM32ER71C226M	22	1210
C_{OUT}	TDK	C3225X5R1C22M	22	1210

Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

Richtek Technology Corporation

Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation

Taipei Office (Marketing)
5F, No. 95, Minchiuan Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)86672399 Fax: (8862)86672377
Email: marketing@richtek.com

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