



DCAN

Configurable CAN Bus Controller ver 1.01

OVERVIEW

The DCAN is a stand-alone controller for the Controller Area Network (CAN) widely used in automotive and industrial applications. DCAN conforms to Bosch CAN 2.0B specification (2.0B Active). Core has simple CPU interface (8/16/32 bit configurable data width) with little or big endian addressing scheme. Hardware message filtering and 64 byte receive FIFO enables back-to-back message reception with minimum CPU load. The DCAN is described at RTL level allowing target use in FPGA or ASIC technologies.

KEY FEATURES

- Conforms to Bosch CAN 2.0B Active
- 8/16/32-bit CPU slave interface with little or big endianess
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames.
- Data rate up to 1 Mbps
- Hardware message filtering (dual/single filter)
- 64 byte receive FIFO
- One transmit buffer
- No overload frames are generated
- Normal & Listen Only Mode
- Single Shot transmission
- Ability to abort transmission
- Readable error counters

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- Last Error Code
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

APPLICATIONS

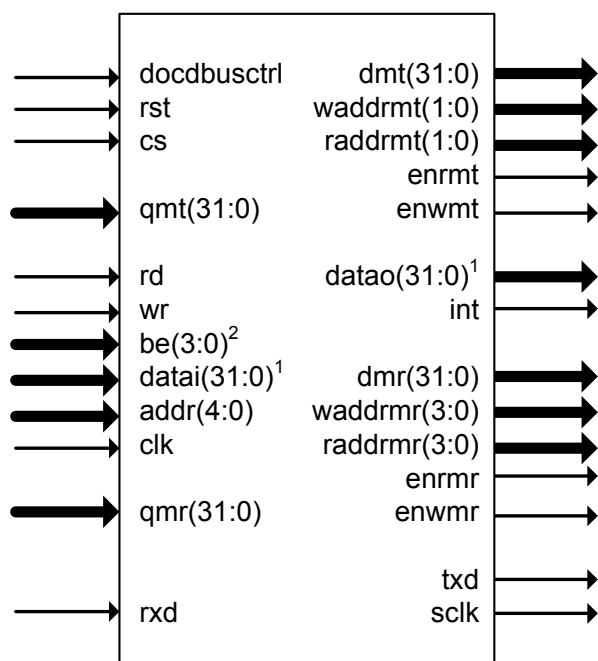
- Embedded communication systems
- Automotive, industrial
- Medical equipment

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code
- ◆ VHDL test bench environment
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

<http://www.DigitalCoreDesign.com>
<http://www.dcd.pl>

SYMBOL



1 – data bus can be configured as 8-, 16- or 32- bit depends on processor's bus size

2 – byte enable (be) size is set accordingly to data bus size

PINS DESCRIPTION

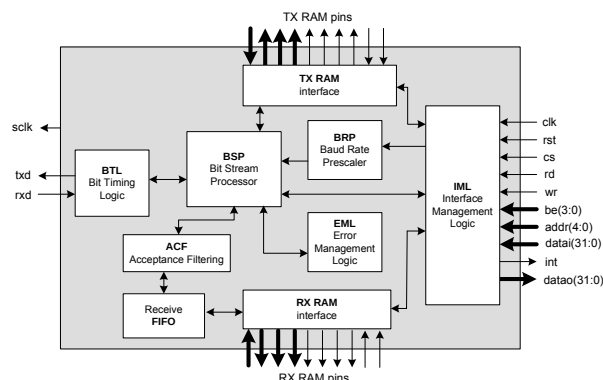
PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
cs	input	Chip select
rd	input	Read data strobe
wr	input	Write data strobe
addr(4:0)	input	Host address bus
be(3:0) ²	input	Host byte enable
dataai(31:0) ¹	input	Host output data bus
qmr(31:0)	input	RX DPRAM data output
qmt(31:0)	input	TX DPRAM data output
rxd	input	CAN receive data
docdbusctrl	input	DoCD debugger input
dataao(31:0) ¹	output	Host input data bus
int	output	Interrupt signal
dmr(31:0)	output	RX DPRAM data input
waddrmr(3:0)	output	RX DPRAM write address
raddrmr(3:0)	output	RX DPRAM read address
enrmr	output	RX DPRAM read enable
enwmr	output	RX DPRAM write enable
dmt(31:0)	output	TX DPRAM data input
waddrmt(1:0)	output	TX DPRAM write address
raddrmt(1:0)	output	TX DPRAM read address

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enrmt	output	TX DPRAM read enable
enwmt	output	TX DPRAM write enable
txd	output	CAN transmit data
sclk	output	SCLK clock output

BLOCK DIAGRAM

Figure below shows the DCAN IP Core block diagram.



Interface Management Logic (IML) – interprets commands from the CPU, provides interrupt and status indication.

Bit Stream Processor (BSP) – translates messages into frames and vice versa.

Baud Rate Prescaler (BRP) – defines the length of time quantum.

Bit Timing Logic (BTL) – processes the bit time, calculates position of the sample point and performs synchronization.

Error Management Logic (EML) – is responsible for fault confinement handling.

Acceptance Filter (ACF) – decides whether incoming messages are accepted or not based upon filter registers settings.

TX/RX RAM interfaces – interfaces to external dual port memories used by the DCAN core to store received and transmitted frames.

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PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F _{max}
CYCLONE	-6	1956 + 2 ESB	123 MHz
CYCLONE2	-6	1899 + 2 ESB	137 MHz
STRATIX	-5	1956 + 2 ESB	130 MHz
STRATIX2	-3	1956 + 2 ESB	188 MHz
STRATIXGX	-5	1956 + 2 ESB	131 MHz
MERCURY	-5	1956 + 2 ESB	138 MHz
EXCALIBUR	-1	1956 + 2 ESB	79 MHz
APEX2A	-7	1956 + 2 ESB	108 MHz
APEX20KC	-7	1956 + 2 ESB	94 MHz
APEX20KE	-1	1956 + 2 ESB	83 MHz
APEX20K	-1	1956 + 2 ESB	66 MHz
ACEX1K	-1	1956 + 2 ESB	66 MHz
FLEX10KE	-1	1956 + 2 ESB	66 MHz

8-bit CPU Core performance in ALTERA® devices

Device	Speed grade	Logic Cells	F _{max}
CYCLONE	-6	1967 + 2 ESB	124 MHz
CYCLONE2	-6	1890 + 2 ESB	135 MHz
STRATIX	-5	1967 + 2 ESB	131 MHz
STRATIX2	-3	1523 + 2 ESB	187 MHz
STRATIXGX	-5	1967 + 2 ESB	132 MHz
MERCURY	-5	1967 + 2 ESB	141 MHz
EXCALIBUR	-1	1967 + 2 ESB	79 MHz
APEX2A	-7	1967 + 2 ESB	113 MHz
APEX20KC	-7	1967 + 2 ESB	95 MHz
APEX20KE	-1	1937 + 2 ESB	78 MHz
APEX20K	-1	1967 + 2 ESB	68 MHz
ACEX1K	-1	1967 + 2 ESB	63 MHz
FLEX10KE	-1	1967 + 2 ESB	63 MHz

16-bit Core performance in ALTERA® devices

Device	Speed grade	Logic Cells	F _{max}
CYCLONE	-6	1931 + 2 ESB	123 MHz
CYCLONE2	-6	1879 + 2 ESB	136 MHz
STRATIX	-5	1931 + 2 ESB	134 MHz
STRATIX2	-3	1510 + 2 ESB	185 MHz
STRATIXGX	-5	1931 + 2 ESB	130 MHz
MERCURY	-5	1931 + 2 ESB	143 MHz
EXCALIBUR	-1	1931 + 2 ESB	84 MHz
APEX2A	-7	1931 + 2 ESB	110 MHz
APEX20KC	-7	1931 + 2 ESB	94 MHz
APEX20KE	-1	1931 + 2 ESB	83 MHz
APEX20K	-1	1931 + 2 ESB	66 MHz
ACEX1K	-1	1931 + 2 ESB	66 MHz
FLEX10KE	-1	1931 + 2 ESB	66 MHz

32-bit Core performance in ALTERA® devices

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