Low-Voltage, Low r_{ON}, Dual SPST Analog Switch

DESCRIPTION

The DG2037/2038/2039 are dual single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, fast switching, low on-resistance ($r_{DS(on)}$: 3.0 Ω at 2.7 V) and small physical size, the DG2037/2038/2039 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2037/2038/2039 are built on Vishay Siliconix's new high density low voltage process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 3.0 Ω
- Fast Switching - 12 ns
- Low Charge Injection - Q_{INJ}: 10 pC
- Low Power Consumption
- TTL/CMOS Compatible
- SOT23-8 and MSOP-8 Packages

BENEFITS

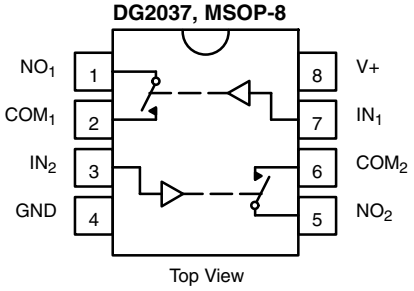
- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG2037

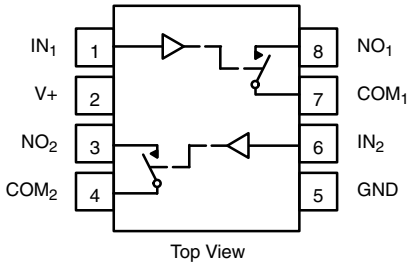
DG2037, MSOP-8



Top View

Device Marking: 2037

DG2037. SOT23-8



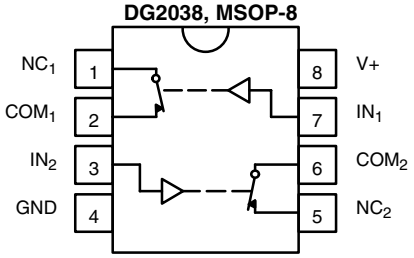
Top View

Device Marking: E0

TRUTH TABLE - DG2037	
Logic	**Switch**
0	Off
1	On

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION - DG2038/DG2039

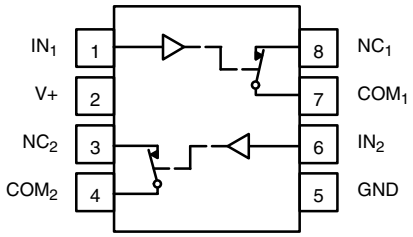
DG2038, MSOP-8



Top View

Device Marking: 2038

DG2038. SOT23-8

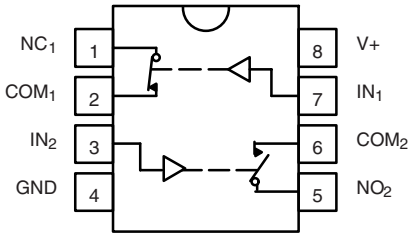


Top View

Device Marking: F1

TRUTH TABLE - DG2038	
Logic	**Switch**
0	On
1	Off

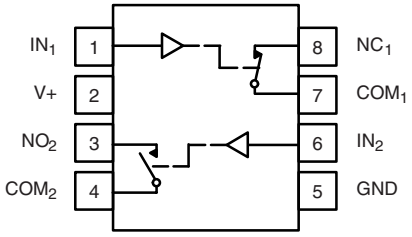
DG2039, MSOP-8



Top View

Device Marking: 2039

DG2039. SOT23-8



Top View

Device Marking: F2

TRUTH TABLE - DG2039		
Logic	**Switch-1**	**Switch-2**
0	On	Off
1	Off	On

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	MSOP-8	DG2037DQ
		DG2038DQ
		DG2039DQ
	SOT23-8	DG2037DS
		DG2038DS
		DG2039DS

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Referenced V+ to GND		- 0.3 to 6.0	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	MSOP-8[c]	320	mW
	SOT23-8[c]	515	

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 25 °C.

SPECIFICATIONS (V+ = 3.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.4 or 1.5 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 1.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		3	6 7	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.5 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.5		
r_{ON} Match[d]	r_{ON} Match	V+ = 2.7 V, V_D = 1.5 to V+, I_D = 10 mA	Room		0.3		
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.5			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}	f = 1 MHz	Full		8		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF Figures 1 and 2	Room Full		22	35 40	ns
Turn-Off Time	t_{OFF}		Room Full		17	31 35	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk[d]	X_{TALK}		Room		- 67		
Source-Off Capacitance[d]	$C_{NC/NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		17		pF
Drain-Off Capacitance[d]	$C_{COM(off)}$		Room		19		
Channel-On Capacitance[d]	C_{ON}		Room		35		
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.02	1.0	µA
Power Consumption	P_C					3.3	µW

SPECIFICATIONS (V+ = 5.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	Limits - 40 to 85 °C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 4.5 V, V_{COM} = 2.5 V, I_{NO}, I_{NC} = 10 mA	Room Full		2.5 1.6	5 6	Ω
r_{ON} Flatness[d]	r_{ON} Flatness	V+ = 4.5 V, V_{COM} = 2.5 to V+, I_{NO}, I_{NC} = 10 mA	Room		0.4		Ω
r_{ON} Match[d]	r_{ON} Match	V+ = 4.5 V, I_D = 10 mA, V_{COM} = 2.5 V	Room		0.2		Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	nA
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	- 1 - 10		1 10	nA
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	V
Input Capacitance	C_{in}	f = 1 MHz	Full		8		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF Figures 1 and 2	Room Full		19	30 35	ns
Turn-Off Time[d]	t_{OFF}		Room Full		12	22 30	ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, Figure 3	Room		1		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 61		dB
Crosstalk[d]	X_{TALK}		Room		- 67		dB
Source-Off Capacitance[d]	$C_{NC/NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		15		pF
Drain-Off Capacitance[d]	$C_{COM(off)}$		Room		17		pF
Channel-On Capacitance[d]	C_{ON}		Room		35		pF
Power Supply							
Power Supply Range	V+			4.5		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.02	1.0	µA
Power Consumption	P_C					5.5	µW

Notes:

a. Room = 25 °C, Full = as determined by the operating suffix.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Typical values are for design aid only, not guaranteed nor subject to production testing.

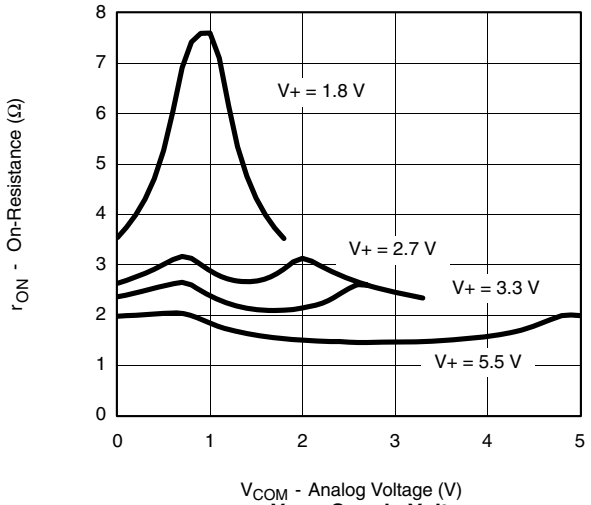
d. Guarantee by design, nor subjected to production test.

e. V_{IN} = input voltage to perform proper function.

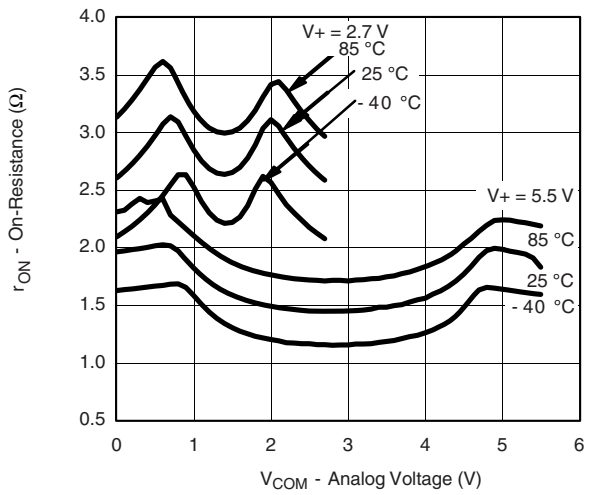
f. Not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

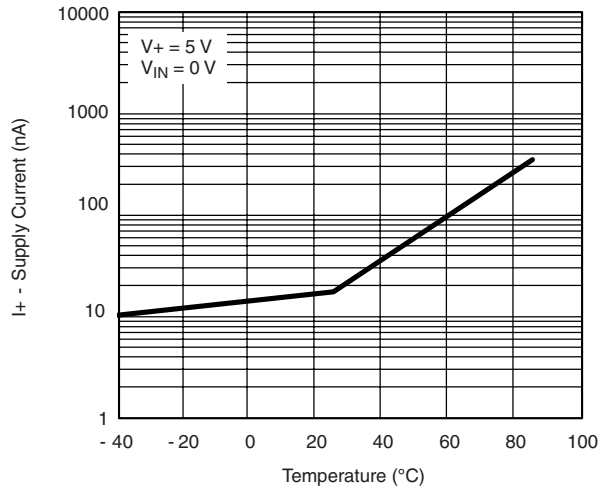
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



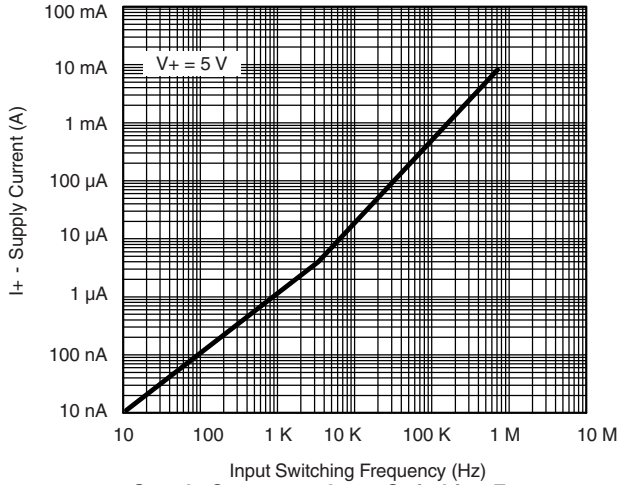
r_{ON} vs. V_{COM} Supply Voltage



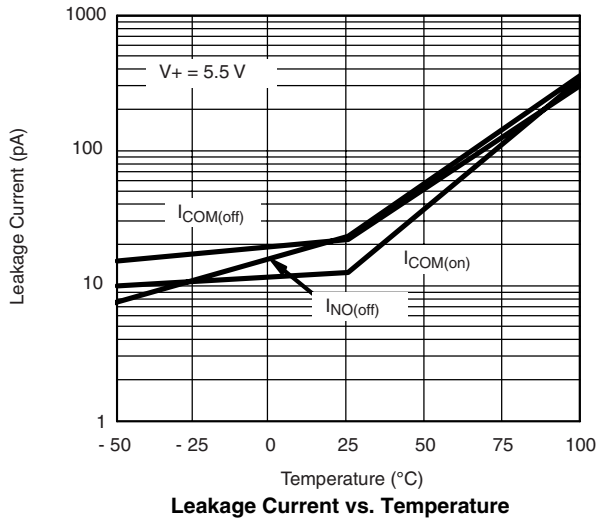
r_{ON} vs. Analog Voltage and Temperature



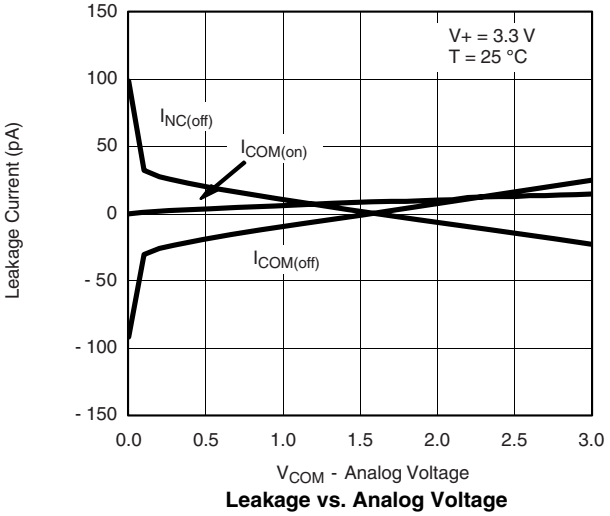
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

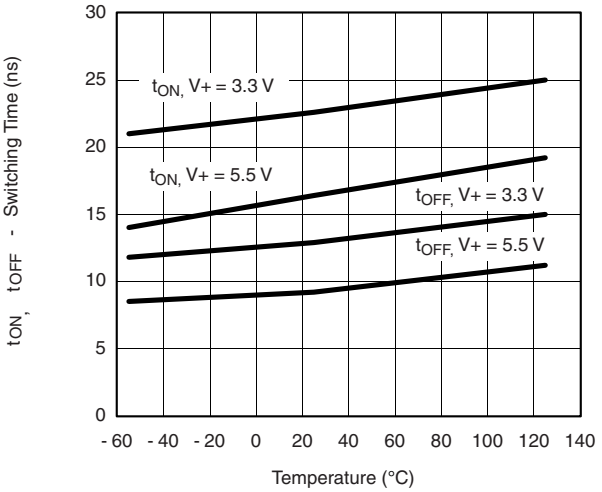


Leakage Current vs. Temperature

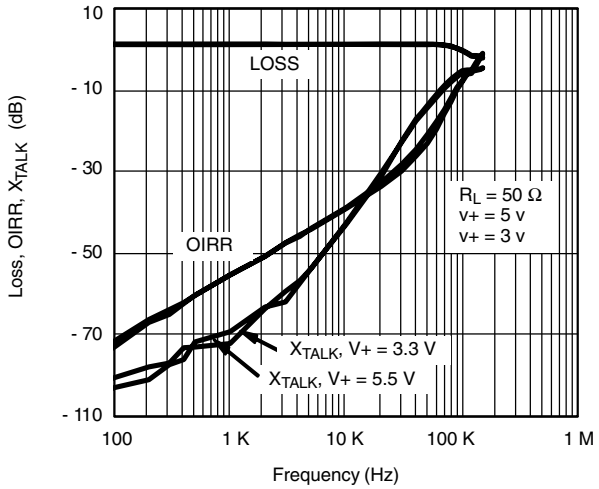


Leakage vs. Analog Voltage

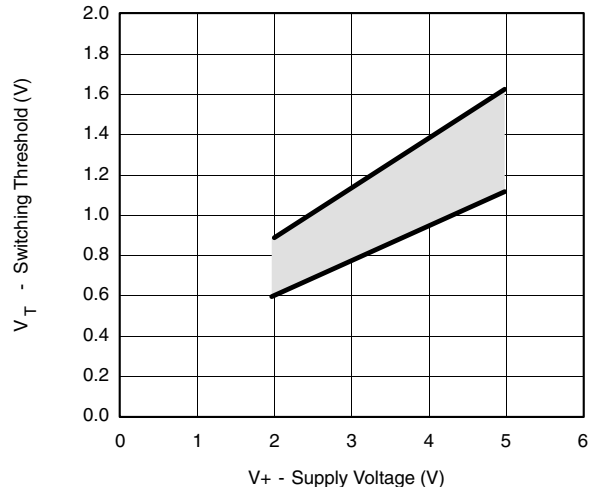
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



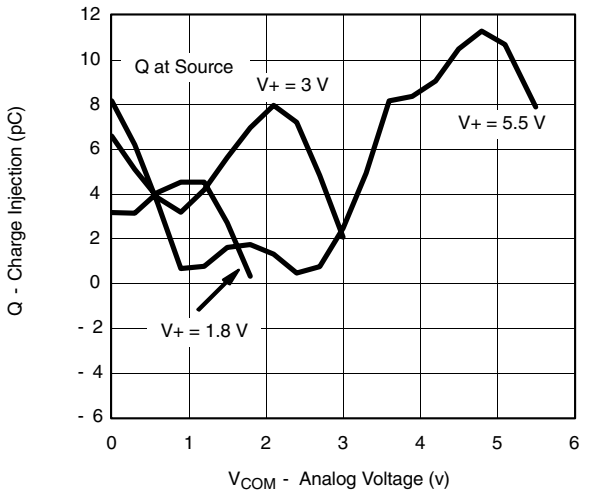
Switching Time vs. Temperature and Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

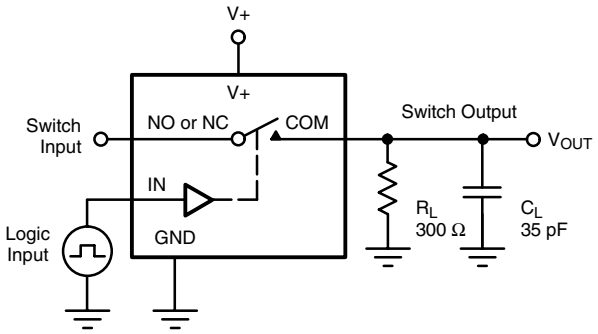


Switching Threshold vs. Supply Voltage



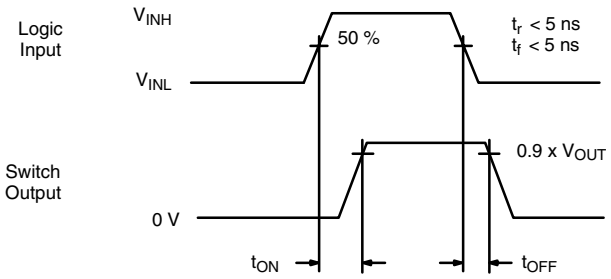
Charge Injection vs. Analog Voltage

TEST CIRCUITS



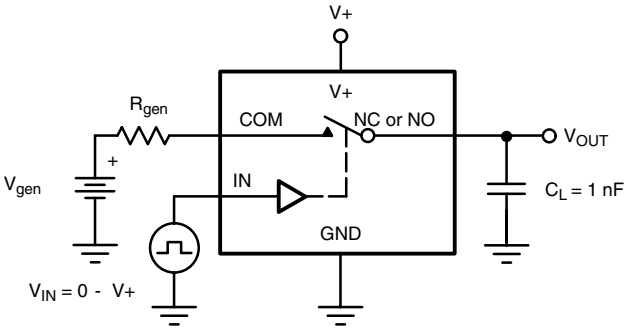
C_L (includes fixture and stray capacitance)

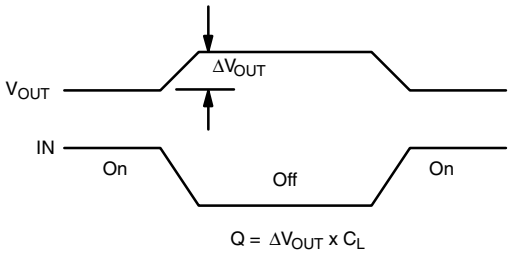
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection

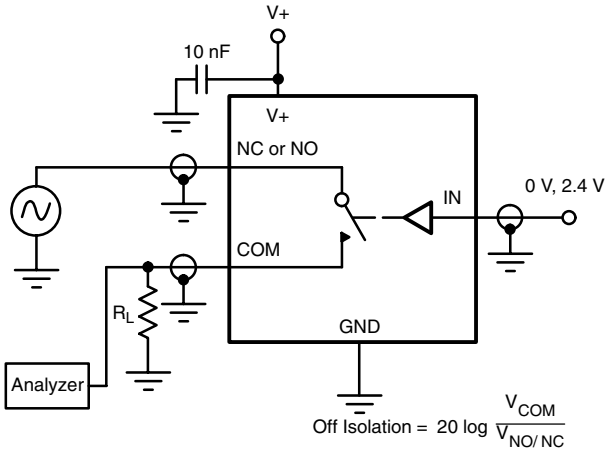


Figure 3. Off-Isolation

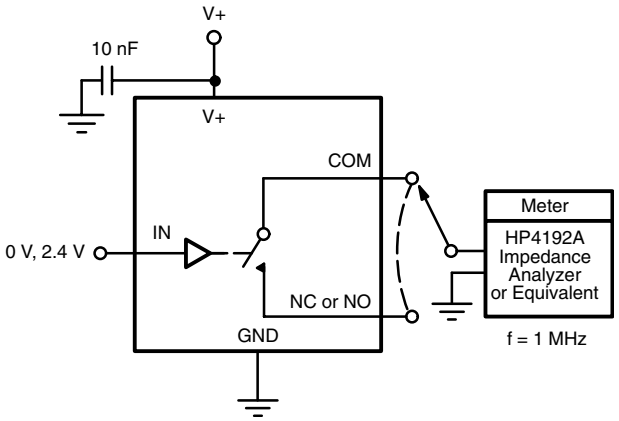


Figure 4. Channel Off/On Capacitance

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