Ordering number : EN5792B

SANYO Semiconductors
DATA SHEET

LB1991V — Monolithic Digital IC For Fan Motor 3-phase Brushless Motor Driver

Overview

The LB1991V is a 3-phase brushless motor driver IC that is optimal for driving the DC fan motor.

Functions

- 3-phase full-wave voltage drive technique (120° voltage-linear technique)
- Torque ripple correction circuit (overlap correction)
- Speed control technique based on motor voltage and current control
- Built-in FG comparators
- Built-in thermal shutdown circuit

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		10	V
	$V_{CC}2$ max		11	V
	V_S max		11	V
Applied output voltage	V_O max		V_S+2	V
Maximum output current	I_O max		1.0	A
Allowable power dissipation	Pd max	Independent IC	440	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$	$V_{CC}1 \leq V_{CC}2$	2.7 to 6.0	V
	$V_{CC}2$		3.5 to 9.0	V
	V_S		Up to $V_{CC}2$	V
Hall input amplitude	V_{HALL}	Between Hall effect element inputs	±20 to ±80	mVp-p

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Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 3V, $V_{CC}2$ = 4.75V, V_S = 1.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply Current						
$V_{CC}1$ current drain	$I_{CC}1$	I_{OUT} = 100mA		3	5	mA
$V_{CC}2$ current drain	$I_{CC}2$	I_{OUT} = 100mA		7.0	10.0	mA
$V_{CC}1$ quiescent current	$I_{CC}1Q$	V_{STBY} = 0V		1.5	3.0	mA
$V_{CC}2$ quiescent current	$I_{CC}2Q$	V_{STBY} = 0V			100	μA
V_S quiescent current	I_SQ	V_{STBY} = 0V		75	100	μA
VX1						
High side residual voltage	$V_{XH}1$	I_{OUT} = 0.2A	0.15	0.22	0.29	V
Low side residual voltage	$V_{XL}1$	I_{OUT} = 0.2A	0.15	0.20	0.25	V
VX2						
High side residual voltage	$V_{XH}2$	I_{OUT} = 0.5A		0.25	0.40	V
Low side residual voltage	$V_{XL}2$	I_{OUT} = 0.5A		0.25	0.40	V
Output saturation voltage	V_O(sat)	I_{OUT} = 0.8A, Sink + Source			1.4	V
Overlap	O.L	R_L = 39Ω × 3, Rangle = 20kΩ *2	72	80	87	%
High/low overlap difference	ΔO.L	(Average upper side overlap) – (Average lower side overlap) *2	-8		+8	%
Hall Amplifiers						
Input offset voltage	V_{HOFF}	Design target *1	-5		+5	mV
Common-mode input voltage range	V_{HCM}	Rangle = 20kΩ	0.95		2.1	V
I/O voltage gain	V_{GVH}	Rangle = 20kΩ	25.5	28.5	31.5	dB
Standby Pin						
High-level voltage	V_{STH}		2.5			V
Low-level voltage	V_{STL}				0.4	V
Input current	I_{STIN}	V_{STBY} = 3V		25	40	μA
Leakage current	I_{STLK}	V_{STBY} = 0V			-30	μA
FRC Pin						
High-level voltage	V_{FRCH}		2.5			V
Low-level voltage	V_{FRCL}				0.4	V
Input current	I_{FRCIN}	V_{FRC} = 3V		25	30	μA
Leakage current	I_{FRCLK}	V_{FRC} = 0V			-30	μA
VH						
Hall supply voltage	V_{HALL}	I_H = 5mA, VH(+) – VH(–)	0.85	0.95	1.05	V
(–) pin voltage	V_H(–)	I_H = 5mA	0.81	0.88	0.95	V
FG Comparator						
Input offset voltage	V_{FGOFF}		-3		+3	mV
Input bias voltage	I_{bFG}	$V_{FGIN}^+ = V_{FGIN}^-$ = 1.5V			500	nA
Input bias current offset	ΔI_{bFG}	$V_{FGIN}^+ = V_{FGIN}^-$ = 1.5V	-100		+100	nA
Common-mode input voltage range	V_{FGCM}		1.2		2.5	V
Output high-level voltage	V_{FGOH}	At the internal pull-up resistors	2.8			V
Output low-level voltage	V_{FGOL}	At the internal pull-up resistors			0.2	V
Voltage gain	V_{GFG}	Design target *1		100		dB
Output current (sink)	I_{FGOS}	For the output pin low level			5	mA
Thermal shutdown						
Operating temperature	TSD	Design target *1		180		°C
Temperature hysteresis	ΔTSD	Design target *1		20		°C

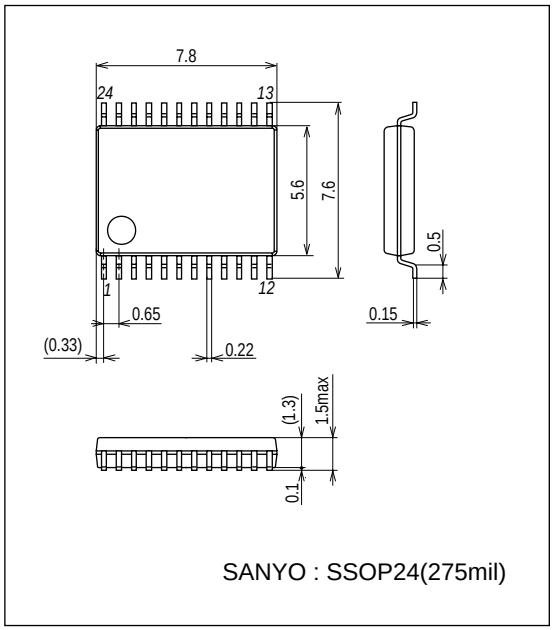
*1: Design target values in the conditions column are not tested.

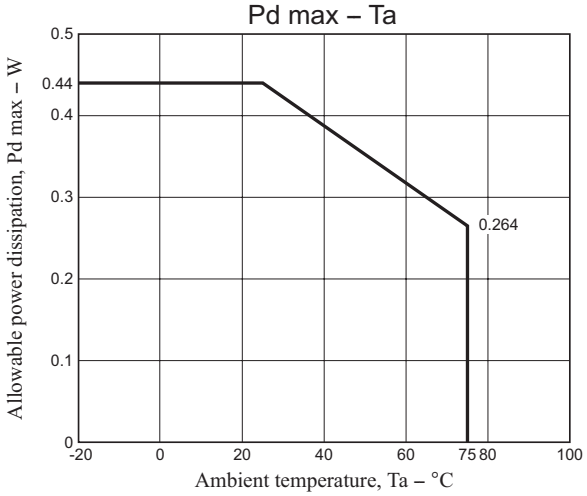
*2: The standard for overlap is the value as measured.

Package Dimensions

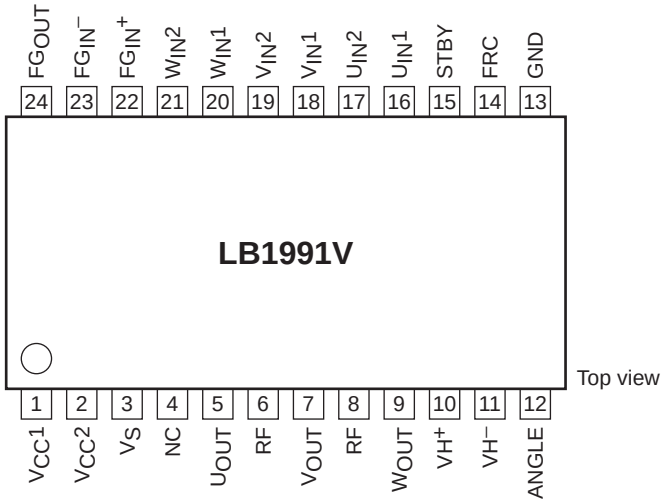
unit : mm (typ)

3175C





Pin Assignment

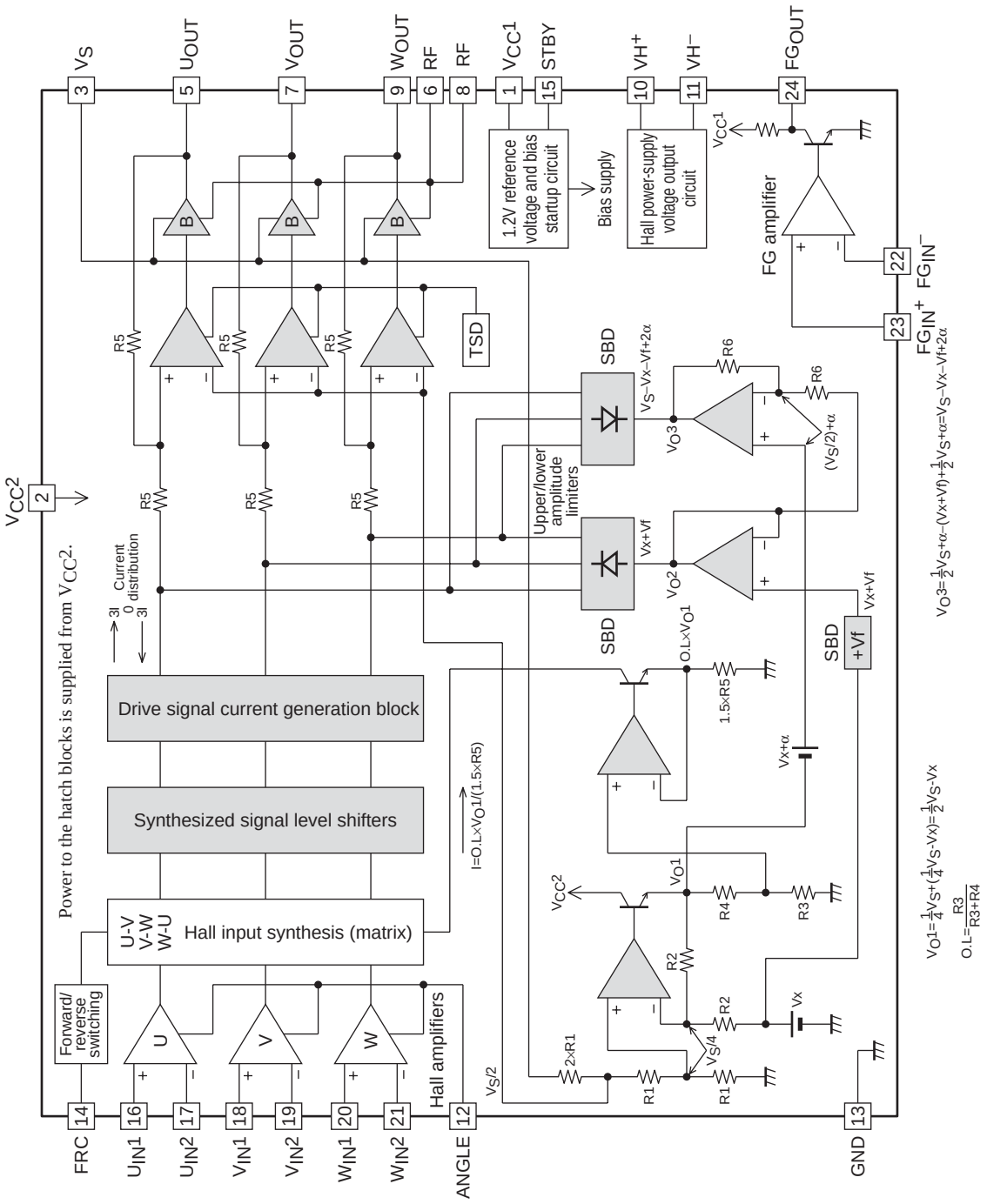


Truth Table

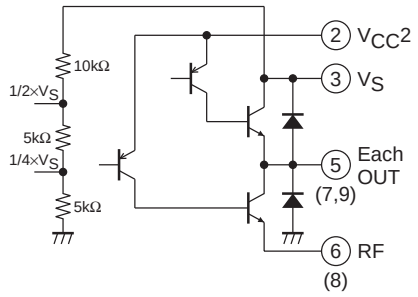
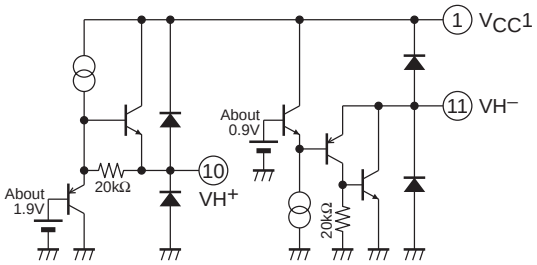
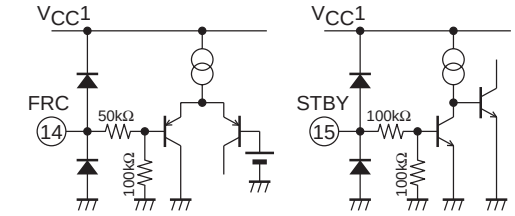
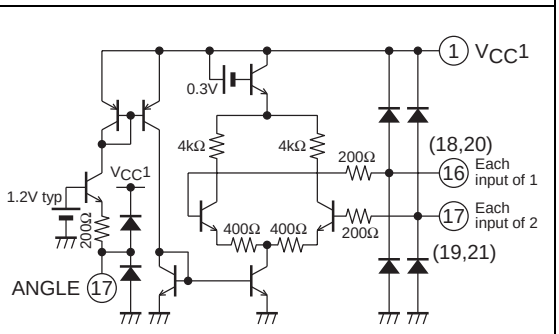
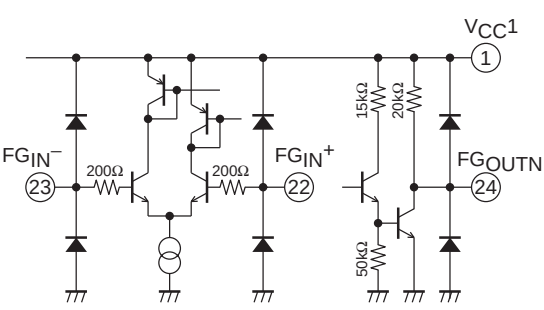
	Source phase → Sink phase	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note: The “H” entries in the FRC column indicate a voltage of 2.50V or higher, and the “L” entries indicate a voltage of 0.4V or lower. (When $V_{CC}1$ is 3V.)
At the Hall inputs, for each phase a high-level input is the state where the (+) input is 0.02V or higher than the (–) input. Similarly, a low-level input is the state where the (+) input is 0.02V or lower than the (–) input.

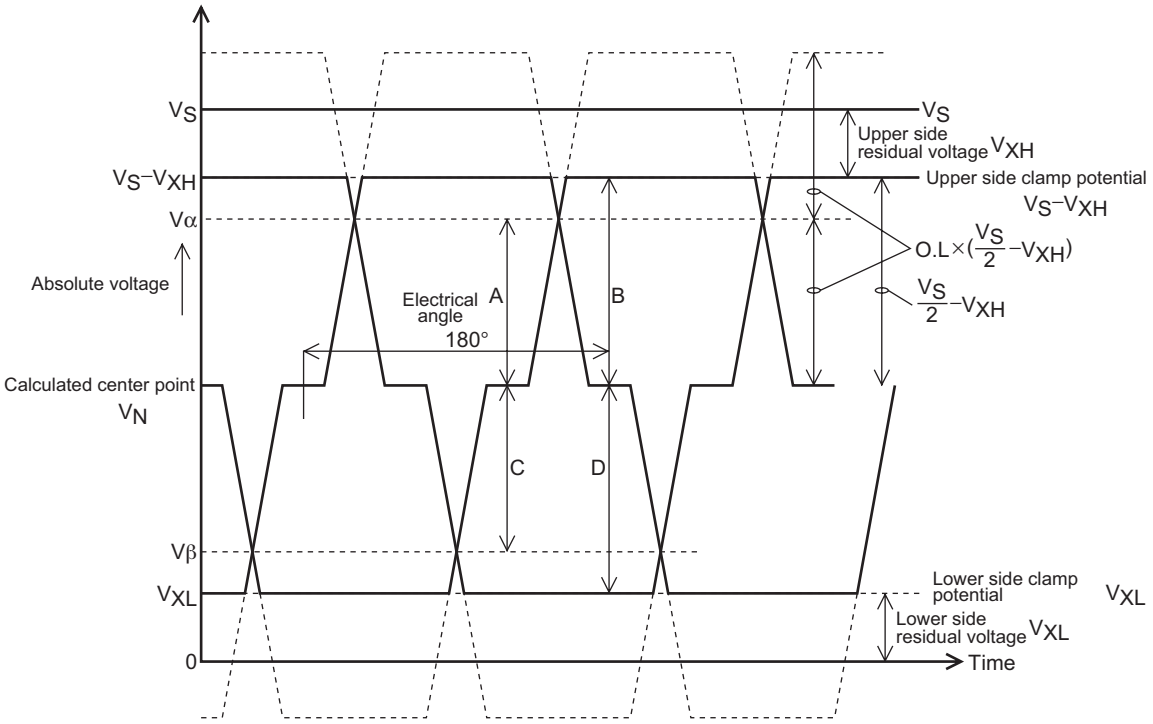
Block Diagram



Pin Function

Pin No.	Pin name	Pin function	Equivalent circuit
1	$V_{CC}1$	Supply voltage for all circuits other than the IC internal output block and the amplitude control block.	
2	$V_{CC}2$	Supply voltage for the IC internal output control block and the amplitude control block.	
3	V_S	Motor drive power supply. The voltage applied to this pin must not exceed $V_{CC}2$.	
5	U_{OUT}	U phase output.	
7	V_{OUT}	V phase output.	
9	W_{OUT}	W phase output. (These outputs include built-in spark killer diodes.)	
6,8	RF	Ground for the output power transistors.	
10	VH^+	Hall element bias voltage supply. A voltage that is typically 0.95V is generated between the VH^+ and VH^- pins (When I_H is 5mA).	
11	VH^-		
13	GND	Ground for circuits other than the output transistor. The RF pin potential is the lowest output transistor potential.	
14	FRC	Forward/reverse selection. Applications can select motor forward or reverse direction rotation using this pin. (This pin has hysteresis characteristics.)	
15	STBY	Selects the bias supply for all circuits other than the FG comparators. The bias supply is cut when this pin is set to the low level.	
16 17	$U_{IN}1$ $U_{IN}2$	U phase Hall element input. The logic high level is the state where the IN^+ voltage is greater than the IN^- voltage.	
18 19	$V_{IN}1$ $V_{IN}2$	V phase Hall element input. The logic high level is the state where the IN^+ voltage is greater than the IN^- voltage.	
20 21	$W_{IN}1$ $W_{IN}2$	W phase Hall element input. The logic high level is the state where the IN^+ voltage is greater than the IN^- voltage.	
12	ANGLE	Hall input/output gain control. The gain is controlled by the resistor connected between this pin and ground.	
22	FG_{IN}^+	FG comparator non-inverting inputs. There is no internally applied bias.	
23	FG_{IN}^-	FG comparator inverting inputs. There is no internally applied bias.	
24	FG_{OUT}	FG comparator outputs. There is an internal 20kΩ resistor load.	

Overlap Generation and Calculation Method



Overlap Generation

Since the voltage generated in the amplitude control block is, taking the center point as the reference, 2 × <overlap> × (1/2 $V_S - V_X$) on one side, the intersection point of the waveform will be <overlap> × (1/2 V_S – VX) from the center point.

To clamp that waveform at (1/2 $V_S - V_X$) referenced to the center point the overlap must be:

A/B × 100 = <overlap> × 100 (%).

Overlap Calculation

• Upper side overlap

Calculated center point: $V_N = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$

Since $A = V\alpha - V_N$, $B = V_S - V_{XH} - V_N$, the upper side overlap will be:

$$<\text{overlap}> = \frac{A}{B} = \frac{V\alpha - ((V_S - V_{XH} + V_{XL})/2)}{V_S - V_{XH} - ((V_S - V_{XH} + V_{XL})/2)} \times 100$$

Which can be calculated as:

$$= \frac{2V\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

• Lower side overlap

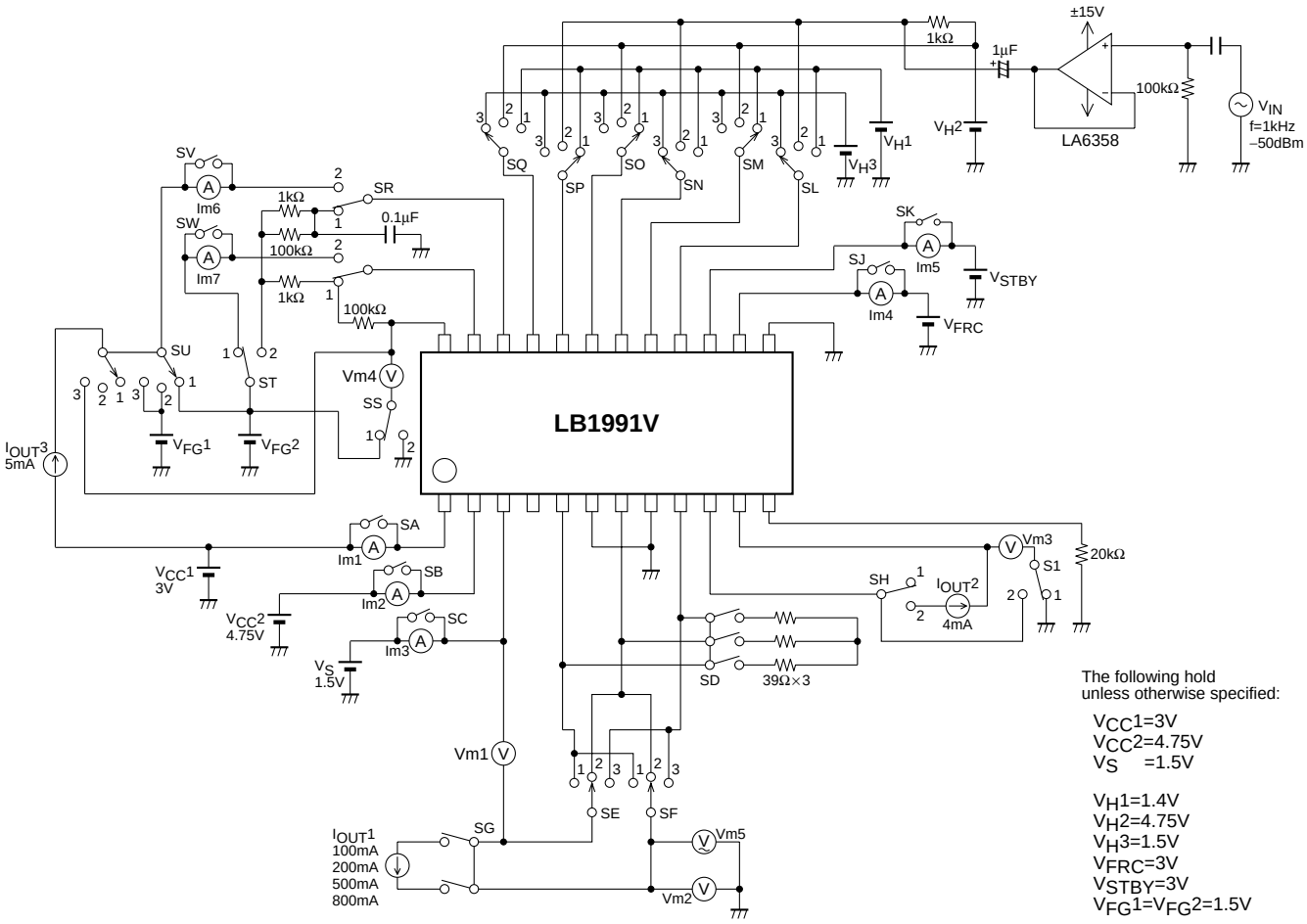
Since $C = V_N - V\beta$, and $D = V_N - V_{XL}$, the lower side overlap will be:

$$<\text{overlap}> = \frac{C}{D} = \frac{((V_S - V_{XH} + V_{XL})/2) - V\beta}{((V_S - V_{XH} + V_{XL})/2) - V_{XL}} \times 100$$

Which can be calculated as:

$$= \frac{(V_S - V_{XH}) + V_{XL} - 2V\beta}{(V_S - V_{XH}) - V_{XL}} \times 100(\%)$$

Test Circuit



The following hold unless otherwise specified:

$V_{CC}1$=3V
$V_{CC}2$=4.75V
V_S =1.5V

V_H1=1.4V
V_H2=4.75V
V_H3=1.5V
V_{FRC}=3V
V_{STBY}=3V
$V_{FG}1$=$V_{FG}2$=1.5V

Switch status:
0 : CLOSED
X : OPEN

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