



CC2652RB SimpleLink™ crystal-less BAW multiprotocol 2.4-GHz wireless MCU

1 Device Overview

1.1 Features

- Microcontroller
 - Powerful 48 MHz Arm® Cortex®-M4F Processor
 - EEMBC CoreMark® Score: 148
 - 352KB of In-System Programmable Flash
 - 256KB of ROM for Protocols and Firmware
 - 8KB of Cache SRAM (Alternatively available as General-Purpose RAM)
 - 80KB of Ultra-Low Leakage SRAM with parity
 - 2-Pin cJTAG and JTAG Debugging
 - Supports Over-the-Air Upgrade (OTA)
- Ultra-Low Power Sensor Controller With 4KB of SRAM
 - Sample, Store, and Process Sensor Data
 - Operation Independent From System CPU
 - Fast Wake-Up for Low-Power Operation
- TI-RTOS, Drivers, Bootloader, *Bluetooth*® 5 Low Energy Controller, and IEEE 802.15.4 MAC in ROM for Optimized Application Size
- RoHS-Compliant Package
 - 7-mm × 7-mm RGZ VQFN48 (31 GPIOs)
- Peripherals
 - Digital Peripherals Can be Routed to Any GPIO
 - 4× 32-Bit or 8× 16-Bit General-Purpose Timers
 - 12-Bit ADC, 200 kSamples/s, 8 Channels
 - 2× Comparators With Internal Reference DAC (1× Continuous Time, 1× Ultra-Low Power)
 - Programmable Current Source
 - 2× UART
 - 2× SSI (SPI, MICROWIRE, TI)
 - I²C
 - I²S
 - Real-Time Clock (RTC)
 - AES 128- and 256-bit Crypto Accelerator
 - ECC and RSA Public Key Hardware Accelerator
 - SHA2 Accelerator (Full Suite Up to SHA-512)
 - True Random Number Generator (TRNG)
 - Capacitive Sensing, Up to 8 Channels
 - Integrated Temperature and Battery Monitor
- External System
 - Integrated Bulk Acoustic Wave (BAW) resonator generating accurate clock for system and RF
 - On-Chip Buck DC/DC Converter
- Low Power
 - Wide Supply Voltage Range: 1.8 V to 3.8 V
 - Active-Mode RX: 7.3 mA
 - Active-Mode TX: 7.9 mA
 - Active-Mode MCU 48 MHz (CoreMark): 3.4 mA (71 µA/MHz)
 - Sensor Controller, Low Power-Mode, 2 MHz, running infinite loop: 30.8 µA
 - Sensor Controller, Active-Mode, 24 MHz, running infinite loop: 808 µA
 - Standby: 0.9 µA (RTC on, 80KB RAM and CPU Retention)
- Radio Section
 - 2.4-GHz RF Transceiver Compatible With Bluetooth 5 Low Energy and IEEE 802.15.4 PHY and MAC
 - Excellent Receiver Sensitivity:
 - –100 dBm for 802.15.4 (2.4 GHz),
 - –101 dBm for Bluetooth 5 Low Energy Coded
 - Programmable Output Power Up to +5 dBm
 - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations
 - EN 300 328, (Europe)
 - EN 300 440 Class 2 (Europe)
 - FCC CFR47 Part 15 (US)
 - ARIB STD-T66 (Japan)
- Development [Tools and Software](#)
 - [LP-CC2652RB LaunchPad™ Development Kit](#)
 - [SimpleLink™ CC13x2 and CC26x2 software development kit](#)
 - [SmartRF™ Studio](#) for Simple Radio Configuration
 - [Sensor Controller Studio](#) for Building Low-Power Sensing Applications



1.2 Applications

- 2400 to 2480 MHz ISM and SRD Systems ⁽¹⁾
With Down to 4 kHz of Receive Bandwidth
- Home and Building Automation
 - Building Security systems – motion detector, electronic door lock, door and window sensor, gateway
 - HVAC – thermostat, wireless environmental sensor, HVAC system controller
 - Fire safety systems – smoke detector, fire alarm control panel
 - Video surveillance – IP camera
 - Garage Door Openers
 - Elevator and escalator control
- Smart Grid and Automatic Meter Reading
 - Water, Gas, and Electricity Meters
 - Heat Cost Allocators
 - Gateways
- Wireless Sensor Networks
 - Long-Range Sensor Applications
- Asset Tracking and Management
- Factory Automation
- Wireless Healthcare Applications
- Energy Harvesting Applications
- Electronic Shelf Label (ESL)

(1) See [RF Core](#) for additional details on supported protocol standards, modulation formats, and data rates.

1.3 Description

The CC2652RB BAW device is a multiprotocol wireless 2.4-GHz MCU targeting Thread, Zigbee®, Bluetooth® 5 Low Energy, IEEE 802.15.4, IPv6-enabled smart objects (6LoWPAN), Wi-SUN®.

The CC2652RB device is a member of the SimpleLink™ MCU platform of cost-effective, ultra-low power, 2.4-GHz and Sub-1 GHz RF devices. Very low active RF and microcontroller (MCU) current, in addition to sub-μA sleep current with up to 80KB of parity protected RAM retention, provide excellent battery lifetime and allow operation on small coin-cell batteries and in energy-harvesting applications.

The CC2652RB device combines a flexible, very low-power [RF transceiver](#) with a powerful 48 MHz Arm® Cortex®-M4F CPU in a platform supporting multiple physical layers and RF standards. A dedicated Radio Controller (Arm® Cortex®-M0) handles low-level RF protocol commands that are stored in ROM or RAM, thus ensuring ultra-low power and great flexibility. The low power consumption of the CC2652RB device does not come at the expense of RF performance; the CC2652RB device has excellent sensitivity and robustness (selectivity and blocking) performance.

The CC2652RB device is a highly integrated, true single-chip solution incorporating a complete RF system and an on-chip DC/DC converter. In addition, the CC2652RB device has an integrated BAW (Bulk Acoustic Wave) resonator used to generate the RF carrier to eliminate the need for an external 48 MHz crystal.

Sensors can be handled in a very low-power manner by a programmable, autonomous ultra-low power Sensor Controller CPU with 4KB of SRAM for program and data. The Sensor Controller, with its fast wake-up and ultra-low-power 2 MHz mode is designed for sampling, buffering, and processing both analog and digital sensor data; thus the MCU system can maximize sleep time and reduce active power.

The CC2652RB device is part of the SimpleLink™ microcontroller (MCU) platform, which consists of Wi-Fi®, Bluetooth® Low Energy, Thread, Zigbee, Sub-1 GHz MCUs, and host MCUs, which all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit ti.com/simplelink.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CC2652RB1FRGZ	VQFN (48)	7.00 mm × 7.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in [Section 9](#), or see the [TI website](#).

1.4 Functional Block Diagram

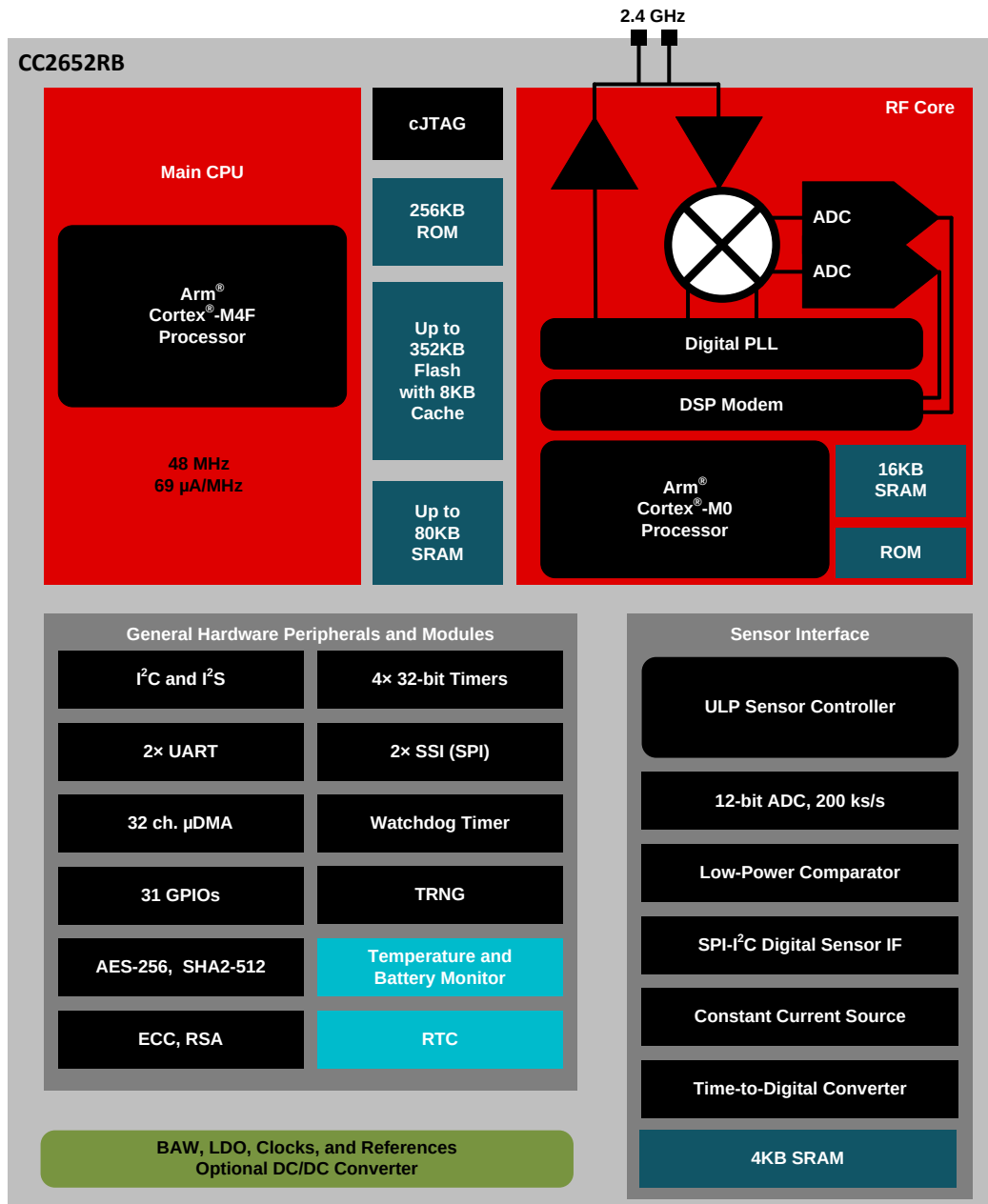


Figure 1-1. CC2652RB Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2019) to Revision A	Page
• Changed Table 5-4	20
• Added paragraph after Table 5-4	20
• Added Figure 5-1	21

3 Device Comparison

Table 3-1. Device Family Overview

DEVICE	RADIO SUPPORT	FLASH (KB)	RAM (KB)	GPIO	PACKAGE SIZE
CC1312R	Sub-1 GHz	352	80	30	RGZ (7-mm × 7-mm VQFN48)
CC1352R	Multiprotocol Sub-1 GHz Bluetooth 5 Low Energy Zigbee Thread 2.4-GHz proprietary FSK-based formats	352	80	28	RGZ (7-mm × 7-mm VQFN48)
CC1352P	Multiprotocol Sub-1 GHz Bluetooth 5 Low Energy Zigbee Thread 2.4-GHz proprietary FSK-based formats +20-dBm high-power amplifier	352	80	26	RGZ (7-mm × 7-mm VQFN48)
CC2642R	Bluetooth 5 Low Energy 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2652R	Multiprotocol Bluetooth 5 Low Energy Zigbee Thread 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48) YBG (3.07 mm × 3.50 mm DSBGA54)
CC2652RB	Multiprotocol Bluetooth 5 Low Energy Zigbee Thread 2.4-GHz proprietary FSK-based formats	352	80	31	RGZ (7-mm × 7-mm VQFN48)
CC2652P	Multiprotocol Bluetooth 5 Low Energy Zigbee Thread 2.4-GHz proprietary FSK-based formats +19.5-dBm high-power amplifier	352	80	26	RGZ (7-mm × 7-mm VQFN48)
CC1310	Sub-1 GHz	32–128	16–20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC1350	Sub-1 GHz Bluetooth 4.2 Low Energy	128	20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32)
CC2640R2F	Bluetooth 5 Low Energy 2.4-GHz proprietary FSK-based formats	128	20	10–31	RGZ (7-mm × 7-mm VQFN48) RHB (5-mm × 5-mm VQFN32) RSM (4-mm × 4-mm VQFN32) YFV (2.7-mm × 2.7-mm DSBGA34)
CC2640R2F-Q1	Bluetooth 5 Low Energy 2.4-GHz proprietary FSK-based formats	128	20	31	RGZ (7-mm × 7-mm VQFN48)

ADVANCE INFORMATION

4 Terminal Configuration and Functions

4.1 Pin Diagram – RGZ Package (Top View)

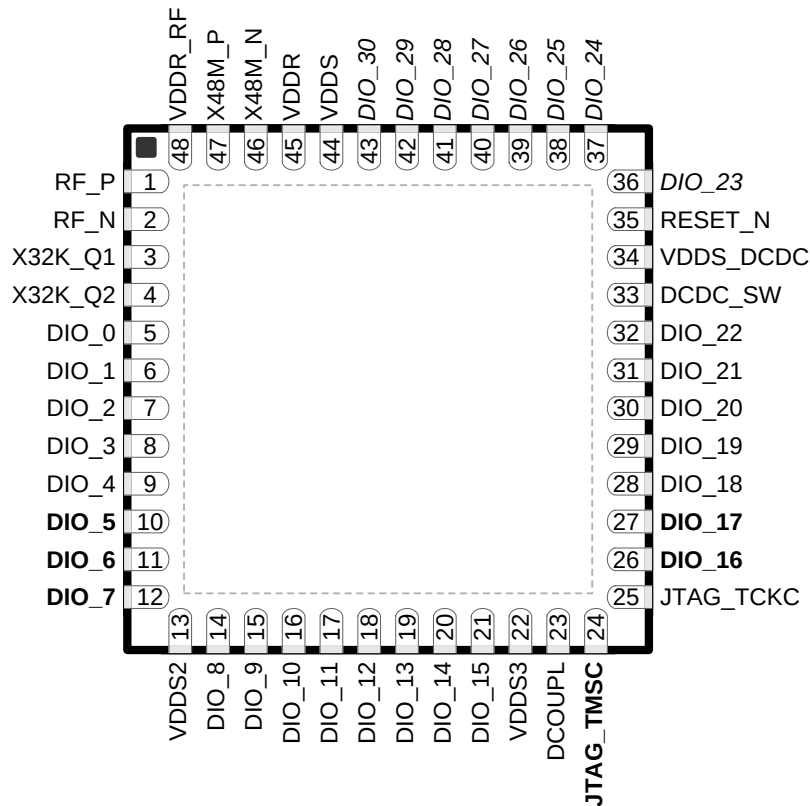


Figure 4-1. RGZ (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in Figure 4-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in Figure 4-1 in *italics* have analog capabilities:

- Pin 36, *DIO_23*
- Pin 37, *DIO_24*
- Pin 38, *DIO_25*
- Pin 39, *DIO_26*
- Pin 40, *DIO_27*
- Pin 41, *DIO_28*
- Pin 42, *DIO_29*
- Pin 43, *DIO_30*

4.2 Signal Descriptions – RGZ Package

Table 4-1. Signal Descriptions – RGZ Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
DCDC_SW	33	—	Power	Output from internal DC/DC converter ⁽¹⁾
DCOUP_L	23	—	Power	For decoupling of internal 1.27 V regulated digital-supply ⁽²⁾
DIO_0	5	I/O	Digital	GPIO
DIO_1	6	I/O	Digital	GPIO
DIO_2	7	I/O	Digital	GPIO
DIO_3	8	I/O	Digital	GPIO
DIO_4	9	I/O	Digital	GPIO
DIO_5	10	I/O	Digital	GPIO, high-drive capability
DIO_6	11	I/O	Digital	GPIO, high-drive capability
DIO_7	12	I/O	Digital	GPIO, high-drive capability
DIO_8	14	I/O	Digital	GPIO
DIO_9	15	I/O	Digital	GPIO
DIO_10	16	I/O	Digital	GPIO
DIO_11	17	I/O	Digital	GPIO
DIO_12	18	I/O	Digital	GPIO
DIO_13	19	I/O	Digital	GPIO
DIO_14	20	I/O	Digital	GPIO
DIO_15	21	I/O	Digital	GPIO
DIO_16	26	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	27	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	28	I/O	Digital	GPIO
DIO_19	29	I/O	Digital	GPIO
DIO_20	30	I/O	Digital	GPIO
DIO_21	31	I/O	Digital	GPIO
DIO_22	32	I/O	Digital	GPIO
DIO_23	36	I/O	Digital or Analog	GPIO, analog capability
DIO_24	37	I/O	Digital or Analog	GPIO, analog capability
DIO_25	38	I/O	Digital or Analog	GPIO, analog capability
DIO_26	39	I/O	Digital or Analog	GPIO, analog capability
DIO_27	40	I/O	Digital or Analog	GPIO, analog capability
DIO_28	41	I/O	Digital or Analog	GPIO, analog capability
DIO_29	42	I/O	Digital or Analog	GPIO, analog capability
DIO_30	43	I/O	Digital or Analog	GPIO, analog capability
EGP	—	—	GND	Ground – exposed ground pad ⁽³⁾
JTAG_TMSC	24	I/O	Digital	JTAG TMS, high-drive capability
JTAG_TCKC	25	I	Digital	JTAG TCK
RESET_N	35	I	Digital	Reset, active low. No internal pullup resistor
RF_P	1	—	RF	Positive RF input signal to LNA during RX Positive RF output signal from PA during TX
RF_N	2	—	RF	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX

(1) For more details, see technical reference manual listed in [Section 8.2](#).

(2) Do not supply external circuitry from this pin.

(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.

Table 4-1. Signal Descriptions – RGZ Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
VDDR	45	—	Power	Internal supply, typically connect to output of internal DC/DC converter ⁽⁴⁾⁽²⁾⁽⁵⁾
VDDR_RF	48	—	Power	Internal supply, typically connect to output of internal DC/DC converter ⁽⁶⁾⁽²⁾⁽⁵⁾
VDDS	44	—	Power	1.8-V to 3.8-V main chip supply ⁽¹⁾
VDDS2	13	—	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS3	22	—	Power	1.8-V to 3.8-V DIO supply ⁽¹⁾
VDDS_DCDC	34	—	Power	1.8-V to 3.8-V DC/DC converter supply
X48M_N	46	—	Analog	48-MHz crystal oscillator pin 1. Do not connect if not in use. (Optional) ⁽⁷⁾
X48M_P	47	—	Analog	48-MHz crystal oscillator pin 2. Do not connect if not in use. (Optional) ⁽⁷⁾
X32K_Q1	3	—	Analog	32-kHz crystal oscillator pin 1
X32K_Q2	4	—	Analog	32-kHz crystal oscillator pin 2

(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.

(5) Output from internal DC/DC and LDO is trimmed to 1.68 V.

(6) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.

(7) The X48M_N and X48M_P pins can be used to connect an external 48-MHz crystal. This clock can be used instead of the internal BAW clock. However, it is not required for the device standard operation.

4.3 Connections for Unused Pins and Modules

Table 4-2. Connections for Unused Pins

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE ⁽¹⁾	PREFERRED PRACTICE ⁽¹⁾
GPIO	DIO_n	5–12 14–21 26–32 36–43	NC or GND	NC
32.768-kHz crystal	X32K_Q1	3	NC or GND	NC
	X32K_Q2	4		
DC/DC converter ⁽²⁾	DCDC_SW	33	NC	NC
	VDDS_DCDC	34	VDDS	VDDS
48-MHz crystal	X48M_N	46	NC	NC
	X48M_P	47	NC	NC

(1) NC = No connect

(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the VDDR decoupling capacitor must be connected and moved close to VDDR.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

		MIN	MAX	UNIT
V _{DD} S ⁽³⁾	Supply voltage	−0.3	4.1	V
	Voltage on any digital pin ⁽⁴⁾	−0.3	V _{DD} S + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2	−0.3	V _{DD} R + 0.3, max 2.25	V
V _{in}	Voltage on ADC input	Voltage scaling enabled	V _{DD} S	V
		Voltage scaling disabled, internal reference	1.49	
		Voltage scaling disabled, V _{DD} S as reference	V _{DD} S / 2.9	
T _{stg}	Storage temperature	−40	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to ground, unless otherwise noted.
- (3) V_{DD}S2 and V_{DD}S3 must be at the same potential as V_{DD}S.
- (4) Including analog capable DIO.

5.2 ESD Ratings

				VALUE	UNIT
V _{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾	All pins	±2000	V
		Charged device model (CDM), per JS-002 ⁽²⁾	All pins	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature range	−40	85	°C
Operating supply voltage (V _{DD} S)	1.8	3.8	V
Rising supply voltage slew rate	0	100	mV/μs
Falling supply voltage slew rate ⁽¹⁾	0	20	mV/μs

- (1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22-μF V_{DD}S input capacitor must be used to ensure compliance with this slew rate.

5.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TYP	UNIT
V _{DD} S Power-on-Reset (POR) threshold		1.1 - 1.55	V
V _{DD} S Brownout Detector (BOD) ⁽¹⁾	Rising Threshold	1.77	V
V _{DD} S Brownout Detector (BOD), before initial boot ⁽²⁾	Rising Threshold	1.70	V
V _{DD} S Brownout Detector (BOD) ⁽¹⁾	Falling Threshold	1.75	V

- (1) For boost mode (V_{DD}R=1.95V), TI drivers software initialization will trim V_{DD}S BOD limits to maximum (approximately 2.0V)
- (2) Brownout Detector is trimmed at first boot, value is kept until device is reset by a POR reset or the RESET_N pin

5.5 Power Consumption - Power Modes

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
CORE CURRENT CONSUMPTION				
I_{core} Core current consumption	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	100	nA
		Shutdown. No clocks running, no retention	105	
	Standby without cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	0.9	μA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	0.99	μA
	Standby with cache retention	RTC running, CPU, 80KB RAM and (partial) register retention. RCOSC_LF	2.82	μA
		RTC running, CPU, 80KB RAM and (partial) register retention. XOSC_LF	2.94	μA
	Idle	Supply Systems and RAM powered. RCOSC_HF	680	μA
	Active	MCU running CoreMark at 48 MHz. RCOSC_HF	3.32	mA
PERIPHERAL CURRENT CONSUMPTION^{(1) (2)}				
I_{peri}	Peripheral power domain	Delta current with domain enabled		μA
	Serial power domain	Delta current with domain enabled		
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle		
	μDMA	Delta current with clock enabled, module is idle		
	Timers	Delta current with clock enabled, module is idle		
	I2C	Delta current with clock enabled, module is idle		
	I2S	Delta current with clock enabled, module is idle		
	SSI	Delta current with clock enabled, module is idle		
	UART	Delta current with clock enabled, module is idle		
	CRYPTO	Delta current with clock enabled, module is idle		

(1) Adds to core current I_{core} for each peripheral unit activated.

(2) I_{peri} is not supported in Standby or Shutdown modes.

5.6 Power Consumption - Radio Modes

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ with DC/DC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	TYP	UNIT
Radio receive current	2440 MHz	7.3	mA
Radio transmit current	0-dBm output power setting 2440 MHz	7.9	mA
	+5-dBm output power setting 2440 MHz	10.2	mA

5.7 Nonvolatile (Flash) Memory Characteristics

over operating free-air temperature range and $V_{DD5} = 3.0\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank		30			k Cycles
Supported flash erase cycles before failure, single sector		60			k Cycles
Maximum number of write operations per row before sector erase ⁽¹⁾				83	write operations
Flash retention	105 °C	11.4			years at 105 °C
Flash sector erase current	Average delta current		10.4		mA
Flash sector erase time ⁽²⁾			8		ms
Flash write current	Average delta current, 4 bytes at a time		6		mA
Flash write time ⁽²⁾	4 bytes at a time		21		µs

- (1) Each row is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole flash sector before a sector erase is required.
- (2) This number is dependent on Flash aging and increases over time and erase cycles.

5.8 Bluetooth Low Energy — Receive (RX)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125-kbps (Bluetooth 5 Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–102		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–260		310	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	–260		260	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	–140		150	ppm
Co-channel rejection ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–3		dB
Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 1\text{ MHz}$, BER = 10^{-3}		9 / 5 ⁽²⁾		dB
Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3}		43 / 32 ⁽²⁾		dB
Selectivity, $\pm 3\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 3\text{ MHz}$, BER = 10^{-3}		47 / 42 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3}		46 / 47 ⁽²⁾		dB
Selectivity, $\pm 6\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\geq \pm 6\text{ MHz}$, BER = 10^{-3}		49 / 46 ⁽²⁾		dB
Alternate channel rejection, $\pm 7\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\geq \pm 7\text{ MHz}$, BER = 10^{-3}		50 / 47 ⁽²⁾		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		32		dB
Selectivity, Image frequency $\pm 1\text{ MHz}$ ⁽¹⁾	Note that Image frequency + 1 MHz is the Co-channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at $\pm 1\text{ MHz}$ from image frequency, BER = 10^{-3}		5 / 32 ⁽²⁾		dB
Blocker rejection, $\pm 8\text{ MHz}$ and above ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\geq \pm 8\text{ MHz}$ and above, BER = 10^{-3}		>46		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		–40		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–22		dBm
Intermodulation	Wanted signal at 2402 MHz, –76 dBm. Two interferers at 2405 and 2408 MHz, respectively, at the given power level		–42		dBm
500-kbps (Bluetooth 5 Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–99		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–240		240	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)	–500		500	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)	–310		330	ppm
Co-channel rejection ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–5		dB
Selectivity, $\pm 1\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 1\text{ MHz}$, BER = 10^{-3}		9 / 5 ⁽²⁾		dB
Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾	Wanted signal at –79 dBm, modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3}		41 / 31 ⁽²⁾		dB

(1) Numbers given as I/C dB.

(2) X / Y, where X is +N MHz and Y is –N MHz.

(3) Excluding one exception at $F_{\text{wanted}} / 2$, per Bluetooth Specification.

Bluetooth Low Energy — Receive (RX) (continued)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, $\pm 3\text{ MHz}^{(1)}$	Wanted signal at -79 dBm , modulated interferer at $\pm 3\text{ MHz}$, $\text{BER} = 10^{-3}$		44 / 41 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}^{(1)}$	Wanted signal at -79 dBm , modulated interferer at $\pm 4\text{ MHz}$, $\text{BER} = 10^{-3}$		44 / 44 ⁽²⁾		dB
Selectivity, $\pm 6\text{ MHz}^{(1)}$	Wanted signal at -79 dBm , modulated interferer at $\geq \pm 6\text{ MHz}$, $\text{BER} = 10^{-3}$		44 / 44 ⁽²⁾		dB
Alternate channel rejection, $\pm 7\text{ MHz}^{(1)}$	Wanted signal at -79 dBm , modulated interferer at $\geq \pm 7\text{ MHz}$, $\text{BER} = 10^{-3}$		44 / 44 ⁽²⁾		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at -79 dBm , modulated interferer at image frequency, $\text{BER} = 10^{-3}$		31		dB
Selectivity, Image frequency $\pm 1\text{ MHz}^{(1)}$	Note that Image frequency + 1 MHz is the Co-channel -1 MHz . Wanted signal at -79 dBm , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $\text{BER} = 10^{-3}$		5 / 41 ⁽²⁾		dB
Blocker rejection, $\pm 8\text{ MHz}$ and above	Wanted signal at -79 dBm , modulated interferer at $\geq \pm 8\text{ MHz}$ and above, $\text{BER} = 10^{-3}$		44		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		-35		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		-19		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		-19		dBm
Intermodulation	Wanted signal at 2402 MHz, -76 dBm . Two interferers at 2405 and 2408 MHz, respectively, at the given power level		-37		dBm
1-Mbps 2-GFSK (Bluetooth 4 and Bluetooth 5 Low Energy)					
Receiver sensitivity	Differential mode. $\text{BER} = 10^{-3}$		-97		dBm
Receiver saturation	Differential mode. $\text{BER} = 10^{-3}$		4		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	-350		350	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	-750		750	ppm
Co-channel rejection ⁽¹⁾	Wanted signal at -67 dBm , modulated interferer in channel, $\text{BER} = 10^{-3}$		-6		dB
Selectivity, $\pm 1\text{ MHz}^{(1)}$	Wanted signal at -67 dBm , modulated interferer at $\pm 1\text{ MHz}$, $\text{BER} = 10^{-3}$		7 / 3 ⁽²⁾		dB
Selectivity, $\pm 2\text{ MHz}^{(1)}$	Wanted signal at -67 dBm , modulated interferer at $\pm 2\text{ MHz}$, $\text{BER} = 10^{-3}$		34 / 25 ⁽²⁾		dB
Selectivity, $\pm 3\text{ MHz}^{(1)}$	Wanted signal at -67 dBm , modulated interferer at $\pm 3\text{ MHz}$, $\text{BER} = 10^{-3}$		38 / 26 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}^{(1)}$	Wanted signal at -67 dBm , modulated interferer at $\pm 4\text{ MHz}$, $\text{BER} = 10^{-3}$		42 / 29 ⁽²⁾		dB
Selectivity, $\pm 5\text{ MHz}$ or more ⁽¹⁾	Wanted signal at -67 dBm , modulated interferer at $\geq \pm 5\text{ MHz}$, $\text{BER} = 10^{-3}$		32		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at -67 dBm , modulated interferer at image frequency, $\text{BER} = 10^{-3}$		25		dB
Selectivity, Image frequency $\pm 1\text{ MHz}^{(1)}$	Wanted signal at -67 dBm , modulated interferer at $\pm 1\text{ MHz}$ from image frequency, $\text{BER} = 10^{-3}$		3 / 26 ⁽²⁾		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		-20		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		-5		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		-8		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		-8		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm . Two interferers at 2405 and 2408 MHz, respectively, at the given power level		-34		dBm
Spurious emissions, 30 to 1000 MHz ⁽⁴⁾	Measurement in a 50- Ω single-ended load.		-71		dBm

(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Bluetooth Low Energy — Receive (RX) (continued)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious emissions, 1 to 12.75 GHz ⁽⁴⁾	Measurement in a 50 Ω single-ended load.		–62		dBm
RSSI dynamic range			70		dB
RSSI accuracy					dB
2-Mbps 2-GFSK (Bluetooth 5)					
Receiver sensitivity	Differential mode. Measured at SMA connector, BER = 10^{-3}		–92		dBm
Receiver saturation	Differential mode. Measured at SMA connector, BER = 10^{-3}		4		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency	–300		500	kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	–1000		1000	ppm
Co-channel rejection ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–7		dB
Selectivity, $\pm 2\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 2\text{ MHz}$, BER = 10^{-3}		8 / 4 ⁽²⁾		dB
Selectivity, $\pm 4\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 4\text{ MHz}$, BER = 10^{-3}		31 / 26 ⁽²⁾		dB
Selectivity, $\pm 6\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\pm 6\text{ MHz}$, BER = 10^{-3}		37 / 38 ⁽²⁾		dB
Alternate channel rejection, $\pm 7\text{ MHz}$ ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at $\geq \pm 7\text{ MHz}$, BER = 10^{-3}		37 / 36 ⁽²⁾		dB
Selectivity, Image frequency ⁽¹⁾	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB
Selectivity, Image frequency $\pm 2\text{ MHz}$ ⁽¹⁾	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at $\pm 2\text{ MHz}$ from image frequency, BER = 10^{-3}		–7 / 26 ⁽²⁾		dB
Out-of-band blocking ⁽³⁾	30 MHz to 2000 MHz		–33		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–15		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–10		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz, respectively, at the given power level		–45		dBm

5.9 Bluetooth Low Energy — Transmit (TX)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Differential mode, delivered to a single-ended 50 Ω load through a balun		5		dBm
Output power programmable range	Differential mode, delivered to a single-ended 50 Ω load through a balun		26		dB
Output power variation over temperature	Over recommended temperature operating range				dB
Spurious emissions and harmonics					
Spurious emissions ⁽¹⁾	$f < 1\text{ GHz}$, outside restricted bands	+5-dBm setting	-43		dBm
	$f < 1\text{ GHz}$, restricted bands ETSI	+5-dBm setting	-65		dBm
	$f < 1\text{ GHz}$, restricted bands FCC	+5-dBm setting	-76		dBm
	$f > 1\text{ GHz}$, including harmonics	+5-dBm setting	-46		dBm
Harmonics ⁽¹⁾	Second harmonic	+5-dBm setting			dBm
	Third harmonic	+5-dBm setting			dBm
	Fourth harmonic	+5-dBm setting			dBm
	Fifth harmonic	+5-dBm setting			dBm

- (1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

5.10 Zigbee and Thread — IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) — RX

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, $f_{RF} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver sensitivity	PER = 1%		-101		dBm
Receiver saturation	PER = 1%		+4		dBm
Adjacent channel rejection	Wanted signal at -82 dBm, modulated interferer at $\pm 5\text{ MHz}$, PER = 1%		39		dB
Alternate channel rejection	Wanted signal at -82 dBm, modulated interferer at $\pm 10\text{ MHz}$, PER = 1%		52		dB
Channel rejection, $\pm 15\text{ MHz}$ or more	Wanted signal at -82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		57		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		64		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		68		dB
Blocking and desensitization, -5 MHz from lower band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, -10 MHz from lower band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, -20 MHz from lower band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Blocking and desensitization, -50 MHz from lower band edge	Wanted signal at -97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		67		dB
Spurious emissions, 30 MHz to 1000 MHz	Measurement in a 50- Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		-71		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Measurement in a 50- Ω single-ended load. Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66		-62		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		>200		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		>1000		ppm
RSSI dynamic range			100		dB
RSSI accuracy					dB

5.11 Zigbee and Thread — IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) — TX

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, $f_{\text{RF}} = 2440\text{ MHz}$ with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path.

All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power	Differential mode, delivered to a single-ended 50-Ω load through a balun		5			dBm
Output power programmable range	Differential mode, delivered to a single-ended 50-Ω load through a balun		26			dB
Output power variation over temperature	Over recommended temperature operating range					dB
Spurious emissions and harmonics						
Spurious emissions ⁽¹⁾	f < 1 GHz, outside restricted bands	+5-dBm setting	−43			dBm
	f < 1 GHz, restricted bands ETSI	+5-dBm setting	−65			dBm
	f < 1 GHz, restricted bands FCC	+5-dBm setting	−76			dBm
	f > 1 GHz, including harmonics	+5-dBm setting	−46			dBm
Harmonics ⁽¹⁾	Second harmonic	+5-dBm setting				dBm
	Third harmonic	+5-dBm setting				dBm
	Fourth harmonic	+5-dBm setting				dBm
	Fifth harmonic	+5-dBm setting				dBm
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						
Error vector magnitude	+5-dBm setting		2			%

- (1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

5.12 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		PACKAGE	UNIT ⁽²⁾
		RGZ (VQFN)	
		48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) °C/W = degrees Celsius per watt.

5.13 Timing and Switching Characteristics

Table 5-1. Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			μs

Table 5-2. Wakeup Timing

Measured over operating free-air temperature with $V_{DD5} = 3.0\text{ V}$ (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active ⁽¹⁾		850	3000		μs
MCU, Shutdown to Active ⁽¹⁾		850	3000		μs
MCU, Standby to Active			160		μs
MCU, Active to Standby			36		μs
MCU, Idle to Active			14		μs

- (1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.

5.13.1 Clock Specifications

Table 5-3. 48-MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.⁽¹⁾

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance $6\text{ pF} < C_L \leq 9\text{ pF}$		20	60	Ω
ESR	Equivalent series resistance $5\text{ pF} < C_L \leq 6\text{ pF}$			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)		$< 0.5 \times 10^{-24} / C_L^2$		H
C_L	Crystal load capacitance ⁽²⁾	5	7 ⁽³⁾	9	pF
	Start-up time ⁽⁴⁾		250		μs

- (1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
- (2) Adjustable load capacitance is integrated into the device.
- (3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG)
- (4) Startup time number requires use of TI-provided power driver which performs clock calibration every crystal startup. Startup time may increase if driver is not used.

NOTE

The device is designed to use the internal BAW clock. The XOSC_HF crystal oscillator is optional and can be used to replace the BAW clock.

Table 5-4. 48-MHz Bulk Acoustic Wave (BAW) Resonator

Measured on a Texas Instruments reference design with $T_c = -40$ to 85°C and $1.8\text{ V} < V_{\text{DDS}} < 3.8\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Nominal frequency ⁽¹⁾⁽²⁾⁽³⁾	47.808	48	48.192	MHz
Compensated frequency vs. temperature characteristics ⁽⁴⁾⁽⁵⁾	–40		40	ppm
Start-up time		8		μs

- (1) Clock frequency used in MCU and digital domains.
- (2) Exact frequency is measured by TI across temperature and stored in the device for clock compensation purposes.
- (3) Up to ± 200 ppm across temperature range from frequency at reference temperature of $+25^\circ\text{C}$.
- (4) Across operational temperature range.
- (5) Reference frequency is 48 MHz. Includes 10 year aging at 30°C . Compensated clock is provided to the RF PLL and modem.

In order to achieve superior frequency stability over temperature and battery (that is, voltage) conditions as well as device lifetime, the BAW frequency is actively compensated by the modem internal firmware. Every time the PLL is tuned (wake-up of radio from idle/standby or tuned to a different frequency), the modem firmware considers the BAW device characteristics stored on the device along with current temperature and voltage conditions and configures the PLL to compensate accordingly. The RF frequency accuracy around the desired center frequency is ± 40 ppm across temperature. Similar compensation function is also used by the software to compensate timing for non-RF activities such as protocol timing and RTC timer.

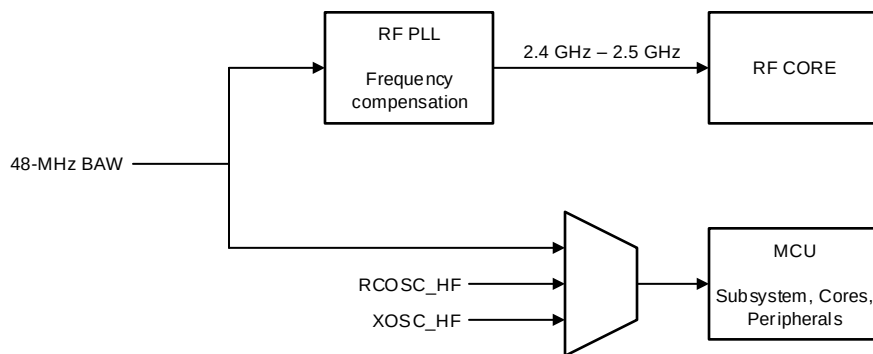


Figure 5-1. BAW Resonator Clocking Diagram

Table 5-5. 32.768-kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	k Ω
C_L	Crystal load capacitance	6	7 ⁽¹⁾	12	pF

- (1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

Table 5-6. 48-MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		± 1		%
Calibrated frequency accuracy ⁽¹⁾		± 0.25		%
Start-up time		5		μs

- (1) Accuracy relatively to the calibration source (XOSC_HF).

Table 5-7. 2-MHz RC Oscillator (RCOSC_MF)

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		2		MHz
Start-up time		5		μs

Table 5-8. 32-kHz RC Oscillator (RCOSC_LF)

Measured on the Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DD5}} = 3.0\text{ V}$, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Calibrated frequency		32.8 ⁽¹⁾		kHz
Temperature coefficient		50		ppm/ $^\circ\text{C}$

- (1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

5.13.2 Synchronous Serial Interface (SSI) Characteristics

Table 5-9. Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	system clocks ⁽¹⁾
S2 ⁽²⁾	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3 ⁽²⁾	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

(2) Refer to SSI timing diagrams [Figure 5-2](#), [Figure 5-3](#), and [Figure 5-4](#).

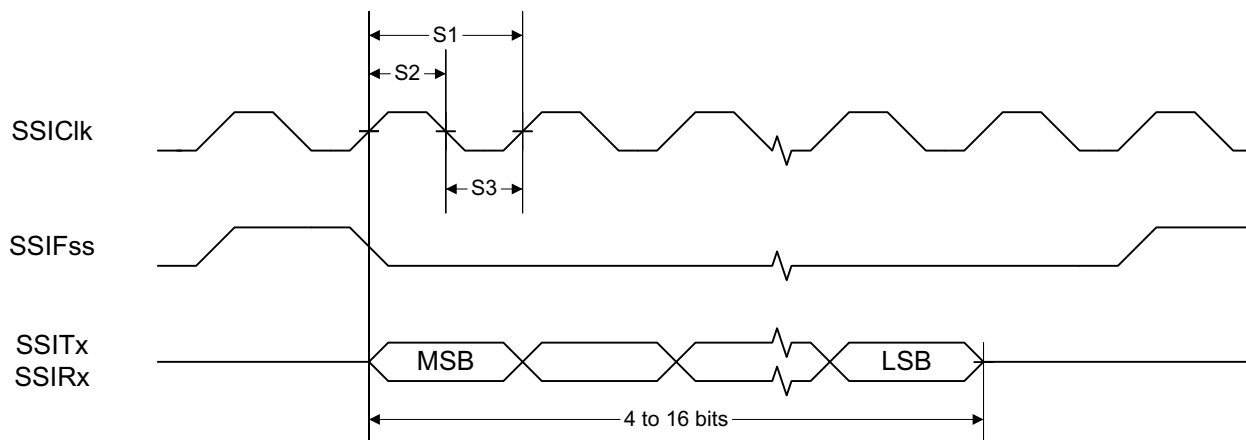


Figure 5-2. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

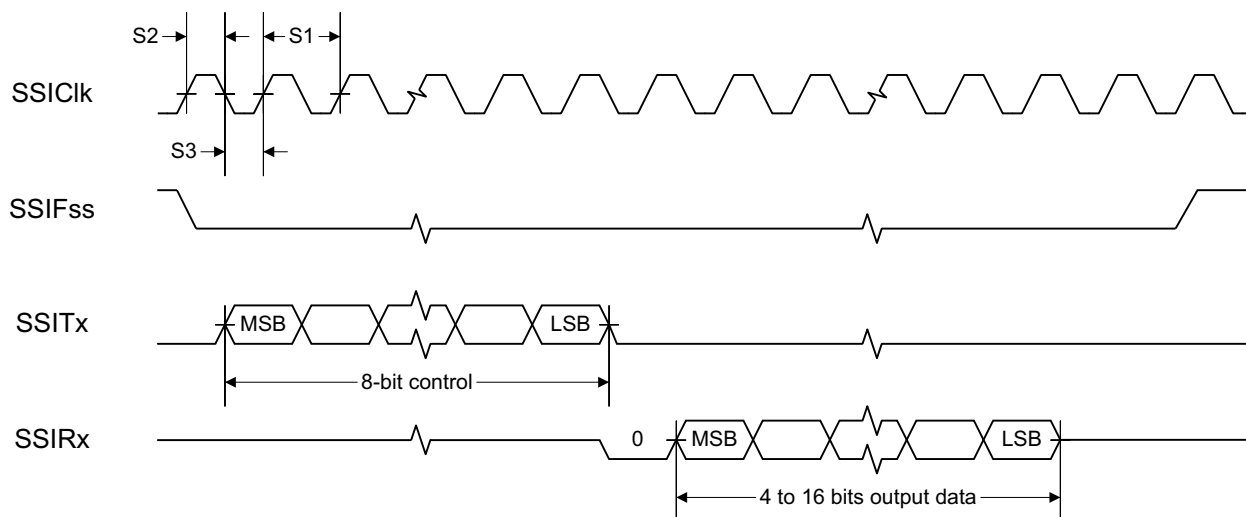


Figure 5-3. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

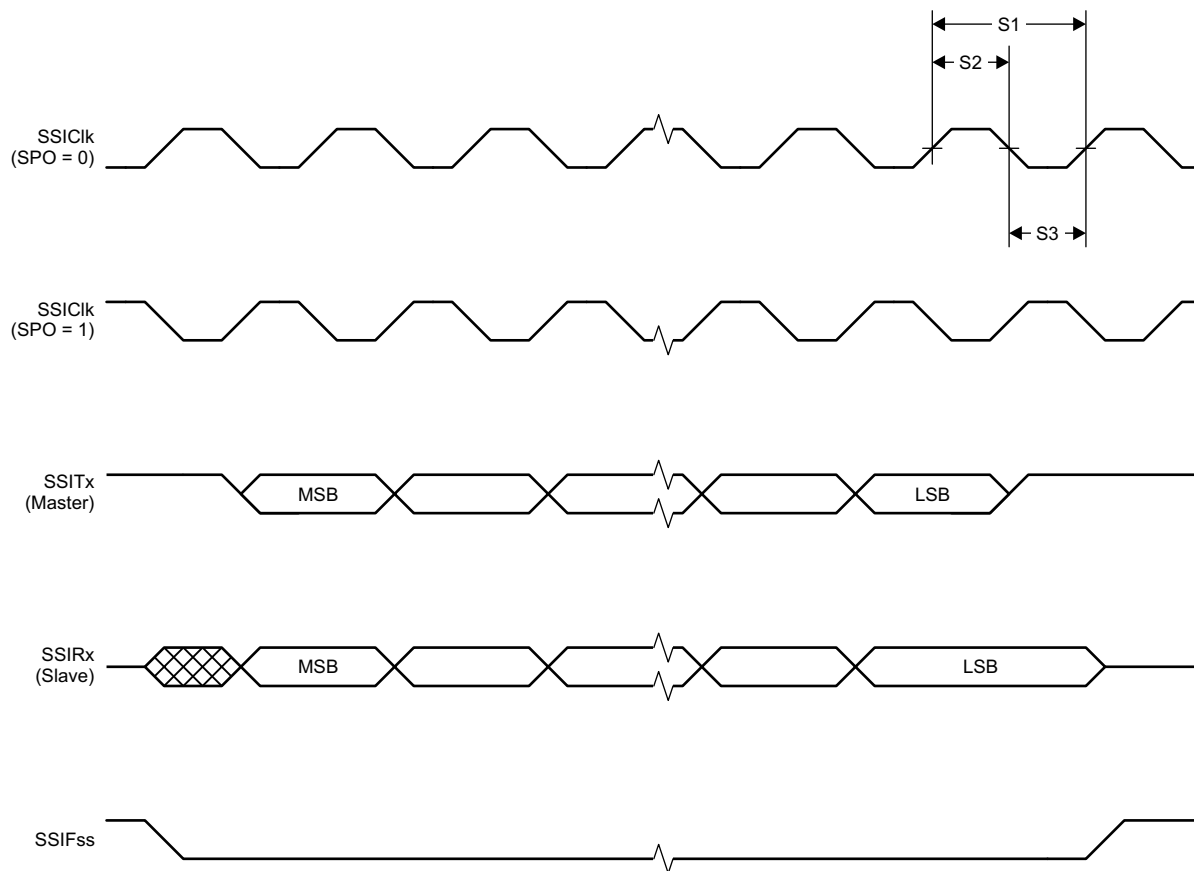


Figure 5-4. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

5.13.3 UART

Table 5-10. UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

5.14 Peripheral Characteristics

5.14.1 ADC

Table 5-11. ADC Characteristics

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$ and voltage scaling enabled, unless otherwise noted.⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V _{DD5}	V
	Resolution			12		Bits
	Sample rate				200	kSamples/s
	Offset	Internal 4.3-V equivalent reference ⁽²⁾		2		LSB
	Gain error	Internal 4.3-V equivalent reference ⁽²⁾		7.8		LSB
DNL ⁽³⁾	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3-V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6-kHz input tone		9.5		Bits
		V _{DD5} as reference, 200 kSamples/s, 9.6-kHz input tone		9.8		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		9.9		
THD	Total harmonic distortion	Internal 4.3-V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6-kHz input tone		–64		dB
		V _{DD5} as reference, 200 kSamples/s, 9.6-kHz input tone		–68		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and Distortion ratio	Internal 4.3-V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6-kHz input tone		59		dB
		V _{DD5} as reference, 200 kSamples/s, 9.6-kHz input tone		61		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3-V equivalent reference ⁽²⁾ , 200 kSamples/s, 9.6-kHz input tone		69		dB
		V _{DD5} as reference, 200 kSamples/s, 9.6-kHz input tone		72		
		Internal 1.44-V reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300-Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24-MHz clock		50		clock-cycles
	Current consumption	Internal 4.3-V equivalent reference ⁽²⁾		0.69		mA
	Current consumption	V _{DD5} as reference		0.93		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1.		4.3 ⁽²⁾⁽⁴⁾		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: $V_{ref} = 4.3\text{ V} \times 1408 / 4095$		1.48		V
	Reference voltage	V _{DD5} as reference (Also known as <i>RELATIVE</i>) (input voltage scaling enabled)		V _{DD5}		V
	Reference voltage	V _{DD5} as reference (Also known as <i>RELATIVE</i>) (input voltage scaling disabled)		V _{DD5} / 2.82 ⁽⁴⁾		V
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods.

(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V.

(3) No missing codes. Positive DNL typically varies up to 1.8 LSB, depending on device.

(4) Applied voltage must be within Absolute Maximum Ratings (see [Section 5.1](#)) at all times.

5.14.2 DAC

Table 5-12. Digital-to-Analog Converter (DAC) Characteristics
 $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution		8			Bits
V _{DDS}	Supply Voltage	Any load, any V _{REF} , Pre-charge OFF, DAC Charge-Pump ON	1.8		3.8	V
		External R C Load, any V _{REF} , Pre-charge OFF, DAC Charge-Pump OFF	2.0		3.8	
		Any load, V _{REF} = DECOUPL, Pre-charge ON	2.6		3.8	
F _{DAC}	Clock Frequency	Buffer ON (recommended for external load)	16		1000	kHz
		Buffer OFF (internal load)	16		250	
	Voltage Output Settling Time	V _{REF} = V _{DDS} , Buffer OFF, Internal Load		15		1 / F _{DAC}
		V _{REF} = V _{DDS} , Buffer ON, External Capacitive Load = 20 pF		19		
	External Capacitive Load				20	pF
	External Resistive Load		10			MΩ
	Short circuit Current				400	μA
I _{DAC}	Average Current Consumption Load = COMP_A or COMP_B Reference Input Buffer OFF DAC Charge-Pump OFF	V _{REF} = V _{DDS} or DECOUPL, Clock 16 kHz				μA
		V _{REF} = V _{DDS} or DECOUPL, Clock 250 kHz				
		V _{REF} = V _{DDS} or DECOUPL, Clock 1000 kHz				
		V _{REF} = ADCREF, Clock 16 kHz				
		V _{REF} = ADCREF, Clock 250 kHz				
		V _{REF} = ADCREF, Clock 1000 kHz				
I _{DAC}	Average Current Consumption External (R C) Load DAC Buffer ON DAC Charge-Pump ON	V _{REF} = V _{DDS} or DECOUPL, Clock 16 kHz				μA
		V _{REF} = V _{DDS} or DECOUPL, Clock 250 kHz				
		V _{REF} = ADCREF, Clock 16 kHz				
		V _{REF} = ADCREF, Clock 250 kHz				
Z _{MAX}	Max Output Impedance Vref = V _{DDS} , Buffer ON, CLK 250 kHz	V _{DDS} = 3.8V, DAC Charge-Pump OFF				kΩ
		V _{DDS} = 3.0V, DAC Charge-Pump ON				
		V _{DDS} = 3.0V, DAC Charge-Pump OFF				
		V _{DDS} = 2.0V, DAC Charge-Pump ON				
		V _{DDS} = 2.0V, DAC Charge-Pump OFF				
		V _{DDS} = 1.8V, DAC Charge-Pump ON				
		V _{DDS} = 1.8V, DAC Charge-Pump OFF				
Internal Load - COMP_A / COMP_B						
INL	Integral Non-Linearity	V _{REF} = V _{DDS} , Load = COMP_A				LSB
		V _{REF} = V _{DDS} , Load = COMP_B				
		V _{REF} = DECOUPL, Load = COMP_A				
		V _{REF} = DECOUPL, Load = COMP_B				
		V _{REF} = ADCREF, Load = COMP_A				
		V _{REF} = ADCREF, Load = COMP_B				
DNL	Differential Non-Linearity ⁽¹⁾	V _{REF} = V _{DDS} , DECOUPL or ADCREF Load = COMP_A or COMP_B		±1		LSB
				±1.6		
	Offset Error Load = COMP_A	V _{REF} = V _{DDS} = 3.8V				LSB
		V _{REF} = V _{DDS} = 3.0V				
		V _{REF} = V _{DDS} = 1.8V				
		V _{REF} = DECOUPL, Pre-charge ON				
		V _{REF} = DECOUPL, Pre-charge OFF				
		V _{REF} = ADCREF				

(1) DNL ≤ 1 LSB is guaranteed monotonic

Table 5-12. Digital-to-Analog Converter (DAC) Characteristics (continued)T_c = 25°C, V_{DD}S = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Offset Error Load = COMP_B	V _{REF} = V _{DD} S = 3.8V				LSB
		V _{REF} = V _{DD} S = 3.0V				
		V _{REF} = V _{DD} S = 1.8V				
		V _{REF} = DECOUPL, Pre-charge ON				
		V _{REF} = DECOUPL, Pre-charge OFF				
		V _{REF} = ADCREF				
	Max Code Output Voltage Variation Load = COMP_A	V _{REF} = V _{DD} S = 3.8V				LSB
		V _{REF} = V _{DD} S = 3.0V				
		V _{REF} = V _{DD} S = 1.8V				
		V _{REF} = DECOUPL, Pre-charge ON				
		V _{REF} = DECOUPL, Pre-charge OFF				
		V _{REF} = ADCREF				
	Max Code Output Voltage Variation Load = COMP_B	V _{REF} = V _{DD} S = 3.8V				LSB
		V _{REF} = V _{DD} S = 3.0V				
		V _{REF} = V _{DD} S = 1.8V				
		V _{REF} = DECOUPL, Pre-charge ON				
		V _{REF} = DECOUPL, Pre-charge OFF				
		V _{REF} = ADCREF				
	Output Voltage Range Load = COMP_A	V _{REF} = V _{DD} S = 3.8V, Code 1				V
		V _{REF} = V _{DD} S = 3.8V, Code 255				
		V _{REF} = V _{DD} S = 3.0V, Code 1				
		V _{REF} = V _{DD} S = 3.0V, Code 255				
		V _{REF} = V _{DD} S = 1.8V, Code 1				
		V _{REF} = V _{DD} S = 1.8V, Code 255				
		V _{REF} = DECOUPL, Pre-charge OFF, Code 1				
		V _{REF} = DECOUPL, Pre-charge OFF, Code 255				
		V _{REF} = DECOUPL, Pre-charge ON, Code 1				
		V _{REF} = DECOUPL, Pre-charge ON, Code 255				
		V _{REF} = ADCREF, Code 1				
		V _{REF} = ADCREF, Code 255				
	Output Voltage Range Load = COMP_B	V _{REF} = V _{DD} S = 3.8V, Code 1				V
		V _{REF} = V _{DD} S = 3.8V, Code 255				
		V _{REF} = V _{DD} S = 3.0V, Code 1				
		V _{REF} = V _{DD} S = 3.0V, Code 255				
		V _{REF} = V _{DD} S = 1.8V, Code 1				
		V _{REF} = V _{DD} S = 1.8V, Code 255				
		V _{REF} = DECOUPL, Pre-charge OFF, Code 1				
		V _{REF} = DECOUPL, Pre-charge OFF, Code 255				
		V _{REF} = DECOUPL, Pre-charge ON, Code 1				
		V _{REF} = DECOUPL, Pre-charge ON, Code 255				
		V _{REF} = ADCREF, Code 1				
		V _{REF} = ADCREF, Code 255				
External (R C) Load						
INL	Integral Non-Linearity	V _{REF} = V _{DD} S, F _{DAC} = 250 kHz				LSB
		V _{REF} = DECOUPL, F _{DAC} = 250 kHz				
		V _{REF} = ADCREF, F _{DAC} = 250 kHz				
DNL	Differential Non-Linearity ⁽¹⁾	V _{REF} = V _{DD} S, DECOUPL or ADCREF F _{DAC} = 250 kHz		±1		LSB

Table 5-12. Digital-to-Analog Converter (DAC) Characteristics (continued)
 $T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Offset Error		$V_{REF} = V_{DD5} = 3.8\text{V}$				LSB
		$V_{REF} = V_{DD5} = 3.0\text{V}$				
		$V_{REF} = V_{DD5} = 1.8\text{V}$				
		$V_{REF} = \text{DECOUPL, Pre-charge ON}$				
		$V_{REF} = \text{DECOUPL, Pre-charge OFF}$				
		$V_{REF} = \text{ADCREf}$				
Max Code Output Voltage Variation		$V_{REF} = V_{DD5} = 3.8\text{V}$				LSB
		$V_{REF} = V_{DD5} = 3.0\text{V}$				
		$V_{REF} = V_{DD5} = 1.8\text{V}$				
		$V_{REF} = \text{DECOUPL, Pre-charge ON}$				
		$V_{REF} = \text{DECOUPL, Pre-charge OFF}$				
		$V_{REF} = \text{ADCREf}$				
Output Voltage Range Load = COMP_B		$V_{REF} = V_{DD5} = 3.8\text{V}$, Code 1				V
		$V_{REF} = V_{DD5} = 3.8\text{V}$, Code 255				
		$V_{REF} = V_{DD5} = 3.0\text{V}$, Code 1				
		$V_{REF} = V_{DD5} = 3.0\text{V}$, Code 255				
		$V_{REF} = V_{DD5} = 1.8\text{V}$, Code 1				
		$V_{REF} = V_{DD5} = 1.8\text{V}$, Code 255				
		$V_{REF} = \text{DECOUPL, Pre-charge OFF, Code 1}$				
		$V_{REF} = \text{DECOUPL, Pre-charge OFF, Code 255}$				
		$V_{REF} = \text{DECOUPL, Pre-charge ON, Code 1}$				
		$V_{REF} = \text{DECOUPL, Pre-charge ON, Code 255}$				
		$V_{REF} = \text{ADCREf, Code 1}$				
		$V_{REF} = \text{ADCREf, Code 255}$				

5.14.3 Temperature and Battery Monitor

Table 5-13. Temperature Sensor

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, $V_{\text{DDS}} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		$^\circ\text{C}$
Accuracy	$-40\text{ }^\circ\text{C}$		4.4		$^\circ\text{C}$
Accuracy	$25\text{ }^\circ\text{C}$		1.9		$^\circ\text{C}$
Accuracy	$85\text{ }^\circ\text{C}$		1.8		$^\circ\text{C}$
Supply voltage coefficient ⁽¹⁾			3.8		$^\circ\text{C/V}$

(1) Automatically compensated when using supplied driver libraries.

Table 5-14. Battery Monitor

Measured on a Texas Instruments reference design with $T_c = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
INL (max)			23		mV
Accuracy	$V_{\text{DDS}} = 3.0\text{ V}$		22.5		mV
Offset error			-32		mV
Gain error			-1		%

5.14.4 Comparators

Table 5-15. Continuous Time Comparator

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DD5}	V
External reference voltage		0		V_{DD5}	V
Internal reference voltage ⁽¹⁾	Using internal DAC with V_{DD5} as reference voltage, DAC code = 0-255		0 - 2.78		V
Offset			± 4		mV
Hysteresis			< 2		mV

- (1) The comparator can use the output of an internal DAC as its reference. Reference voltages can be derived from V_{DD5} , DCOUPL (1.28V), and the internal ADC reference.

Table 5-16. Low-Power Clocked Comparator

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range		0		V_{DD5}	V
Clock frequency			SCLK_LF		
Internal reference voltage ⁽¹⁾	Using internal DAC with V_{DD5} as reference voltage, DAC code = 0-255		0 - 2.78		V

- (1) The comparator can use the output of an internal DAC as its reference. Reference voltages can be derived from V_{DD5} , DCOUPL (1.28V), and the internal ADC reference.

5.14.5 Current Source

Table 5-17. Programmable Current Source

$T_c = 25^\circ\text{C}$, $V_{DD5} = 3.0\text{ V}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range (logarithmic range)			0.25 to 20		μA
Resolution			0.25		μA
Current consumption ⁽¹⁾	Including current source at maximum programmable output		21		μA

- (1) Additionally, the bias module must be enabled when running in standby mode.

5.14.6 GPIO

Table 5-18. GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25°C, V_{DD5} = 1.8V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		1.54		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.25		V
GPIO VOH at 4-mA load	IOCURR = 1		1.58		V
GPIO VOL at 4-mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		68		μA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD5		18.5		μA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.72		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.36		V
T_A = 25°C, V_{DD5} = 3.0V					
GPIO VOH at 8-mA load	IOCURR = 2, high-drive GPIOs only		2.57		V
GPIO VOL at 8-mA load	IOCURR = 2, high-drive GPIOs only		0.45		V
GPIO VOH at 4-mA load	IOCURR = 1		2.61		V
GPIO VOL at 4-mA load	IOCURR = 1		0.40		V
T_A = 25°C, V_{DD5} = 3.8V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		265		μA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDD5		106		μA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.53		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.43		V
VIH	Lowest GPIO input voltage reliably interpreted as a <i>High</i>	0.8*V _{DD5} ⁽¹⁾			V
VIL	Highest GPIO input voltage reliably interpreted as a <i>Low</i>	0.2*V _{DD5} ⁽¹⁾			V

(1) Each GPIO is referenced to a specific VDD5 pin. See the technical reference manual listed in [Section 8.2](#) for more details.

6 Detailed Description

6.1 Overview

[Section 1.4](#) shows the core modules of the CC2652RB device.

6.2 System CPU

The CC2652RB SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
 - Data Watchpoint and Trace Unit (DWT)
 - JTAG Debug Access Port (DAP)
 - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
 - Instrumentation Trace Macrocell Unit (ITM)
 - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

6.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

6.3.1 Bluetooth 5 low energy

The RF Core offers full support for Bluetooth 5 low energy, including the high-speed 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5 stack or through a high-level Bluetooth API. The Bluetooth 5 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5 enables fast, reliable firmware updates.

6.3.2 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mcps per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

6.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the `cfg.c` source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16-KB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4-KB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

6.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still [ensuring ultra-low power](#)
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

[Sensor Controller Studio](#) is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or I²C (UART and I²C are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.
- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

6.6 Cryptography

The CC2652RB device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
 - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
 - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
 - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
 - Short Weierstrass form (full hardware support), such as:
 - NIST-P224, NIST-P256, NIST-P384, NIST-P521
 - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
 - secp256r1
 - Montgomery form (hardware support for multiplication), such as:
 - Curve25519
- **SHA2 based MACs**
 - HMAC with SHA224, SHA256, SHA384, or SHA512
- **Block cipher mode of operation**
 - AESCCM
 - AESGCM
 - AESECB
 - AESCBC
 - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC2652RB device.

6.7 Timers

A large selection of timers are available as part of the CC2652RB device. These timers are:

- **Real-Time Clock (RTC)**

A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF). This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.

- **General Purpose Timers (GPTIMER)**

The four flexible GPTIMERS can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERS are available in Active and Idle power modes.

- **Sensor Controller Timers**

The Sensor Controller contains 3 timers:

AUX Timer 0 and 1 are 16-bit timers with a 2^N prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.

- **Radio Timer**

A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.

- **Watchdog timer**

The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

6.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I²S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I²C interface is also used to communicate with devices compatible with the I²C standard. The I²C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in [Section 4](#). All digital peripherals can be connected to any digital pin on the device.

For more information, see the [CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual](#).

6.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2652RB device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

6.10 μDMA

The device includes a direct memory access (μDMA) controller. The μDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The μDMA controller can perform a transfer between memory and peripherals. The μDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the μDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

6.11 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

6.12 Power Management

To minimize power consumption, the CC2652RB supports a number of power modes and power management features (see [Table 6-1](#)).

Table 6-1. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	BAW or RCOSC_HF	BAW or RCOSC_HF	Off	Off	Off
2 MHz medium-speed clock (SCLK_MF)	RCOSC_MF	RCOSC_MF	Available	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Sensor Controller	Available	Available	Available	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see [Table 6-1](#)).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The [Sensor Controller Studio](#) tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

NOTE

The power, RF and clock management for the CC2652RB device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2652RB software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete [SDK](#) with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

6.13 Clock Systems

The CC2652RB device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF), the internal BAW resonator, or an external 48 MHz crystal (XOSC_HF). Radio operation requires either the internal BAW resonator or an external 48 MHz crystal.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, the internal BAW resonator, an external 48 MHz crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

6.14 Network Processor

Depending on the product configuration, the CC2652RB device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

7 Application, Implementation, and Layout

NOTE

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 LaunchPad™ Development Kit Reference Design

The [LaunchPad Development Kit](#) that supports the CC2652RB device also functions as a detailed reference design for schematic and layout.

CC2652RB LaunchPad™ Development Kit Design Files

The CC2652RB LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2652RB device.

Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag

The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:

- PCB antennas
- Helical antennas
- Chip antennas
- Dual band antennas for 868 and 915 MHz combined with 2.4 GHz

The antenna kit includes a μ SMA (JSC) cable to connect to the wireless LaunchPad Development Kits and SensorTags.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

8.1 Development Support

The CC2652RB device is supported by a variety of software and hardware development tools.

Development Kit

CC2652RB LaunchPad™ Development Kit

The CC2652RB LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2652RB SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy profile and helps to optimize it for ultra-low-power consumption. See [Table 3-1](#) for guidance in selecting the correct device for single-protocol products.

Software

SimpleLink™ CC13x2 and CC26x2 software development kit

The SimpleLink CC13x2 and CC26x2 Software Development Kit (SDK) provides a complete package for the development of Bluetooth-based applications for the CC2652RB wireless MCU. The SimpleLink CC13x2 and CC26x2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit <http://www.ti.com/simplelink>.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

Sensor Controller Studio

Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:

- Ready-to-use examples for several common use cases
- Full toolchain with built-in compiler and assembler for programming in a C-like programming language
- Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms

CCS UniFlash

CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

8.2 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2652RB. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer

Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2652RB Silicon Errata

The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

Getting Started With the CC13XX and CC26XX Sensor Controller

The application note is an introduction to the low-power Sensor Controller in the CC2652RB device. It explains the benefits of using the Sensor Controller in various use cases and demonstrates how low power consumption is achievable when using the Sensor Controller.

Technical Reference Manual (TRM)

CC13x2, CC26x2 SimpleLink™ Wireless MCU TRM

The TRM provides a detailed description of all modules and peripherals available in the device family.

8.2.1 TI SimpleLink™

TI's new SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

8.2.2 TI Design Network

The TI Design Network is a worldwide community of respected, well-established companies offering products and services that complement TI's semiconductor device solutions. Products and services include a broad range of reference designs, turnkey products and services, system modules, embedded software, engineering services, and development tools that help customers accelerate development efforts and reduce time-to-market.

Search the network on www.ti.com/3p to find a suitable partner for modules, engineering services, or development tools.

8.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

TI Embedded Processors Wiki Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.4 Trademarks

SmartRF, SimpleLink, LaunchPad, EnergyTrace, Code Composer Studio, E2E are trademarks of Texas Instruments.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2652RB1FRGZR	PREVIEW	VQFN	RGZ	48	2500	TBD	Call TI	Call TI	-40 to 85		
XCC2652RBRGZR	ACTIVE	VQFN	RGZ	48	2500	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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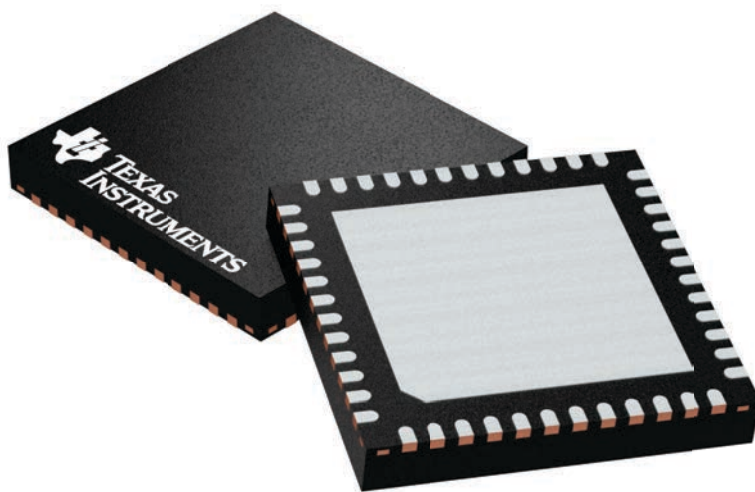
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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