UNITRODE

UC1904
UC2904
UC3904

Precision Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring Up to Four Supply Voltages
- Two Inputs Preset for -5V and -12V Monitoring, or Programmable Positive Levels
- Precision 2.5V Reference
- Separate Inputs for Over-Current and Line Fault Sensing
- Adjustable Under- to Over-Voltage Fault Windows
- Latched Over-Voltage and Over-Current Output
- Power Good and Power Warning Outputs
- Auto Restart Function with ON/OFF Control, and Programmable Delay
- Programmable Pwr On Reset Delay

DESCRIPTION

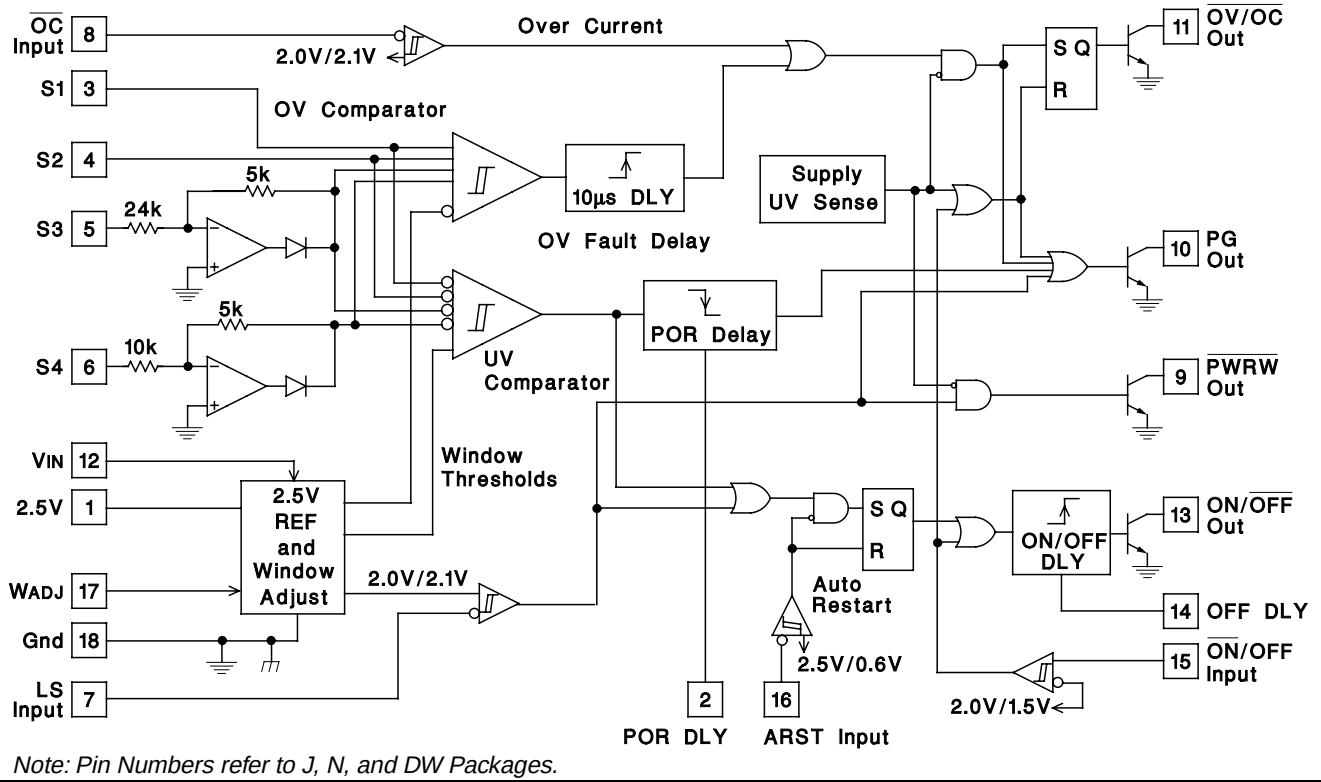
The UC1904 Quad Supply Monitor will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. Four independent positive voltages can be monitored or, alternatively, two of the sense inputs are preset to monitor -5V and -12V supplies. The device also monitors Over-Current and Line Sense inputs, both with precision input thresholds.

Four open collector outputs on the UC1904 give the following responses: 1. The $\overline{OV}/\overline{OC}$ output is a latched over-voltage, or over-current response. 2. A Power Good signal responds low with any fault detection – on power-up a programmable delay is used to hold this output low for a system Power On Reset signal. 3. The $\overline{PWRW}$ output responds only to a Line Sense input, for early warning of power failures. 4. The last open collector, the ON/$\overline{OFF}$ output, generates a delayed supply OFF control signal in response to an OFF input command, under-voltage condition, or line fault detection.

The OV-UV fault window is adjustable with a programming input. The thresholds are centered around the precision 2.5V reference, with a scaled hysteresis for precise, glitch free operation. In the positive mode of operation, the fault windows at each of the sense inputs can be independently scaled using external resistors and the 2.5V reference output. An Auto Restart function couples with the under-voltage and line sensing circuits to allow controlled power supply start-up and shutdown.

This device will operate over a supply range of 4.75V to 18V. The device is available in a DIP, SOIC, or PLCC outline. This device is ESD protected on all pins.

BLOCK DIAGRAM



Note: Pin Numbers refer to J, N, and DW Packages.

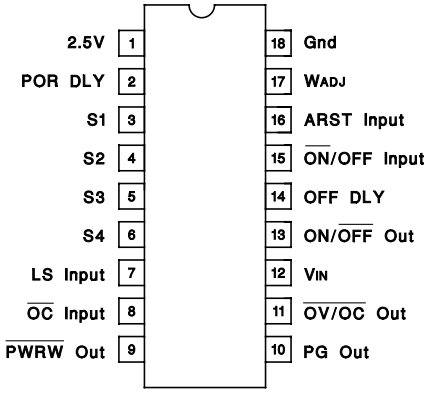
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage 20V
Sense Inputs, S1 And S2, Other Analog And Logic Inputs
  Maximum Forced Voltage . . . . . -0.3V to 10V
  Maximum Forced Current . . . . . ±10mA
Sense Input S3, (-12V Sense Input)
  Maximum Forced Voltage . . . . . -18V to 10V
  Maximum Forced Current . . . . . ±10mA
Sense Input S4, (-5V Sense Input)
  Maximum Forced Voltage . . . . . -10V to 10V
  Maximum Forced Current . . . . . ±10mA
Open Collector Outputs
  Maximum Voltage 20V
  Maximum Current 50mA
Reference Output Current . . . . . Internally Limited
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C

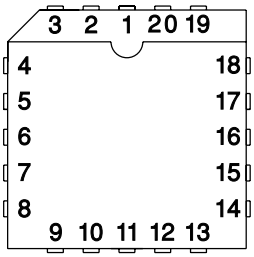
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N PACKAGE, DW PACKAGE



PLCC-20 (TOP VIEW)
Q PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
2.5V	1
POR DLY	2
N.C.	3
S1	4
S2	5
S3	6
S4	7
N.C.	8
LS Input	9
$\overline{OC}$ Input	10
$\overline{PWRW}$ Out	11
PG Out	12
$\overline{OV/OC}$ Out	13
VIN	14
ON/$\overline{OFF}$ Out	15
OFF DLY	16
$\overline{ON}$/OFF Input	17
ARST Input	18
WADJ	19
Gnd	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +V_{IN} = 15V, W_{ADJ} = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	VIN = 15V		3.2	4.5	mA
VIN UVLO Threshold	Low to High		4.5	4.75	V
UVLO Threshold Hysteresis			50		mV
Minimum VIN to Enable PG Out			0.8	1.5	V
Reference					
Output Voltage(VREF)	TJ = 25°C	2.475	2.5	2.525	V
	Over Temperature, UC3904	2.47		2.53	V
	Over Temperature, UC2904 & UC1904	2.465		2.535	V
Load Regulation	IOUT = 0 to 4mA			6	mV
Line Regulation	VIN = 4.75 to 18V			5	mV
Short Circuit Current	VREF = 0V		17		mA
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds					
Over-Voltage Thresholds S1, S2	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	140	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	270	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	540	mV
Over-Voltage Thresholds S3, S4 Positive Mode	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	145	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	280	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	550	mV

ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, $+V_{IN}$ = 15V, W_{ADJ} = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds (cont.)					
Under-Voltage Thresholds S1, S2	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-140	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-270	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-540	-500	-460	mV
Under-Voltage Thresholds S3, S4 Positive Mode	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-150	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-285	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-555	-500	-460	mV
OV and UV Threshold Hysteresis	As a Function of W_{ADJ}	30	50	70	mV/V
S3 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-13.52	-13.2	-12.88	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-11.06	-10.8	-10.54	V
	Hysteresis, W_{ADJ} = 0.5V	80	120	160	mV
S4 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-5.63	-5.5	-5.37	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-4.61	-4.5	-4.39	V
	Hysteresis, W_{ADJ} = 0.5V	30	50	70	mV
W_{ADJ} Input Bias Current	0.25V < W_{ADJ} <1.0V	-5		5	µA/V
LS Threshold	Input = H to L	1.96	2	2.04	V
	Threshold hysteresis	65	100	125	mV
$\overline{OC}$ Threshold	Input = H to L	1.9	2	2.1	V
	Threshold hysteresis	50	100	150	mV
ARST Input Threshold	Input = L to H	2.25	2.5	2.75	V
	Input = H to L	0.56	0.625	0.69	V
$\overline{ON}$/OFF Input Threshold	Input high level		1.74	2.4	V
	Input low level	0.6	1.35		V
Sense and Logic Input Bias Currents					
Sense 1-4, Positive Mode	Input = 2.8V		250	800	nA
	Input = 2.2V	-1000	-250		nA
Sense 3 Negative Mode	Input = -12V	-700	-500	-300	µA
Sense 4 Negative Mode	Input = -5V	-700	-500	-300	µA
Line, and OC Inputs	Input = 2.2V		300	1000	nA
$\overline{ON}$/OFF Input	Input = 2.5V		150	600	nA
ARST Input	Input = 0.5	-2000	-700		nA
Open Collector Outputs ($\overline{OV}$/$\overline{OC}$ Out, PG Out, $\overline{PWRW}$ Out, ON/$\overline{OFF}$ Out)					
Saturation Voltage	I_{OUT} = 10mA		0.2	0.4	V
Leakage current	V_{OUT} = 20V			5	µA
POR Delay					
Delay		160	250	350	ms/µF
Internal Pullup Current			9		µA
Threshold Low to High			2.25		V
OFF Delay					
Delay		120	185	250	ms/µF
Internal Pullup current			12		µA
Threshold Low to High			2.25		V
OV Fault Delay					
Delay		10	20	50	µs

PIN FUNCTIONAL DESCRIPTION

2.5V: This is the output of the precision 2.5V reference.

ARST Input: This input, with a 4:1 hysteretic threshold, is used to sequence a power system through the **A**uto **R**e**S**tar**T** cycle. A delayed representation of a supply output voltage is used at this pin to provide adequate startup time for the power system, and a minimum power-off period.

Gnd: Reference point for the internal reference and all thresholds, as well as the return for the remainder of the device.

LS Input: The **L**ine **S**ense input is used to monitor a voltage that varies with the input line voltage to a system. The input is compared to a precision 2.0V level and is used to activate the $\overline{\text{PWRW}}$ and PG outputs, as well as triggering the Auto Restart sequence.

$\overline{\text{OC}}$ Input: The **O**ver-**C**urrent input can be used to respond to an inverted over-current signal. A low level signal at this input latches in a fault indication at the **$\overline{\text{OV}}$/$\overline{\text{OC}}$** output.

OFF DLY: This pin functions similarly to the **POR DLY** pin to delay the turn-on of the ON/$\overline{\text{OFF}}$ output transistor. The charging current and upper threshold are 12µA and 2.1V.

ON/$\overline{\text{OFF}}$ Input: With a high level at this input the **ON/$\overline{\text{OFF}}$ Out** pin is activated after a user-programmable delay. A high level also activates the **PG Out** pin, and resets the **OV/$\overline{\text{OC}}$** fault latch.

On/$\overline{\text{Off}}$ Out: This output is an open collector output that is activated by the **ON/$\overline{\text{OFF}}$ Input**, or the Auto Restart circuitry. Saturation voltage on this and all the open collector outputs is rated at 10mA of current.

$\overline{\text{OV}}$/$\overline{\text{OC}}$ Out: In response to either an **O**ver-**V**oltage or **O**ver-**C**urrent situation this output is latched active low. There is nominal 20µs delay in the OV path to the fault latch, providing rejection to transient overshooting on the monitored voltages. The low condition is cleared when the fault latch is reset by the **ON/$\overline{\text{OFF}}$ Input**, or a **UVLO** condition on the device.

POR DLY: This pin is used, with an external capacitor, to program a **P**ower-**O**n-**R**eset delay. This delay is reset whenever there is a UV condition at one of the S1-S4 inputs, and then triggered upon the clearing of the UV condition. When reset, the voltage across the capacitor is quickly discharged to near zero volts, and the **PG Out** pin goes active low. Once triggered the capacitor is charged by a 9µA current source. The **PG Out** pin remains active low until the delay capacitor voltage reaches a 2.1V threshold.

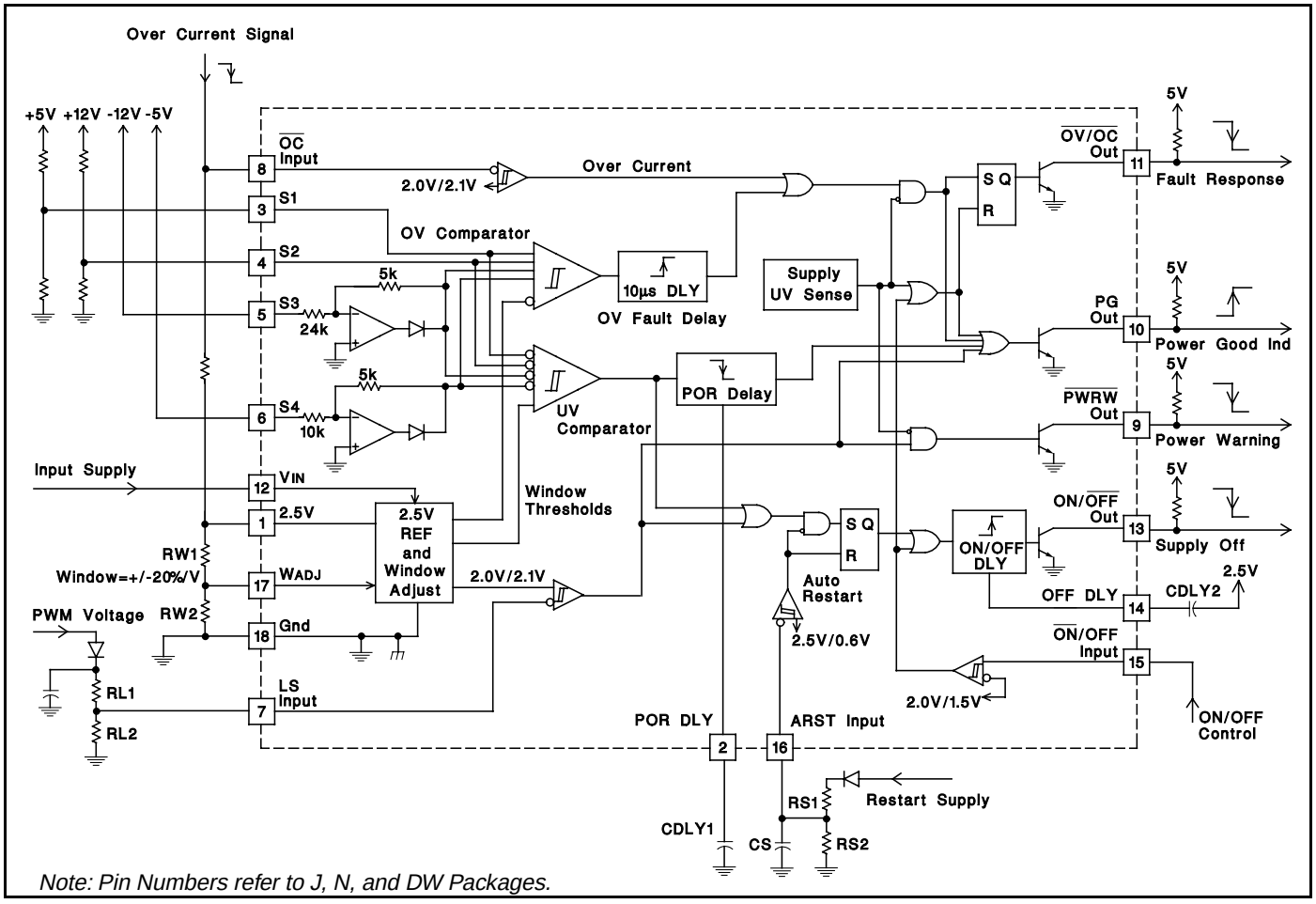
PG Out: During any fault, under-voltage, or UVLO condition this output is low. A **P**ower **G**ood indication (output off) is given when all supply conditions are within defined operating limits. During power-up the **PG** signal is delayed by a programmable **P**ower **O**n **R**eset delay. During **UVLO** the output is active low as long as the input supply, **V_{IN}**, is above approximately 1.0V.

$\overline{\text{PWRW}}$ Out: When a low line condition is sensed by the **LS Input** this output goes low. This output is disabled (off) during a **UVLO** condition.

S1-S4: These are the sense inputs for OV and UV monitoring of external voltages. All four inputs can be used to sense positive voltages with a simple divider to scale the voltage level to the 2.5V centered window. The **S3** and **S4** inputs can also be used to sense -12V and -5V supplies respectively with no external components. This is done with internal precision resistor dividers and two source only op-amps that are disabled when the pins are used in the positive mode.

V_{IN}: Input supply for the UC1904. The device is operational with 4.75V to 18V on this pin.

W_{ADJ}: The **W_{ADJ}** input is used to program the OV and UV window thresholds. The OV-UV window is centered around the 2.5V reference and is nominally ±20% per volt on the **W_{ADJ}** input pin.



Note: Pin Numbers refer to J, N, and DW Packages.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC2904DW	OBSOLETE	SOIC	DW	18		TBD	Call TI	Call TI
UC2904DWTR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC2904N	OBSOLETE	PDIP	N	18		TBD	Call TI	Call TI
UC2904Q	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI
UC2904QTR	OBSOLETE	PLCC	FN	20		TBD	Call TI	Call TI
UC3904DW	OBSOLETE	SOIC	DW	18		TBD	Call TI	Call TI
UC3904DWTR	OBSOLETE	SOIC	DW	18		TBD	Call TI	Call TI
UC3904N	OBSOLETE	PDIP	N	18		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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