Adaptive Power MOSFET Driver[1]

FEATURES

- dv/dt and di/dt Control
- Undervoltage Protection
- Short-Circuit Protection
- t_{rr} Shoot-Through Current Limiting
- Low Quiescent Current
- CMOS Compatible Inputs
- Compatible with Wide Range of MOSFET Devices
- Bootstrap and Charge Pump Compatible (High-Side Drive)

DESCRIPTION

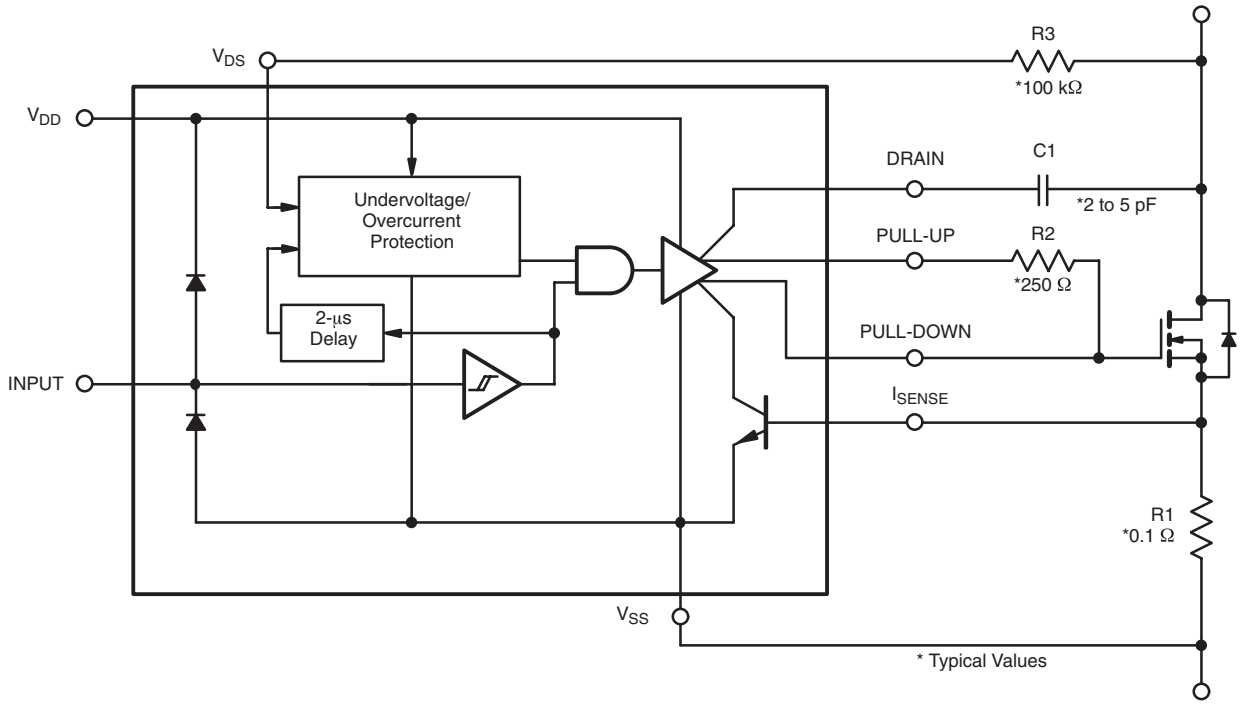
The Si9910 Power MOSFET driver provides optimized gate drive signals, protection circuitry and logic level interface. Very low quiescent current is provided by a CMOS buffer and a high-current emitter-follower output stage. This efficiency allows operation in high-voltage bridge applications with “bootstrap” or “charge-pump” floating power supply techniques.

The non-inverting output configuration minimizes current drain for an n-channel “on” state. The logic input is internally diode clamped to allow simple pull-down in high-side drives.

Fault protection circuitry senses an undervoltage or output short-circuit condition and disables the power MOSFET. Addition of one external resistor limits maximum di/dt of the external Power MOSFET. A fast feedback circuit may be used to limit shoot-through current during t_{rr} (diode reverse recovery time) in a bridge configuration.

The Si9910 is available in both standard and lead (Pb)-free 8-pin plastic DIP and SOIC packages which are specified to operate over the industrial temperature range of –40°C to 85°C.

FUNCTIONAL BLOCK DIAGRAM



1. Patent Number 484116.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V_{SS} Pin

V_{DD} Supply Range ..... −0.3 V to 18 V

Pin 1, 4, 5, 7, 8 ..... −0.3 V to V_{DD} + 0.3 V

Pin 2 ..... −0.7 V to V_{DD} + 0.3 V

Input Current ..... ±20 mA

Peak Current (I_{pk}) ..... 1 A

Storage Temperature ..... −65 to 150°C

Operating Temperature ..... −40 to 85°C

Junction Temperature (T_J) ..... 150°C

Power Dissipation (Package)[a]

8-Pin SOIC (Y Suffix)[b] ..... 700 mW

8-Pin Plastic DIP (J Suffix)[b] ..... 700 mW

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 5.6 mW/°C above 25°C.

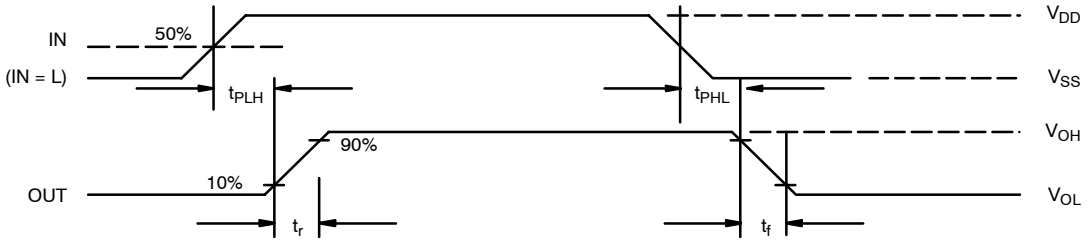
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{DD} 10.8 V to 16.5 V T_A = OperatingTemperature Range	Limits Min[c]	Limits Typ[b]	Limits Max[c]	Unit
Input						
High Level Input Voltage	V_{IH}		0.70 x V_{DD}	7.4		V
Low Level Input Voltage	V_{IL}			6.0	0.35 x V_{DD}	V
Input Voltage Hysteresis	V_h		0.90	2.0	3.0	V
High Level Input Current	I_{IH}	V_{IN} = V_{DD}			±1	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V			±1	µA
Output						
High Level Output Voltage	V_{OH}	I_{OH} = −200 mA	V_{DD} −3	10.7		V
Low Level Output Voltage	V_{OL}	I_{OL} = 200 mA		1.3	3	V
Undervoltage Lockout	V_{UVLO}		8.3	9.2	10.6	V
I_{SENSE} Pin Threshold	V_{TH}	Max I_S = 2 mA, Input High 100 mV Change on Drain	0.5	0.66	0.8	V
Voltage Drain-Source Maximum	V_{DS}	Input High	8.3	9.1	10.2	V
Input Current for V_{DS} Input	I_{VDS}			12	20.0	µA
Peak Output Source Current	I_{OS+}			1		A
Peak Output Sink Current	I_{OS-}			−1		A
Supply						
Supply Range	V_{DD}		10.8		16.5	V
Supply Current	I_{DD1}	Output High, No Load		0.1	1	µA
	I_{DD2}	Output Low, No Load		100	500	µA
Dynamic						
Propagation Delay Time Low to High Level	t_{PLH}	C_L = 2000 pF		120		ns
Propagation Delay Time High to Low Level	t_{PHL}			135		ns
Rise Time	t_r			50		ns
Fall Time	t_f			35		ns
Overcurrent Sense Delay (V_{DS})	t_{DS}			1		µS
Input Capacitance	C_{in}			5		pF

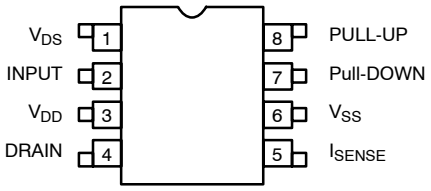
Notes
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.

AC TESTING CONDITIONS



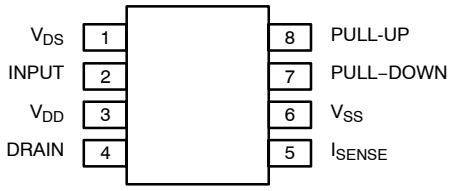
PIN CONFIGURATIONS AND ORDERING INFORMATION

PDIP-8



Top View

SOIC-8



Top View

ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9910DY	–40 to 85°C	SOIC-8
Si9910DY-T1		
Si9910DY-T1—E3		
Si9910DJ		PDIP-8
Si9910DJ—E3		

PIN DESCRIPTION

Pin 1: V_{DS}

Pin 1 or V_{DS} is a sense input for the maximum source-drain voltage limit. Two microseconds after a high transition on input pin 2, an internal timer enables the $V_{DS(max)}$ sense circuitry. A catastrophic overcurrent condition, excessive on-resistance, or insufficient gate-drive voltage can be sensed by limiting the maximum voltage drop across the power MOSFET. An external resistor (R3) is required to protect pin 1 from overvoltage during the MOSFET "off" condition. Exceeding $V_{DS(max)}$ latches the Si9910 "off." Drive is re-enabled on the next positive- going input on pin 2. If pin 1 is not used, it must be connected to pin 6 (V_{SS}).

Pin 2: INPUT

A non-inverting, Schmidt trigger input controls the state of the MOSFET gate-drive outputs and enables the protection logic. When the input is low ($\leq V_{IL}$), V_{DD} is monitored for an undervoltage condition (insufficiently charged bootstrap capacitor). If an undervoltage ($\leq V_{DD(min)}$) condition exists, the driver will ignore a turn-on input signal. An undervoltage ($\leq V_{DD(min)}$) condition during an "on" state will not be sensed.

Pin 3: V_{DD}

V_{DD} supplies power for the driver's internal circuitry and charging current for the power MOSFET's gate capacitance. The Si9910 minimizes the internal I_{DD} in the "on" state (gate-drive outputs high) allowing a "floating" power supply to be provided by charge pump or bootstrap techniques.

Pin 4: DRAIN

Drain is an analog input to the internal dv/dt limiting circuitry. An external capacitor (C1) must be used to protect the input from exposure to the high-voltage ("off" state) drain and to set the power MOSFET's maximum rate of dv/dt. If dv/dt feedback is not used, pin 4 must be left open.

Pin 5: I_{SENSE}

I_{SENSE} in combination with an external resistor ($R_{1)}$ protects the power MOSFET from potentially catastrophic peak currents. I_{SENSE} is an analog feedback that limits current during the power MOSFET's transition to an "on" state. It is intended to protect power MOSFETs (in a half-bridge arrangement) from "shoot-through" current, resulting from excess di/dt and t_{rr} of flyback diodes or from logic timing overlap. An 0.8-V drop across (R1) should indicate a current level that is approximately four times the maximum allowable load current. When the I_{SENSE} input is not used, it should be tied to pin 6 (V_{SS}).

Pin 6: V_{SS}

V_{SS} is the driver's ground return pin. The applications diagram illustrates the connection of V_{SS} for source-referenced "floating" applications (half-bridge, high-side) and ground-referenced applications (half-bridge, low-side).

Pin 7: PULL-DOWN
Pin 8: PULL-UP

Pull-up and pull-down outputs collectively provide the power MOSFET gate with charging and discharging currents. Turn "on" or "off" di/dt can be limited by adding resistance (R_2) in series with the appropriate output.

APPLICATIONS

"Floating" High-Side Drive Applications

As demonstrated in Figure 1, the Si9910 is intended for use as both a ground-referenced gate driver and as a "high-side" or source-referenced gate driver in half-bridge applications. Several features of the Si9910 permit its use in half-bridge high-side drive applications.

A simple and inexpensive method of isolating a floating supply to power the Si9910 in high-side driver applications had to be provided. Therefore, the Si9910 was designed to be compatible with two of the most commonly used floating supply techniques: the bootstrap and the charge pump. Both of these techniques have limitations when used alone. A properly designed bootstrap circuit can provide low-impedance drive which minimizes transition losses and the charge pump circuit provides static operation.

The Si9910 is configured to take advantage of either floating supply technique if the application is not sensitive to their particular limitations, or both techniques if switching losses must be minimized and static operation is necessary. The schematic above illustrates both the charge pump and bootstrap circuits used in conjunction with an Si9910 in a high-side driver application.

Input signal level shifting is accomplished with a passive pull-up (R4) and n-channel MOSFET (Q2) for pull-down in applications below 500 V. Total node capacitance defines the value of R4 needed to guarantee an input transition rate which safely exceeds the maximum dv/dt rate of the output half-bridge. Using level-shift devices with higher current capabilities may necessitate the addition of current-limiting components such as R5.

Bootstrap Undervoltage Lockout

When using a bootstrap capacitor as a high-side floating supply, care must be taken to ensure time is available to recharge the bootstrap capacitor prior to turn-on of the high-side MOSFET. As a catastrophic protection against abnormal conditions such as start-up, loss of power, etc., an internal voltage monitor has been included which monitors the bootstrap voltage when the Si9910 is in the low state. The Si9910 will not respond to a high input signal until the voltage on the bootstrap capacitor is sufficient to fully enhance the power MOSFET gate. For more details, please refer to Application Note AN705.

APPLICATION CIRCUIT

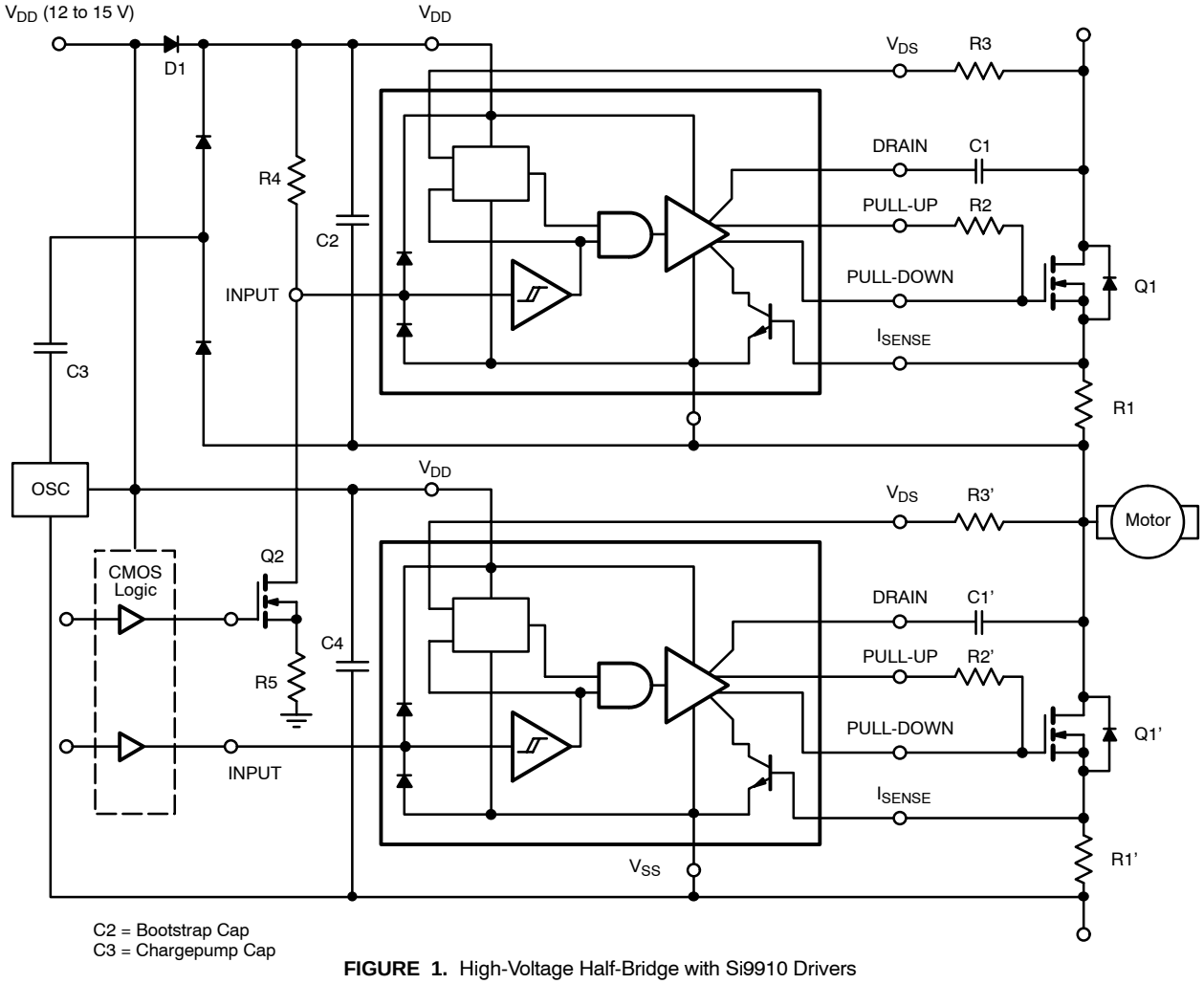
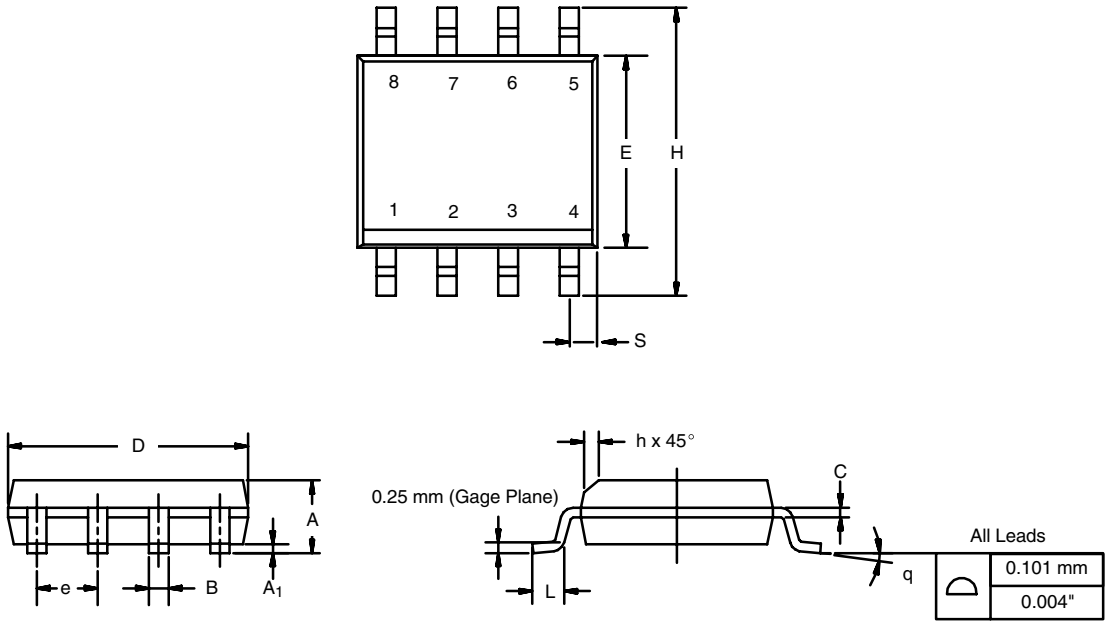


FIGURE 1. High-Voltage Half-Bridge with Si9910 Drivers

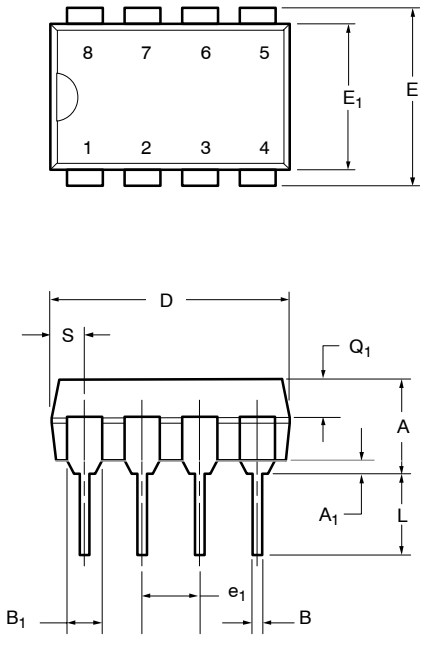
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SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

PDIP: 8-LEAD (POWER IC ONLY)



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	9.02	10.92	0.355	0.430
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.76	1.65	0.030	0.065

ECN: S-40081—Rev. A, 02-Feb-04
DWG: 5918

NOTE: End leads may be half leads.

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