High Efficiency, Synchronous, 4-Switch Buck-Boost Controller

FEATURES

- **Single Inductor Architecture Allows V_{IN} Above, Below or Equal to Regulated V_{OUT}**
- **Programmable Input or Output Current Feedback Loop**
- **Wide V_{IN} Range: 4V to 38V**
- **1% Output Voltage Accuracy: 0.8V < V_{OUT} < 38V**
- **Synchronous Rectification: Up to 98% Efficiency**
- **Current Mode Control**
- Phase-Lockable Fixed Frequency: 200kHz to 600kHz
- No Reverse Current During Start-Up
- Power Good Output Voltage Monitor
- Internal 5.5V LDO
- Quad N-Channel MOSFET Synchronous Drive
- V_{OUT} Disconnected from V_{IN} During Shutdown
- Adjustable Soft-Start Output Ramping
- Available in 28-Lead QFN (4mm × 5mm) and 28-Lead SSOP Packages

APPLICATIONS

- Automotive Systems
- Distributed DC Power Systems
- High Power Battery-Operated Devices
- Industrial Control

DESCRIPTION

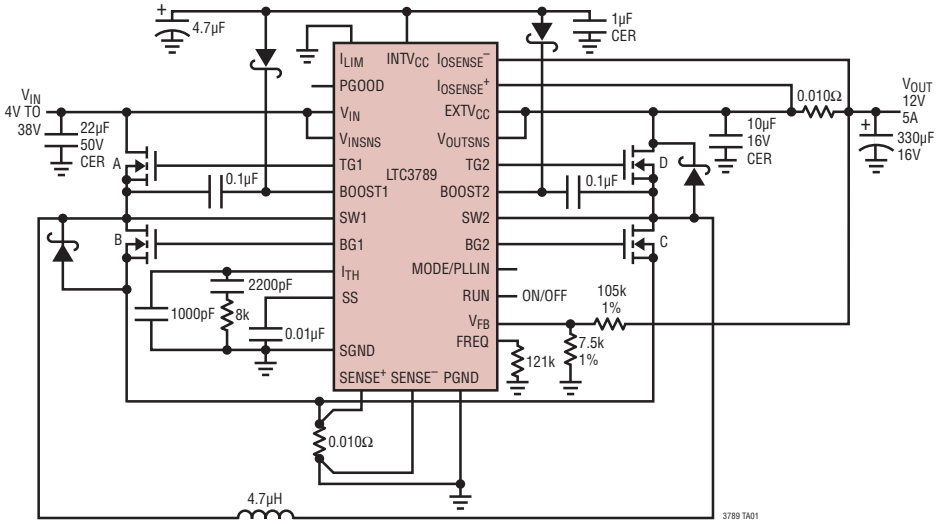
The LTC®3789 is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The constant-frequency, current mode architecture allows a phase-lockable frequency of up to 600kHz, while an output current feedback loop provides support for battery charging. With a wide 4V to 38V (40V maximum) input and output range and seamless, low noise transitions between operating regions, the LTC3789 is ideal for automotive, telecom and battery-powered systems.

The operating mode of the controller is determined through the MODE/PLLIN pin. The MODE/PLLIN pin can select between pulse-skipping mode and forced continuous mode operation and allows the IC to be synchronized to an external clock. Pulse-skipping mode offers the lowest ripple at light loads, while forced continuous mode operates at a constant frequency for noise-sensitive applications.

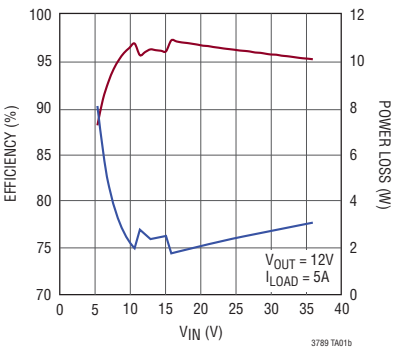
A power good output pin indicates when the output is within 10% of its designed set point. The LTC3789 is available in low profile 28-pin 4mm × 5mm QFN and narrow SSOP packages.

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TYPICAL APPLICATION



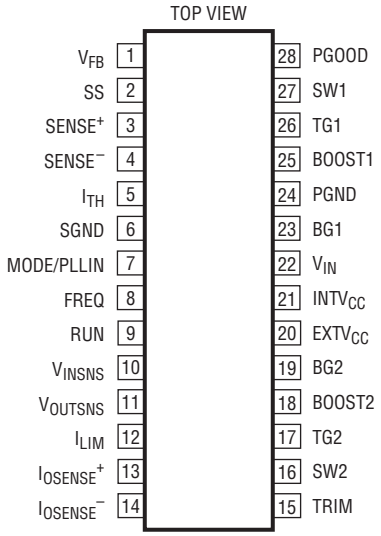
Efficiency and Power Loss



ABSOLUTE MAXIMUM RATINGS (Note 1)

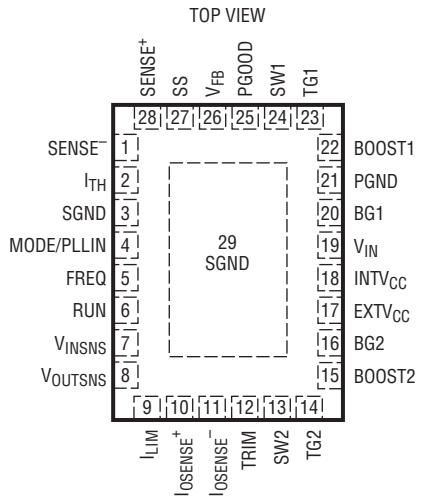
Input Supply Voltage (V_{IN}) ..... 40V to –0.3V
Topside Driver Voltages
(BOOST1, BOOST2) ..... 46V to –0.3V
Switch Voltage (SW1, SW2) ..... 40V to –5V
Current Sense Voltages (I_{OSENSE}^+, I_{OSENSE}^-)...40V to –0.3V
BOOST1, BOOST2 – SW1, SW2..... 6V to –0.3V
TG1, TG2 – SW1, SW2..... 6V to –0.3V
$EXTV_{CC}$ Voltage..... 14V to –0.3V
$INTV_{CC}$ Voltage..... 6V to –0.3V
$SENSE^+$, $SENSE^-$ Voltages ..... $INTV_{CC}$ to –0.3V
MODE/PLLIN, SS Voltages ..... $INTV_{CC}$ to –0.3V
V_{INSNS}, V_{OUTSNS}..... 40V to –0.3V
BG1, BG2 Voltages ..... $INTV_{CC}$ to –0.3V
I_{TH}, FREQ, I_{LIM} Voltages..... $INTV_{CC}$ to –0.3V
V_{FB} Voltage..... 2.7V to –0.3V
RUN, PGOOD Voltage ..... 6V to –0.3V
Operating Junction Temperature Range
(Notes 2, 3)..... –40°C to 125°C
Storage Temperature Range..... –65°C to 125°C
$INTV_{CC}$ Peak Output Current 100mA
Lead Temperature (Soldering, 10 sec.)
GN Package..... 300°C

PIN CONFIGURATION



GN PACKAGE
28-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 80°C/W



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 29) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3789EGN#PBF	LTC3789EGN#TRPBF	LTC3789	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3789IGN#PBF	LTC3789IGN#TRPBF	LTC3789	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3789EUFD#PBF	LTC3789EUFD#TRPBF	3789	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3789IUFD#PBF	LTC3789IUFD#TRPBF	3789	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Supply Voltage			4		38	V
V_{OUT}	Output Voltage			0.8		38	V
V_{FB}	Regulated Feedback Voltage	I_{TH} Voltage = 1.2V (Note 4), T_A = –40°C to 85°C I_{TH} = 1.2V, T_A = 125°C, T_A = –40°C to 125°C	● ●	0.792 0.788	0.800 0.800	0.808 0.812	V V
I_{FB}	Feedback Current	(Note 4)			–15	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4V to 38V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage = 1.4V to 2V Measured in Servo Loop, ΔI_{TH} Voltage = 2V to 2.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 5µA (Note 4)			1.5		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	 (Note 5) V_{RUN} = 0V			 3 40	 60	 mA µA
UVLO	Undervoltage Lockout	$INTV_{CC}$ Ramping Down			3.4	3.6	V
UVLO Hyst	Undervoltage Hysteresis				0.4		V
I_{SENSE^+} I_{SENSE^-}	SENSE Pins Current	V_{SENSE^-} = V_{SENSE^+} = 0V			0.2	±1	µA
$I_{IOSENSE^+}$ $I_{IOSENSE^-}$	I_{OSENSE} Pins Current	$V_{IOSENSE^-}$ = $V_{IOSENSE^+}$ = 10V			10	14	µA
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		2	3	4	µA
$V_{RUN(ON)}$	RUN Pin On-Threshold	V_{RUN} Rising			1.22		V
$V_{RUN(HYS)}$	RUN Pin On-Hysteresis				150		mV
I_{RUN}	RUN Pin Source Current				1.2		µA
$I_{RUN(HYS)}$	RUN Pin Hysteresis Current				5		µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold Buck Region Boost Region	 V_{FB} = 0.7V V_{FB} = 0.7V	 ● ●	 60 110	 90 140	 110 165	 mV mV
$V_{SENSE(IAVG)}$	Maximum Input/Output Average Current Sense Threshold	I_{LIM} = 0V I_{LIM} Floating I_{LIM} = $INTV_{CC}$		47 90 130	50 100 145	53 106 160	mV mV mV
$R_{DSPFET(ON)}$	Driver Pull-Up On-Resistance				2.6		Ω
$R_{DSNFET(ON)}$	Driver Pull-Down On-Resistance				1.5		Ω
TG t_r TG t_f	Top Gate Rise Time Top Gate Fall Time				25 25		ns ns
BG t_r BG t_f	Bottom Gate Rise Time Bottom Gate Fall Time				25 25		ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			60		ns
BG/TG t_{1D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver (Note 6)			60		ns
$DF_{MAX,BOOST}$	Maximum Duty Factor	% Switch C On			90		%
$D_{ON(MIN,BOOST)}$	Minimum Duty Factor for Main Switch in Boost Operation	% Switch C On			9		%
$D_{ON(MIN,BUCK)}$	Minimum Duty Factor for Main Switch in Buck Operation	% Switch B On			9		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVIN}$	Internal V_{CC} Voltage	6.5V < V_{IN} < 40V, V_{EXTVCC} = 0V		5.2	5.5	5.8	V
V_{LDOVIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 0V			0.2	1.0	%
$V_{INTVCCEXT}$	Internal V_{CC} Voltage	6.5V < V_{EXTVCC} < 14V		5.2	5.5	5.8	V
V_{LDOEXT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, V_{EXTVCC} = 12V			0.2	1.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{CC} = 0mA to 20mA, $EXTV_{CC}$ Ramping Positive		4.7	4.8		V
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				0.25		V
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V, R_{FREQ} = 1.22k		350	400	440	kHz
f_{LOW}	Low Fixed Frequency	V_{FREQ} = 0V		175	200	225	kHz
f_{HIGH}	High Fixed Frequency	V_{FREQ} = 2.4V		570	640	710	kHz
f_{SYNC}	Synchronizable Frequency	MODE/PLLIN = External Clock	●	200		600	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				220		kΩ
I_{FREQ}	Frequency Setting Current			8	10	12	µA
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3789 is tested under pulse load conditions such that $T_J \approx T_A$. The LTC3789E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3789I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3789GN: $T_J = T_A + (P_D \bullet 80°C/W)$

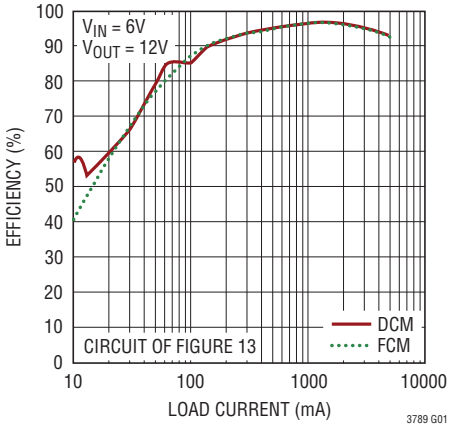
LTC3789UFD: $T_J = T_A + (P_D \bullet 34°C/W)$

Note 4: The LTC3789 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

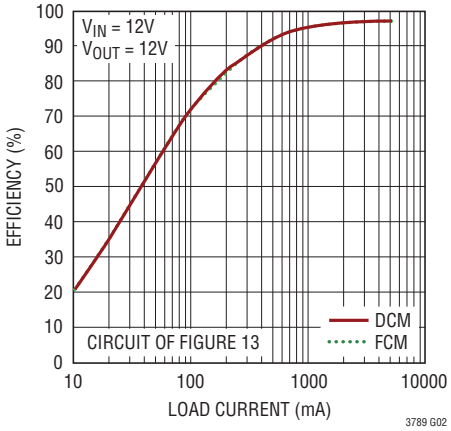
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

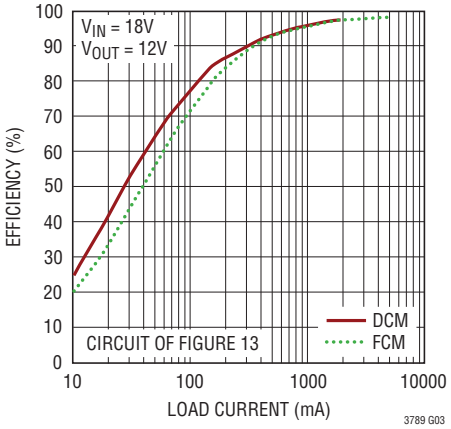
Efficiency vs Output Current (Boost Region)



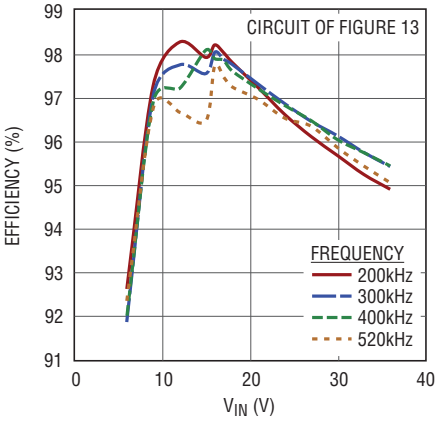
Efficiency vs Output Current (Buck-Boost Region)



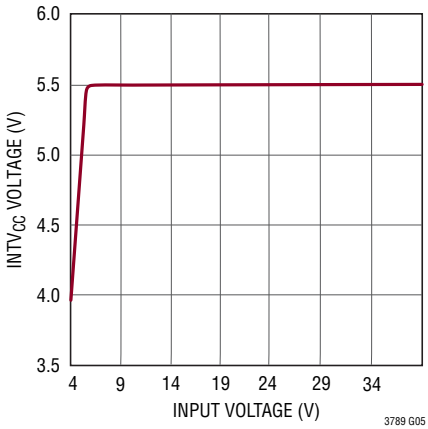
Efficiency vs Output Current (Buck Region)



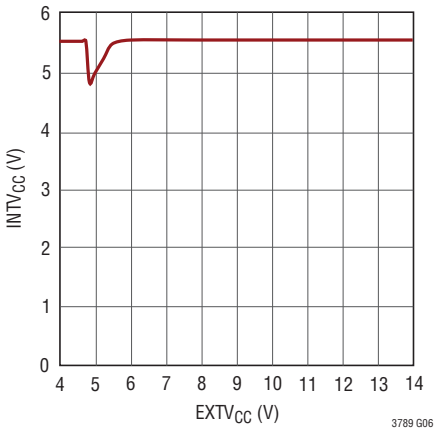
Efficiency vs V_{IN}



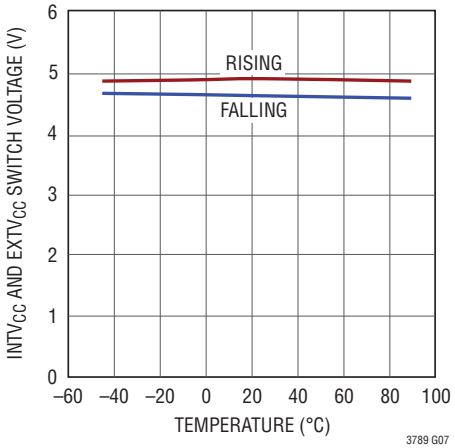
Internal 5.5V LDO Line Regulation



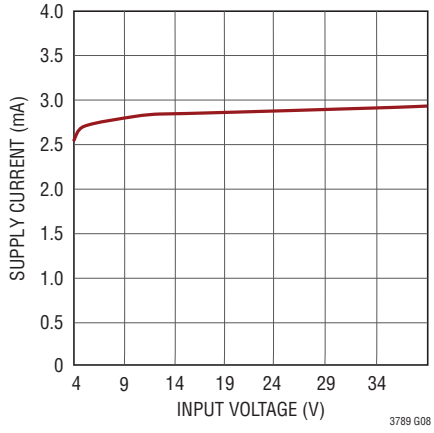
$EXTV_{CC}$ LDO Line Regulation



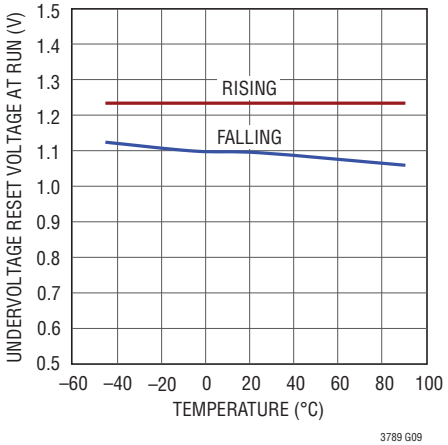
$INTV_{CC}$ and $EXTV_{CC}$ Switch Voltage vs Temperature



Supply Current vs Input Voltage

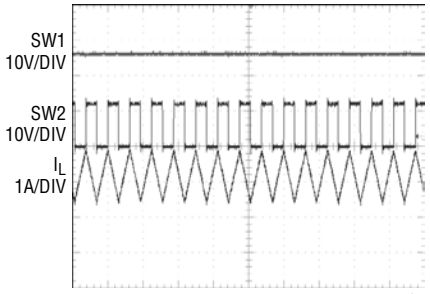


RUN Pin Threshold vs Temperature



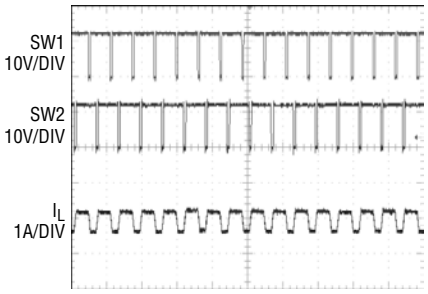
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Forced Continuous Mode



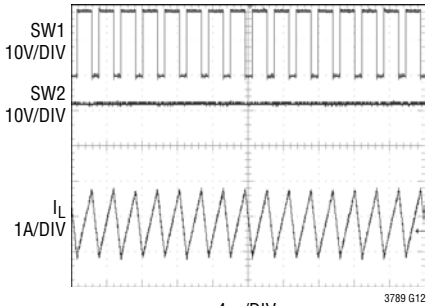
V_{IN} = 6V
V_{OUT} = 12V

Forced Continuous Mode



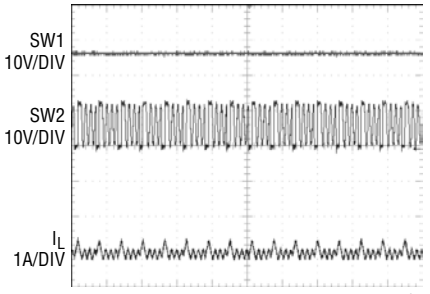
V_{IN} = 12V
V_{OUT} = 12V

Forced Continuous Mode



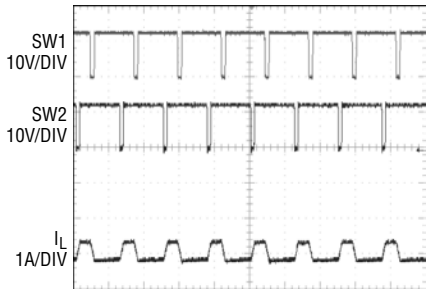
V_{IN} = 18V
V_{OUT} = 12V

Pulse-Skipping Mode



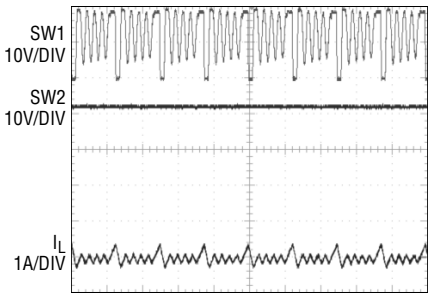
V_{IN} = 6V
V_{OUT} = 12V

Pulse-Skipping Mode



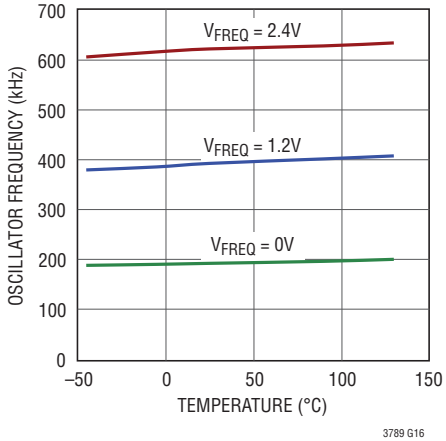
V_{IN} = 12V
V_{OUT} = 12V

Pulse-Skipping Mode

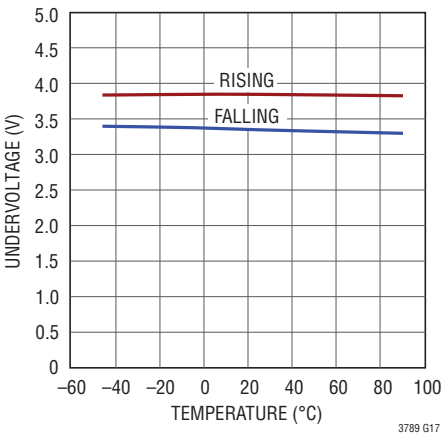


V_{IN} = 18V
V_{OUT} = 12V

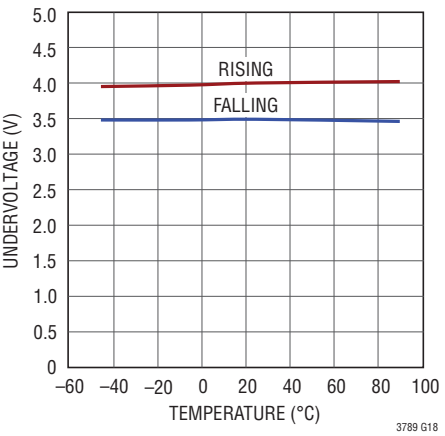
Oscillator Frequency vs Temperature



Undervoltage Threshold at $INTV_{CC}$ vs Temperature

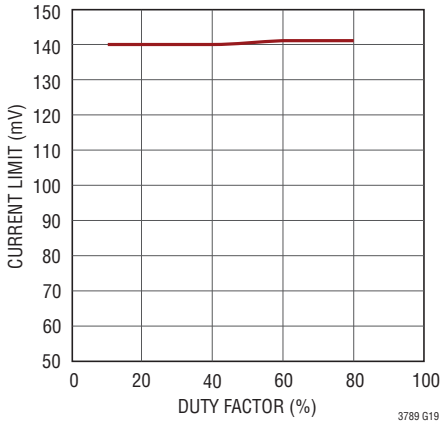


Undervoltage Threshold at V_{IN} vs Temperature

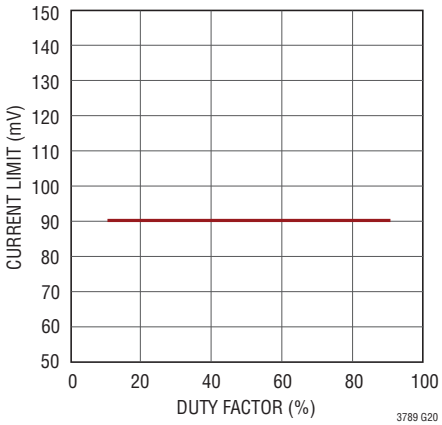


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

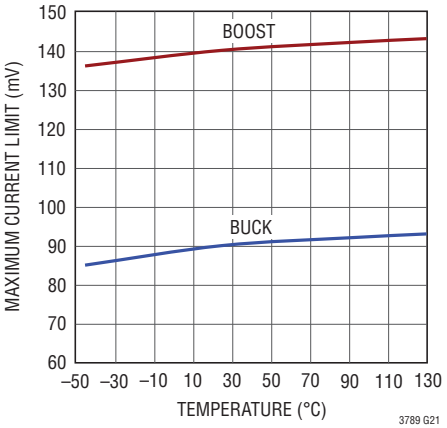
Maximum Current Sense Threshold vs Duty Factor (Boost)



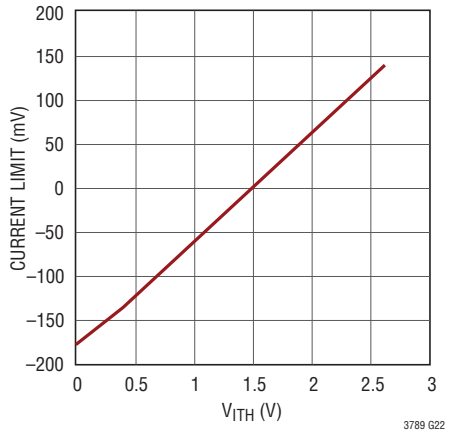
Maximum Current Sense Threshold vs Duty Factor (Buck)



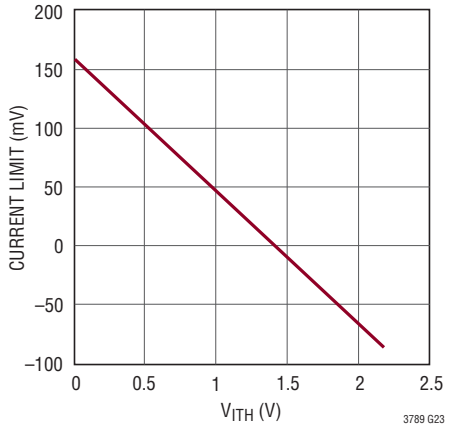
Maximum Current Limit vs Temperature



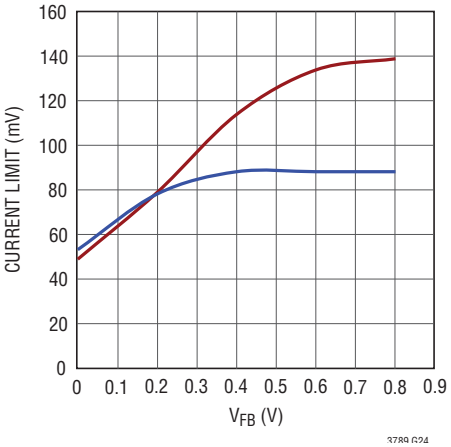
Peak Current Threshold vs V_{ITH} (Boost)



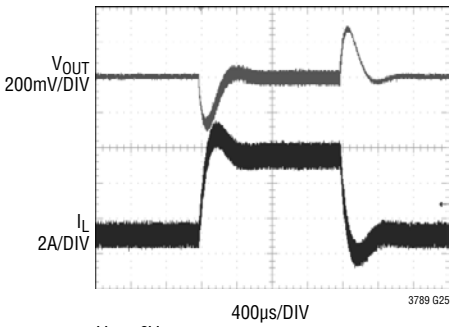
Valley Current Threshold vs V_{ITH} (Buck)



Current Foldback Limit

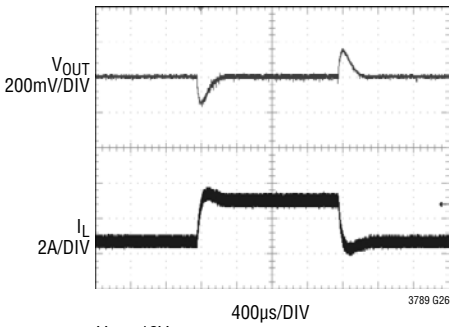


Load Step



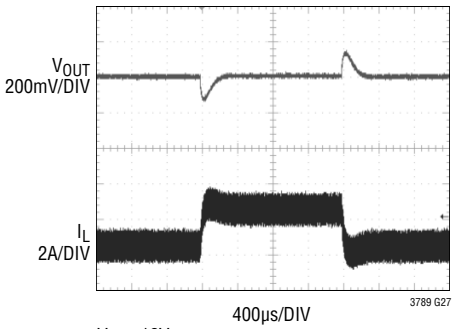
V_{IN} = 6V
V_{OUT} = 12V
LOAD STEP = 200mA TO 2A

Load Step



V_{IN} = 12V
V_{OUT} = 12V
LOAD STEP = 300mA TO 3A

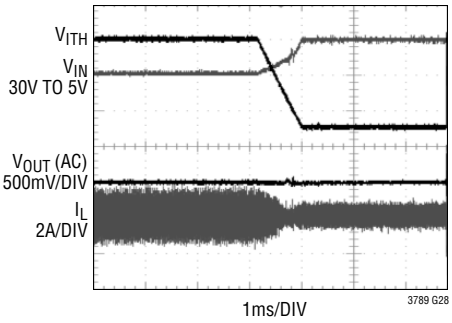
Load Step



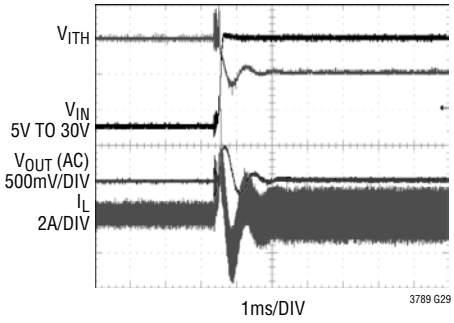
V_{IN} = 18V
V_{OUT} = 12V
LOAD STEP = 300mA TO 3A

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Line Transient



Line Transient



PIN FUNCTIONS (SSOP/QFN)

V_{FB} (Pin 1/Pin 26): Error Amplifier Feedback Pin. Receives the feedback voltage for the controller from an external resistive divider across the output.

SS (Pin 2/Pin 27): External Soft-Start Input. The LTC3789 regulates the V_{FB} voltage to the smaller of 0.8V or the voltage on the SS pin. A internal 3µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage.

$SENSE^+$ (Pin 3/Pin 28): The (+) Input to the Current Sense Comparator. The I_{TH} pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins, in conjunction with R_{SENSE}, set the current trip threshold.

$SENSE^-$ (Pin 4/Pin 1): The (–) Input to the Current Sense Comparator.

I_{TH} (Pin 5/Pin 2): Error Amplifier Output and Switching Regulator Compensation Point. The channel's current comparator trip point increases with this control voltage.

SGND (Pin 6/Pins 3, Exposed Pad Pin 29): Small Signal Ground. Must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitors. In the QFN package, the exposed pad is SGND. It must be soldered to PCB ground for rated thermal performance.

MODE/PLLIN (Pin 7/Pin 4): Mode Selection or External Synchronization Input to Phase Detector. This is a dual-purpose pin. When external frequency synchronization is not used, this pin selects the operating mode. The pin can be tied to SGND or $INTV_{CC}$. SGND or below 0.8V enables forced continuous mode. $INTV_{CC}$ enables pulse-skipping mode. For external sync, apply a clock signal to this pin; the internal PLL will synchronize the internal oscillator to the clock. The PLL composition network is integrated into the IC.

FREQ (Pin 8/Pin 5): Frequency Set Pin. There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which, in turn, programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

RUN (Pin 9/Pin 6): Run Control Input. Forcing the pin below 0.5V shuts down the controller, reducing quiescent current. There are 1.2µA pull-up currents for this pin. Once the RUN pin rises above 1.22V, the IC is turned on, and an additional 5µA pull-up current is added to the pin.

V_{INSNS} (Pin 10/Pin 7): V_{IN} Sense Input to the Buck-Boost Transition Comparator. Connect this pin to the drain of the top N-channel MOSFET on the input side.

PIN FUNCTIONS (SSOP/QFN)

V_{OUTSNS} (Pin 11/Pin 8): V_{OUT} Sense Input to the Buck-Boost Transition Comparator. Connect this pin to the drain of the top N-channel MOSFET on the output side.

I_{LIM} (Pin 12/Pin 9): Input/Output Average Current Sense Range Input. This pin tied to SGND, $INTV_{CC}$ or left floating, sets the maximum average current sense threshold.

I_{OSENSE}^+ (Pin 13/Pin 10): The (+) Input to the Input/Output Average Current Sense Amplifier.

I_{OSENSE}^- (Pin 14/Pin 11): The (–) Input to the Input/Output Average Current Sense Amplifier.

TRIM (Pin 15/Pin 12): Tie this pin to GND for normal operation. Do not allow this pin to float.

$EXTV_{CC}$ (Pin 20/Pin 17): External Power Input to an Internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{IN} whenever $EXTV_{CC}$ is higher than 4.8V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not exceed 14V on this pin.

$INTV_{CC}$ (Pin 21/Pin 18): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be bypassed to power ground with a minimum of 4.7µF tantalum, ceramic, or other low ESR capacitor.

V_{IN} (Pin 22/Pin 19): Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

BG1, BG2 (Pins 23, 19/Pins 20, 16): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

PGND (Pin 24/Pin 21): Driver Power Ground. Connects to C_{OUT} and R_{SENSE} (–) terminal(s) of C_{IN}.

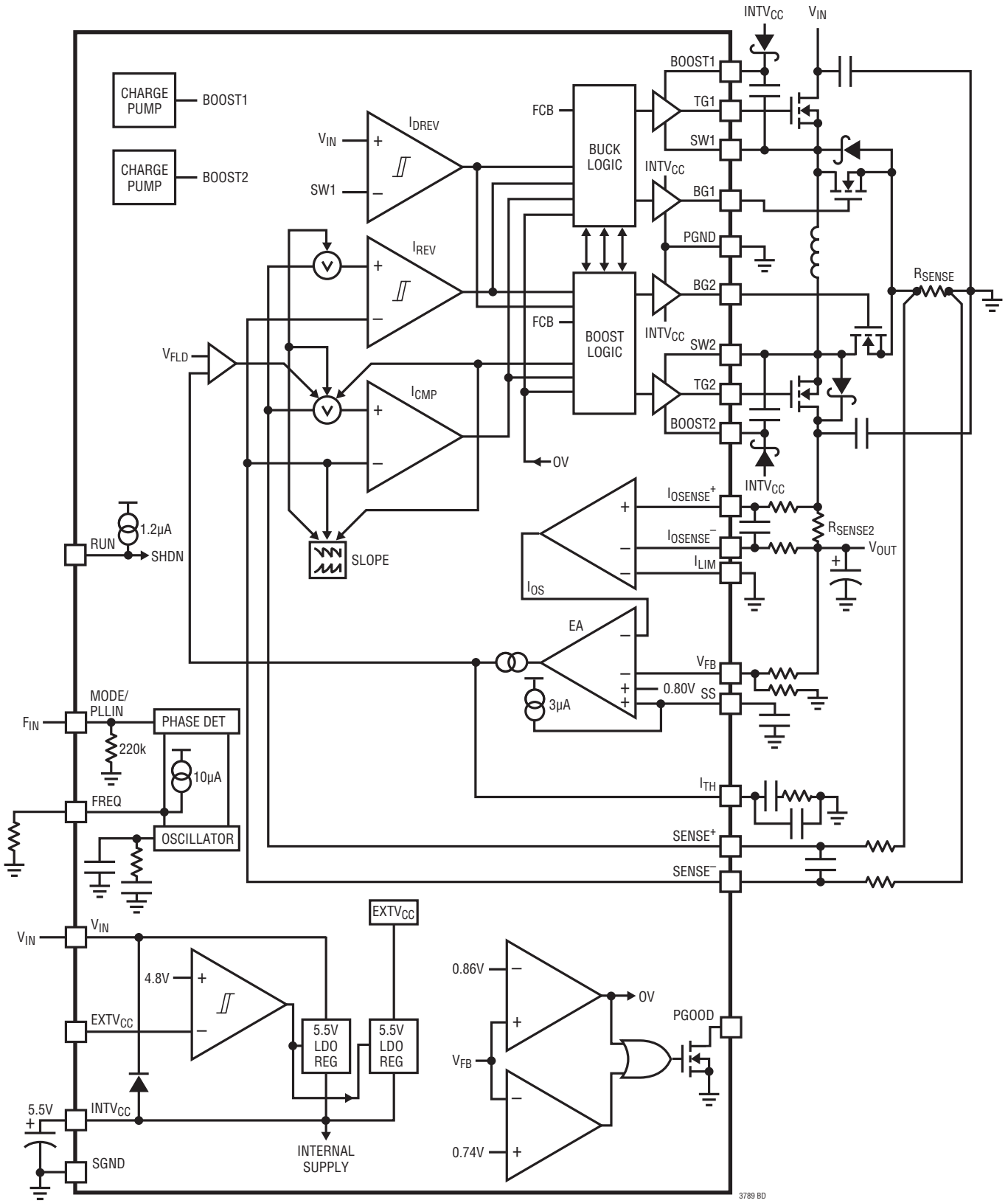
BOOST1, BOOST2 (Pins 25, 18/Pins 22, 15): Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

TG1, TG2 (Pins 26, 17/Pins 23, 14): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

SW1, SW2 (Pins 27, 16/Pins 24, 13): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

PGOOD (Pin 28/Pin 25): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on the V_{FB} pin is not within ±10% of its regulation window, after the internal 20µs power-bad mask timer expires.

BLOCK DIAGRAM



OPERATION

MAIN CONTROL LOOP

The LTC3789 is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC proprietary topology and control architecture employs a current-sensing resistor. The inductor current is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. If the input/output current regulation loop is implemented, the sensed inductor current is controlled by either the sensed feedback voltage or the input/output current.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ is left open or tied to a voltage less than 4.5V, an internal 5.5V low dropout (LDO) regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.8V, the 5.5V regulator is turned off, and another LDO regulates $INTV_{CC}$ from $EXTV_{CC}$. The $EXTV_{CC}$ LDO allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as the LTC3789 regulator output. The absolute maximum voltage on $EXTV_{CC}$ is 14V.

Internal Charge Pump

Each top MOSFET driver is biased from the floating bootstrap capacitors C_A and C_B, which are normally recharged by $INTV_{CC}$ through an external diode when the top MOSFET is turned off. When the LTC3789 operates exclusively in the buck or boost regions, one of the top MOSFETs is constantly on. An internal charge pump recharges the bootstrap capacitor to compensate for the small leakage current through the bootstrap diode so that the MOSFET can be kept on. However, if a high leakage diode is used such that the internal charge pump cannot provide sufficient charges to the external bootstrap capacitor, an internal UVLO comparator, which constantly monitors the drop across the capacitor, will sense the (BOOST – SW) voltage when it is below 3.6V. It will turn off the top MOSFET for about one-twelfth of the clock period every four cycles to allow C_A or C_B to recharge.

Shutdown and Start-Up

The controller can be shut down by pulling the RUN pin low. When the RUN pin voltage is below 0.5V, the LTC3789 goes into low quiescent current mode. Releasing RUN allows an internal 1.2µA current to pull up the pin and enable the controller. When RUN is above the accurate threshold of 1.22V, the internal LDO will power up the $INTV_{CC}$. At the same time, a 6µA pull-up current will kick in to provide more RUN pin hysteresis. The RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin.

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 0.8V internal reference, the LTC3789 regulates the V_{FB} voltage to the SS voltage instead of the 0.8V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to SGND. An internal 3µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively, the SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. When RUN is pulled low to disable the controller, or when $INTV_{CC}$ is below the undervoltage lockout threshold of 3.4V, the SS pin is pulled low by an internal MOSFET. In undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

OPERATION

POWER SWITCH CONTROL

Figure 1 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 2 shows the regions of operation for the LTC3789 as a function of duty cycle, D. The power switches are properly controlled so the transfer between regions is continuous.

Buck Region (V_{IN} >> V_{OUT})

Switch D is always on and switch C is always off in this region. At the start of every cycle, synchronous switch B is turned on first. Inductor current is sensed when synchronous switch B is turned on. After the sensed voltage falls below a reference voltage, which is proportional to V_{ITH}, synchronous switch B is turned off and switch A is turned on for the remainder of the cycle. Switches A and B will alternate, behaving like a typical synchronous buck regulator. The duty cycle of switch A increases until the maximum duty cycle of the converter reaches D_{MAX_BUCK}, given by:

$$D_{MAX_BUCK} = \left(1 - \frac{1}{12}\right) \bullet 100\% = 91.67\%$$

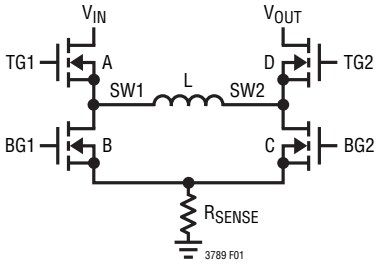


Figure 1. Simplified Diagram of the Output Switches

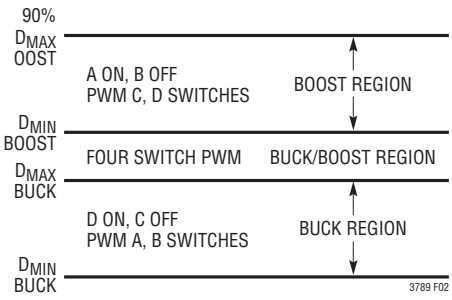


Figure 2. Operating Region vs Duty Cycle

Figure 3 shows typical buck region waveforms. If V_{IN} approaches V_{OUT}, the buck-boost region is reached.

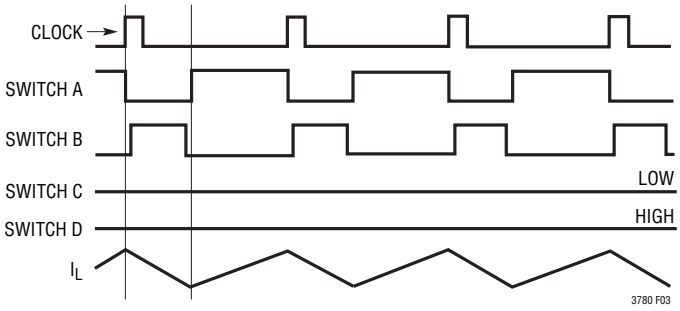


Figure 3. Buck Region (V_{IN} >> V_{OUT})

Buck-Boost Region (V_{IN} ≈ V_{OUT})

When V_{IN} is close to V_{OUT}, the controller enters buck-boost region. Figure 4 shows the typical waveforms in this region. At the beginning of a clock cycle, if the controller starts with B and D on, the controller first operates as a buck region. When I_{CMP} trips, switch B is turned off, and switch A is turned on. At 120° clock phase, switch C is turned on. The LTC3789 starts to operate as a boost until I_{CMP} trips. Then, switch D is turned on for the remainder of the clock period. If the controller starts with switches A and C on, the controller first operates as a boost, until I_{CMP} trips and switch D is turned on. At 120°, switch B is turned on, making it operate as a buck. Then, I_{CMP} trips, turning switch B off and switch A on for the remainder of the clock period.

Boost Region (V_{IN} << V_{OUT})

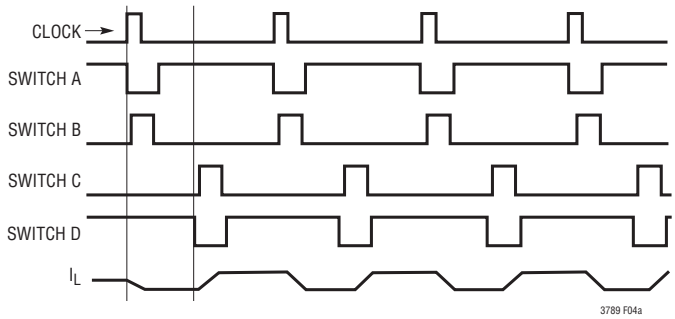
Switch A is always on and synchronous switch B is always off in the boost region. In every cycle, switch C is turned on first. Inductor current is sensed when synchronous switch C is turned on. After the sensed inductor current exceeds what the reference voltage demands, which is proportional to V_{ITH}, switch C is turned off and synchronous switch D is turned on for the remainder of the cycle. Switches C and D will alternate, behaving like a typical synchronous boost regulator.

OPERATION

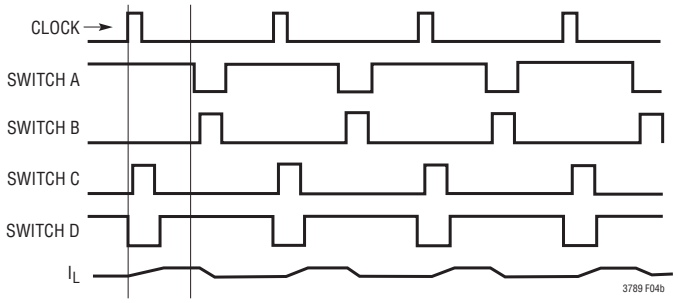
The duty cycle of switch C decreases until the minimum duty cycle of the converter reaches D_{MIN_BOOST}, given by:

$$D_{MIN_BOOST} = \left(\frac{1}{12}\right) \bullet 100\% = 8.33\%$$

Figure 5 shows typical boost region waveforms. If V_{IN} approaches V_{OUT}, the buck-boost region is reached.



(4a) Buck-Boost Region ($V_{IN} \geq V_{OUT}$)



(4b) Buck-Boost Region ($V_{IN} \leq V_{OUT}$)

Figure 4. Buck-Boost Region

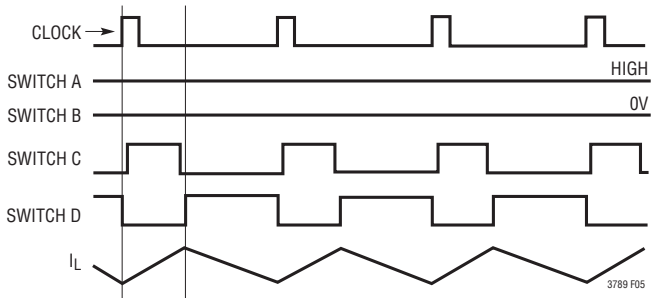


Figure 5. Boost Region ($V_{IN} << V_{OUT}$)

Light Load Current Operation

The LTC3789 can be enabled to enter pulse-skipping mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC voltage below 0.8V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$.

When the LTC3789 enters pulse-skipping mode, in the boost region, synchronous switch D is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force switch C to stay off for the same number of cycles (i.e., skipping pulses). In the buck region, the inductor current is not allowed to reverse. Synchronous switch B is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator, I_{CMP}, may remain untripped for several cycles, holding switch A off for the same number of cycles. Synchronous switch B also remains off for the skipped cycles. In the buck-boost region, the controller operates alternatively in boost and buck region in one clock cycle, as in continuous operation. A small amount of reverse current is allowed, to minimize ripple. For the same reason, a narrow band of continuous buck and boost operation is allowed on the high and low line ends of the buck-boost region.

Output Overvoltage

If the output voltage is higher than the value commanded by the V_{FB} resistor divider, the LTC3789 will respond according to the mode and region of operation. In continuous conduction mode, the LTC3789 will sink current into the input. If the input supply is capable of sinking current, the LTC3789 will allow up to about $160mV/R_{SENSE}$ to be sunk into the input. In pulse-skipping mode and in the buck or boost regions, switching will stop and the output will be allowed to remain high. In pulse-skipping mode, and in the buck/boost region as well as the narrow band of continuous boost operation that adjoins it, current sunk into the input through switch A is limited to approximately $40mV/R_{DS(ON)}$ of switch A. If this level is reached, switching will stop and the output will rise. In pulse-skipping mode, and in the narrow continuous buck region that adjoins the buck/boost region, current sunk into the input through R_{SENSE} is limited to approximately $40mV/R_{SENSE}$.

OPERATION

Constant-Current Regulation

The LTC3789 provides a constant-current regulation loop for either input or output current. A sensing resistor close to the input or output capacitor will sense the input or output current. When the current exceeds the programmed current limit, the voltage on the I_{TH} pin will be pulled down to maintain the desired maximum input or output current. The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current limit protection for a constant-voltage regulation application. The input/output current limit function has an operating voltage range of GND to the absolute maximum V_{OUT} (V_{IN}).

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC3789's controllers can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 200kHz to 600kHz.

Switching frequency is determined by the voltage on the FREQ pin. Since there is a precision 10µA current flowing out of the FREQ pin, the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided in the Applications Information section to show the relationship between the voltage on the FREQ pin and the switching frequency.

A phase-locked loop (PLL) is integrated on the LTC3789 to synchronize the internal oscillator to an external clock source driving the MODE/PLLIN pin. The controller operates in forced continuous mode when it is synchronized. The PLL filter network is integrated inside the LTC3789.

The PLL is capable of locking to any frequency within the range of 200kHz to 600kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Power Good (PGOOD) Pins

The PGOOD pin is connected to the open drain of an internal N-channel MOSFET. When V_{FB} is not within ±10% of the 0.8V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when RUN is below 1.22V or when the LTC3789 is in the soft-start phase. There is an internal 20µs power good or bad mask when V_{FB} goes in or out of the ±10% window. The PGOOD pin is allowed to be pulled up by an external resistor to $INTV_{CC}$ or an external source of up to 6V.

Short-Circuit Protection, Current Limit and Current Limit Foldback

The maximum current threshold of the controller is limited by a voltage clamp on the I_{TH} pin. In every boost cycle, the sensed maximum peak voltage is limited to 140mV. In every buck cycle, the sensed maximum voltage is limited to 90mV. In the buck-boost region, only peak sensed voltage is limited by the same threshold as in the boost region.

The LTC3789 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 50% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum value to one-third of the maximum value. Foldback current limiting is disabled during the soft-start. Under short-circuit conditions, the LTC3789 will limit the current by operating as a buck with very low duty cycles, and by skipping cycles. In this situation, synchronous switch B will dissipate most of the power (but less than in normal operation).

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3789 application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 38V.

R_{SENSE} Selection and Maximum Output Current

R_{SENSE} is chosen based on the required output current. The current comparator threshold sets the peak of the inductor current in the boost region and the maximum inductor valley current in the buck region. In the boost region, the maximum average load current at $V_{IN(MIN)}$ is:

$$I_{OUT(MAX,BOOST)} = \left(\frac{140mV}{R_{SENSE}} - \frac{\Delta I_L}{2}\right) \bullet \frac{V_{IN(MIN)}}{V_{OUT}}$$

where ΔI_L is peak-to-peak inductor ripple current. In the buck region, the maximum average load current is:

$$I_{OUT(MAX,BUCK)} = \frac{90mV}{R_{SENSE}} + \frac{\Delta I_L}{2}$$

Figure 6 shows how the load current ($I_{LOAD(MAX)} \bullet R_{SENSE}$) varies with input and output voltage.

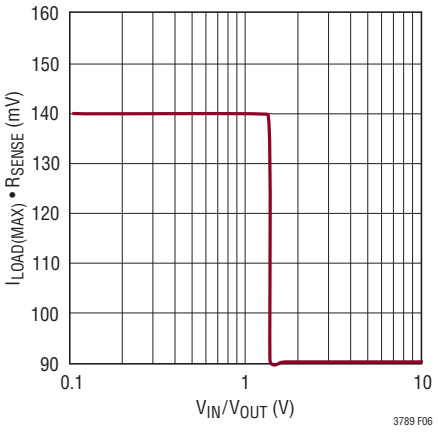


Figure 6. Load Current vs V_{IN}/V_{OUT}

The maximum current sensing R_{SENSE} value for the boost region is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 140mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_{L,BOOST} \bullet V_{IN(MIN)}}$$

The maximum current sensing R_{SENSE} value for the buck region is:

$$R_{SENSE(MAX)} = \frac{2 \bullet 90mV}{2 \bullet I_{OUT(MAX,BUCK)} - \Delta I_{L,BUCK}}$$

The final R_{SENSE} value should be lower than the calculated $R_{SENSE(MAX)}$ in both the boost and buck regions. A 20% to 30% margin is usually recommended.

Programming Input/Output Current Limit

As shown in Figures 7 and 8, current sense resistor R_{SENSE2} should be placed between the buck capacitor for V_{IN}/V_{OUT} and the decoupling capacitor. A lowpass filter formed by R_F and C_F is recommended to reduce the switching noise. The input/output current limit is set by the I_{LIM} pin for 50mV, 100mV or 140mV with I_{LIM} pulled to the GND, floating, or tied to $INTV_{CC}$, respectively. If input/output current limit is not desired, the I_{OSENSE}^+ and I_{OSENSE}^- pins should be shorted to either V_{OUT} or V_{IN}.

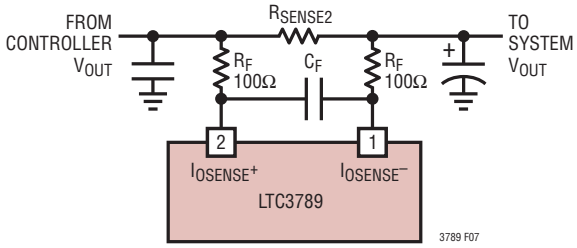


Figure 7. Programming Output Current Limit

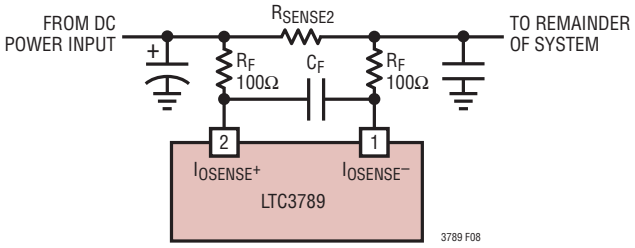


Figure 8. Programming Input Current Limit

APPLICATIONS INFORMATION

With the typical 100Ω resistors shown here, the value of capacitor C_F should be 1µF to 2.2µF. The current loop's transfer function should approximate that of the voltage loop. Crossover frequency should be one-tenth the switching frequency, and gain should decrease by 20dB/decade. Similar current and voltage loop transfer functions will ensure overall system stability.

When the I_{OSENSE} common mode voltage is above ~3.2V, the I_{OSENSE}^- pin sources 10µA. The I_{OSENSE}^+ pin, however, sources 18.3µA, 26.6µA and 35µA when the I_{LIM} pin is low, floating, and high, respectively, and when a constant current is being regulated. The error introduced by this mismatch can be offset to a first order by scaling the I_{OSENSE}^+ and I_{OSENSE}^- resistors accordingly. For example, if the I_{OSENSE}^+ branch has a 100Ω resistor, the 1.83mV across it can be replicated in the I_{OSENSE}^- branch by using a 182Ω resistor.

When the I_{OSENSE} common mode voltage falls below ~3.2V by a diode drop, the I_{OSENSE} current decreases linearly; it reaches approximately –300µA at zero volts. The values of the diode drop and maximum current sinking can vary by 20% to 30% due to process variation.

Slope Compensation

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles in boost operation and at low duty cycles in buck operation. This is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40% in the boost region, or subtracting a ramp from the inductor current signal at lower than 40% duty cycles in the buck region. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40% in the boost region, or an increase of maximum inductor current for duty cycles <40% in the buck region. However, the LTC3789 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor current to remain unaffected throughout all duty cycles.

Phase-Locked Loop and Frequency Synchronization

The LTC3789 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET of the controller to be locked to the rising edge of an external clock signal applied to the MODE/PLLIN pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false locking to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 10µA of current flowing out of the FREQ pin. This allows a single resistor to SGND to set the switching frequency when no external clock is applied to the MODE/PLLIN pin. The internal switch between FREQ and the integrated PLL filter network is on, allowing the filter network to be at the same voltage on the FREQ pin. Operating frequency is shown in Figure 9 and specified in the Electrical Characteristics table. If an external clock is detected on the MODE/PLLIN pin, the internal switch previously mentioned will turn off and isolate the influence of the FREQ pin. Note that the LTC3789 can only be synchronized to an external

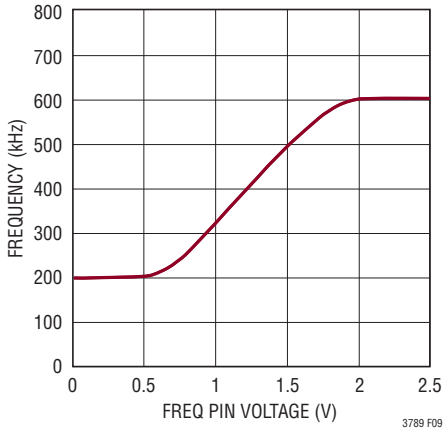


Figure 9. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

APPLICATIONS INFORMATION

clock whose frequency is within range of the LTC3789's internal VCO. This is guaranteed to be between 200kHz and 600kHz. A simplified block diagram is shown in Figure 10.

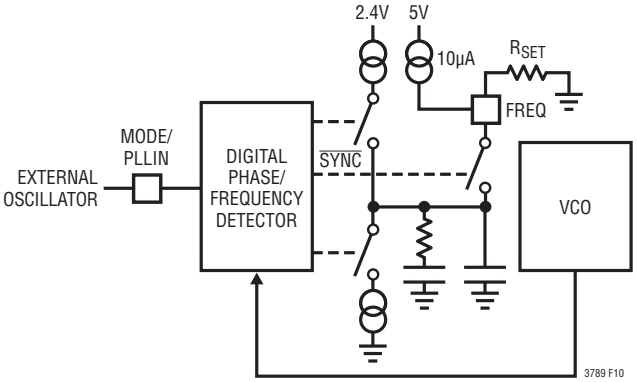


Figure 10. Phase-Locked Loop Block Diagram

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for the amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on the MODE/PLLIN pin) input high threshold is 1.6V, while the input low threshold is 1V.

Inductor Selection

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The inductor value has a direct effect on ripple current. The inductor current ripple ΔI_L is typically set to 20% to 40% of the maximum inductor current in the boost region at $V_{IN(MIN)}$.

For a given ripple the inductance terms in continuous mode are as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)}^{2} \bullet V_{OUT} - V_{IN(MIN)} \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%\ Ripple \bullet V_{OUT2}}\ H,$$

$$L_{BUCK} > \frac{V_{OUT} \bullet \left(V_{IN(MAX)} - V_{OUT}\right) \bullet 100}{f \bullet I_{OUT(MAX)} \bullet \%\ Ripple \bullet V_{IN(MAX)}}\ H$$

where:

f is operating frequency, Hz

% Ripple is allowable inductor current ripple

$V_{IN(MIN)}$ is minimum input voltage, V

$V_{IN(MAX)}$ is maximum input voltage, V

V_{OUT} is output voltage, V

$I_{OUT(MAX)}$ is maximum output load current, A

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

C_{IN} and C_{OUT} Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to derate the capacitor.

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In the boost region, the discontinuous current shifts from the input to the output, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$\text{Ripple (Boost,Cap)} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

$$\text{Ripple (Buck,Cap)} = \frac{I_{OUT(MAX)} \bullet \left(V_{IN(MAX)} - V_{OUT}\right)}{C_{OUT} \bullet V_{IN(MAX)} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST,ESR} = I_{L(MAX,BOOST)} \bullet ESR$$

$$\Delta V_{BUCK,ESR} = I_{L(MAX,BUCK)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings, such as OS-CON and POSCAP.

Power MOSFET Selection and Efficiency Considerations

The LTC3789 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in Figure 1) and two for the bottom switches (switches B and C, shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage $V_{BR,DSS}$, threshold voltage $V_{GS,TH}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and maximum current $I_{DS(MAX)}$.

The drive voltage is set by the 5.5V $INTV_{CC}$ supply. Consequently, logic-level threshold MOSFETs must be used in LTC3789 applications.

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A,BOOST} = \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

where ρ_τ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C, as shown in Figure 11. For a maximum junction temperature of 125°C, using a value ρ_τ = 1.5 is reasonable.

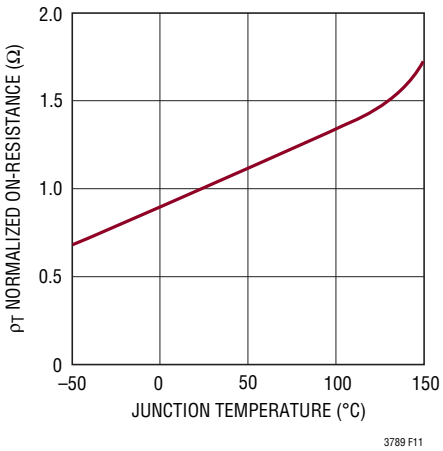


Figure 11. Normalized $R_{DS(ON)}$ vs Temperature

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C,BOOST} = \frac{\left(V_{OUT} - V_{IN}\right)V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

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where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)} \right)^2 \bullet \rho_{\tau} \bullet R_{DS(ON)}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output.

From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Schottky Diode (D1, D2) Selection

The Schottky diodes, D1 and D2, shown in Figure 13, conduct during the dead time between the conduction of the power MOSFET switches. They are intended to prevent the body diode of synchronous switches B and D from turning on and storing charge during the dead time. In particular, D2 significantly reduces reverse recovery current between switch D turn-off and switch C turn-on, which improves converter efficiency and reduces switch C voltage stress. In order for the diode to be effective, the inductance between it and the synchronous switch must be as small as possible, mandating that these components be placed adjacently.

$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3789 features a true PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3789's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5.5V when V_{IN} is greater than 6.5V. $EXTV_{CC}$ can supply the needed power when its voltage is higher than 4.8V through another on-chip PMOS LDO. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient current required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3789 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5.5V linear regulator from V_{IN} or the 5.5V LDO from $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.5V, the linear regulator from V_{IN} is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3789 $INTV_{CC}$ current is limited to less than 24mA from a 24V supply in the SSOP package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (28mA)(24V)(80°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = SGND) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the $INTV_{CC}$ linear regulator from V_{IN} is turned off and the linear regulator from $EXTV_{CC}$ is turned on and remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from the LTC3789's switching regulator output during normal operation and from the V_{IN} when the output is out of regulation (e.g., start-up, short-circuit). Do not apply more than 14V to $EXTV_{CC}$.

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Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the $EXTV_{CC}$ pin to a 12V output reduces the junction temperature in the previous example from 125°C to 97°C:

$$T_J = 70°C + (28mA)(12V)(80°C/W) = 97°C$$

Powering $INTV_{CC}$ from the output can also provide enough gate drive when V_{IN} drops below 5V. This allows a wider operating range for V_{IN} after the controller start into regulation.

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5.5V regulator at the cost of a small efficiency penalty.
2. $EXTV_{CC}$ connected directly to V_{OUT} ($4.7V < V_{OUT} < 14V$). This is the normal connection for the 5.5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available in the 4.7V to 14V range, it may be used to power $EXTV_{CC}$ provided it is compatible with the MOSFET gate drive requirements.

Note that there is an internal body diode from $INTV_{CC}$ to V_{IN}. When $INTV_{CC}$ is powered from $EXTV_{CC}$ and V_{IN} drops lower than 4.5V, the diode will create a back-feeding path from $EXTV_{CC}$ to V_{IN}. To limit this back-feeding current, a $10\Omega \sim 15\Omega$ resistor is recommended between the system V_{IN} voltage and the chip V_{IN} pin.

Output Voltage

The LTC3789 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.8V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R2}{R1}\right)$$

where R1 and R2 are defined in Figure 13.

Topside MOSFET Driver Supply (C_A, D_A, C_B, D_B)

Referring to Figure 13, the external bootstrap capacitors C_A and C_B connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside MOSFET switches A and D. When the top switch A turns on, the switch node SW2 rises to V_{IN} and the BOOST2 pin rises to approximately $V_{IN} + INTV_{CC}$. When the bottom switch B turns on, the switch node SW2 drops to low and the boost capacitor C_B is charged through D_B from $INTV_{CC}$. When the top switch D turns on, the switch node SW1 rises to V_{OUT} and the BOOST1 pin rises to approximately $V_{OUT} + INTV_{CC}$. When the bottom switch C turns on, the switch node SW1 drops to low and the boost capacitor C_A is charged through D_A from $INTV_{CC}$. The boost capacitors C_A and C_B need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate.

Undervoltage Lockout

The LTC3789 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.4V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 400mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 5µA of current flows out of the RUN pin once its voltage passes 1.22V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider.

Soft-Start Function

When a capacitor is connected to the SS pin, a soft-start current of 3µA starts to charge the capacitor. A soft-start function is achieved by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase to ensure smooth soft-start. When the chip is in the shutdown state with its RUN pin voltage below 1.22V, the SS pin is actively pulled

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to ground. The soft-start range is defined to be the voltage range from 0V to 0.8V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.8 \bullet \frac{C_{SS}}{3\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to SS = 0.8V.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. In the boost region, maximum sense voltage and the sense resistance determine the maximum allowed inductor peak current, which is:

$$I_{L(MAX,BOOST)} = \frac{140mV}{R_{SENSE}}$$

In the buck region, maximum sense voltage and the sense resistance determine the maximum allowed inductor valley current, which is:

$$I_{L(MAX,BUCK)} = \frac{90mV}{R_{SENSE}}$$

To further limit current in the event of a short circuit to ground, the LTC3789 includes foldback current limiting. If the output falls by more than 50%, then the maximum sense voltage is progressively lowered to about one-third of its full value.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Although all dissipative elements in circuit produce losses, four main sources account for most of the losses in LTC3789 circuits:

1. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. Transition loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors. The loss is significant at input voltages above 20V and can be estimated from:

   $$\text{Transition Loss} \approx 1.7A^{-1} \bullet V_{IN}^2 \bullet I_{OUT} \bullet C_{RSS} \bullet f$$

   where C_{RSS} is the reverse transfer capacitance.
3. $INTV_{CC}$ current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying $INTV_{CC}$ current through the $EXTV_{CC}$ pin from a high efficiency source, such as the output (if 4.7V < V_{OUT} < 14V) or alternate supply if available.
4. C_{IN} and C_{OUT} loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other losses. Schottky diodes D1 and D2 are responsible for conduction losses during dead time and light load conduction periods. Inductor core loss occurs predominately at light loads. Switch C causes reverse recovery current loss in boost mode.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

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Design Example

V_{IN} = 5V to 18V

V_{OUT} = 12V

$I_{OUT(MAX)}$ = 5A

f = 400kHz

Maximum ambient temperature = 60°C

Set the frequency at 400kHz by applying 1.2V on the FREQ pin (see Figure 7). The 10µA current flowing out of the FREQ pin will give 1.2V across a 120k resistor to GND. The inductance value is chosen first based on a 30% ripple current assumption. In the buck region, the ripple current is:

$$\Delta I_{L,BUCK} = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$I_{RIPPLE,BUCK} = \frac{\Delta I_{L,BUCK} \bullet 100}{I_{OUT}} \%$$

The highest value of ripple current occurs at the maximum input voltage. In the boost region, the ripple current is:

$$\Delta I_{L,BOOST} = \frac{V_{IN}}{f \bullet L} \bullet \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

$$I_{RIPPLE,BOOST} = \frac{\Delta I_{L,BOOST} \bullet 100}{I_{IN}} \%$$

The highest value of ripple current occurs at V_{IN} = V_{OUT}/2.

A 6.8µH inductor will produce 11% ripple in the boost region (V_{IN} = 6V) and 29% ripple in the buck region (V_{IN} = 18V).

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances.

$$R_{SENSE} = \frac{2 \bullet 140mV \bullet V_{IN(MIN)}}{2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT} + \Delta I_{L,BOOST} \bullet V_{IN(MIN)}}$$

Select an R_{SENSE} of 10mΩ.

Output voltage is 12V. Select R1 as 20k. R2 is:

$$R2 = \frac{V_{OUT} \bullet R1}{0.8} - R1$$

Select R2 as 280k. Both R1 and R2 should have a tolerance of no more than 1%.

Selecting MOSFET Switches

The MOSFETs are selected based on voltage rating and $R_{DS(ON)}$ value. It is important to ensure that the part is specified for operation with the available gate voltage amplitude. In this case, the amplitude is 5.5V and MOSFETs with an $R_{DS(ON)}$ value specified at V_{GS} = 4.5V can be used.

Select QA and QB. With 18V maximum input voltage MOSFETs with a rating of at least 30V are used. As we do not yet know the actual thermal resistance (circuit board design and airflow have a major impact) we assume that the MOSFET thermal resistance from junction to ambient is 50°C/W.

If we design for a maximum junction temperature, $T_{J(MAX)}$ = 125°C, the maximum $R_{DS(ON)}$ value can be calculated. First, calculate the maximum power dissipation:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_{A(MAX)}}{R_{(j-a)}}\right)$$

$$P_{D(MAX)} = \frac{(125 - 60)}{50} = 1.3W$$

The maximum dissipation in QA occurs at minimum input voltage when the circuit operates in the boost region and QA is on continuously. The input current is then:

$$\frac{V_{OUT} \bullet I_{OUT(MAX)}}{V_{IN(MIN)}}, \text{ OR } 12A$$

We calculate a maximum value for $R_{DS(ON)}$:

$$R_{DS(ON)}\ (125°C) < \frac{P_{D(MAX)}}{I_{IN(MAX)}^2}$$

$$R_{DS(ON)}\ (125°C) < \frac{1.3W}{(12A)^2} = 0.009\Omega$$

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The Vishay SiR422DP has a typical $R_{DS(ON)}$ of 0.010Ω at T_J = 125°C and V_{GS} = 4.5V.

The maximum dissipation in QB occurs at maximum input voltage when the circuit is operating in the buck region. The dissipation is:

$$P_{B,BUCK} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

$$R_{DS(ON)}(125°C) < \frac{1.3W}{\frac{18V\ TO\ -12V}{18V} \bullet (5A)^2} = 0.156\Omega$$

This seems to indicate that a quite small MOSFET can be used for QB if we only look at power loss. However, with 5A current the voltage drop across 0.156Ω is 0.78V, which means the MOSFET body diode is conducting. To avoid body diode current flow we should keep the maximum voltage drop well below 0.5V, using, for example, Vishay Si4840BDY in the SO-8 package ($R_{DSON(MAX)}$ = 0.012Ω).

Select QC and QD. With 12V output voltage we need MOSFETs with 20V or higher rating.

The highest dissipation occurs at minimum input voltage when the inductor current is highest. For switch QC the dissipation is:

$$P_{C,BOOST} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet \rho_\tau \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{RSS} \bullet f$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

The dissipation in switch QD is:

$$P_{D,BOOST} = \frac{V_{IN}}{V_{OUT}} \bullet \left(\frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}\right)^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

Vishay SiR484OY is a possible choice for QC and QD. The calculated power loss at 5V input voltage is then 1.3W for QC and 0.84W for QD.

C_{IN} is chosen to filter the square current in the buck region. In this mode, the maximum input current peak is:

$$I_{IN,PEAK(MAX,BUCK)} = 5A \bullet \left(1 + \frac{29\%}{2}\right) = 5.7A$$

A low ESR (10mΩ) capacitor is selected. Input voltage ripple is 57mV (assuming ESR dominates the ripple).

C_{OUT} is chosen to filter the square current in the boost region. In this mode, the maximum output current peak is:

$$I_{OUT,PEAK(MAX,BOOST)} = \frac{12}{5} \bullet 5 \bullet \left(1 + \frac{11\%}{2}\right) = 10.6A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 53mV (assuming ESR dominates the ripple).

PC Board Layout Checklist

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components.

- The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B and D1 in one compact area. Place C_{OUT}, switch C, switch D and D2 in one compact area. One layout example is shown in Figure 12.
- Use immediate vias to connect the components (including the LTC3789's SGND and PGND pins) to the ground plane. Use several large vias for each power component.

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- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND). When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3789. These items are also illustrated in Figure 13.
- Segregate the signal and power grounds. All small-signal components should return to the SGND pin at one point, which is then tied to the PGND pin close to the inductor current sense resistor R_{SENSE}.
- Place switch B and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dV/dT SW1, SW2, BOOST1, BOOST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B, D1 and the C_{IN} capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D, D2 and the C_{OUT} capacitor also should have short leads and PC trace lengths.

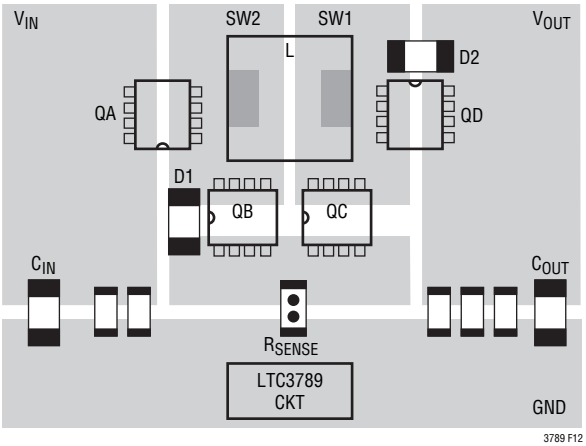


Figure 12. Switches Layout

- The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor C_A closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor C_B closely to the BOOST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck region.
- Connect V_{FB} pin resistive dividers to the (+) terminals of C_{OUT} and signal ground. A small V_{FB} bypass capacitor may be connected closely to the LTC3789 SGND pin. The R2 connection should not be along the high current or noise paths, such as the input capacitors.
- Route $SENSE^-$ and $SENSE^+$ leads together with minimum PC trace spacing. Avoid having sense lines pass through noisy areas, such as switch nodes. The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor. One layout example is shown in Figure 14.
- Connect the I_{TH} pin compensation network closely to the IC, between I_{TH} and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the $INTV_{CC}$ bypass capacitor, C_{VCC}, closely to the IC, between the $INTV_{CC}$ and the power ground pins. This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.

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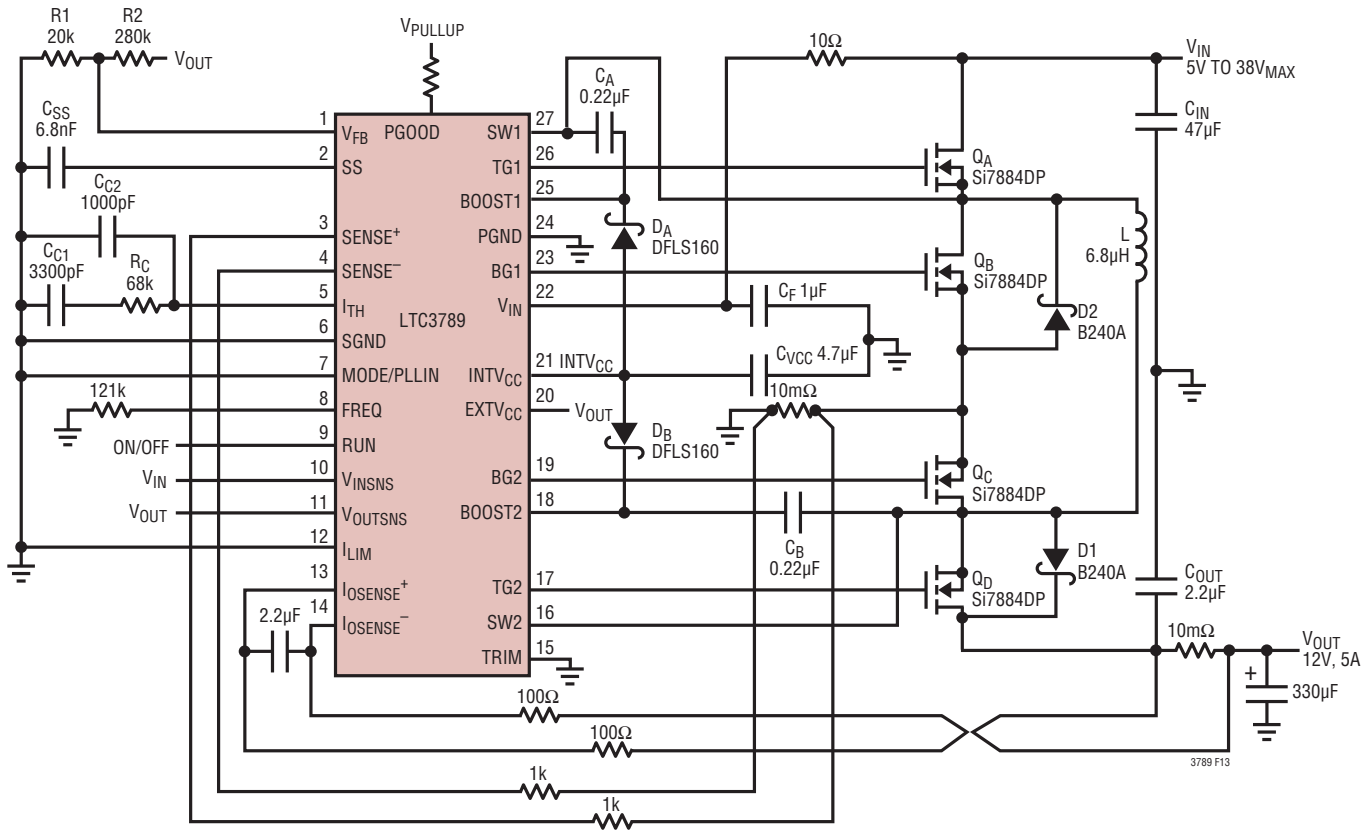


Figure 13. LTC3789 12V/5A, Buck-Boost Regulator

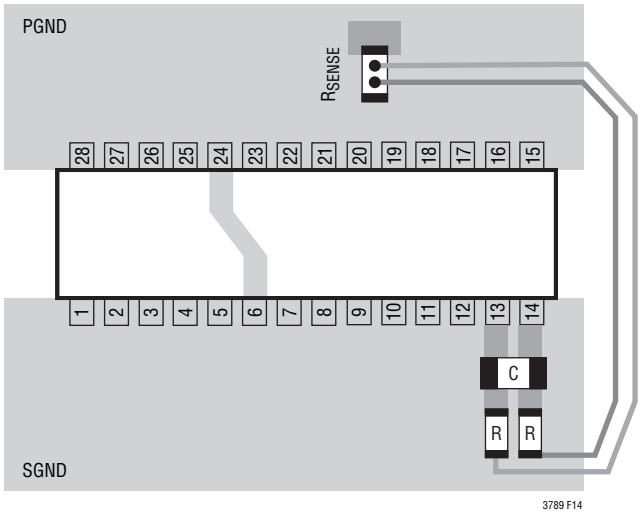
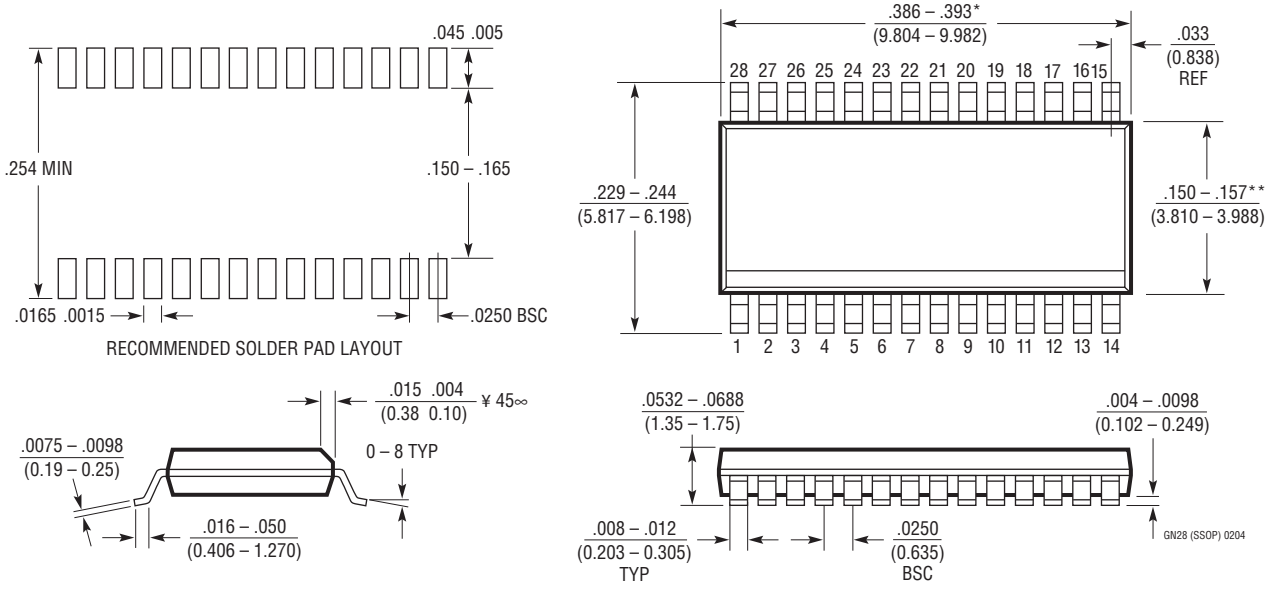


Figure 14. Sense Lines Layout

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



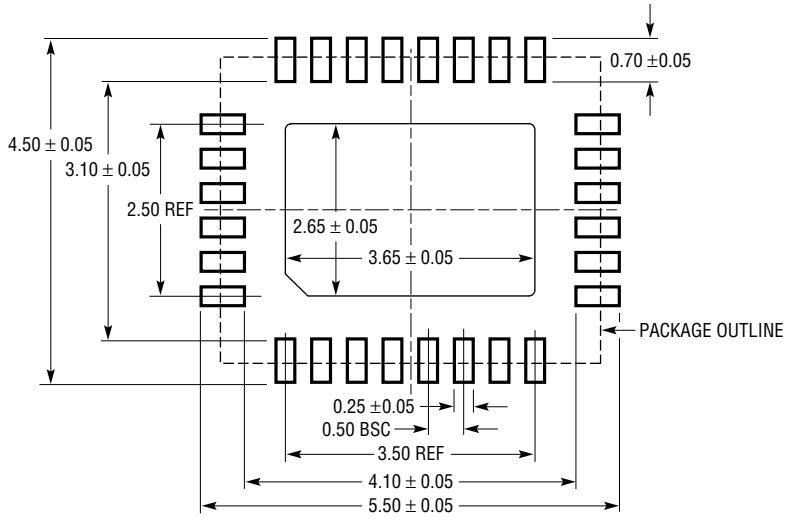
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

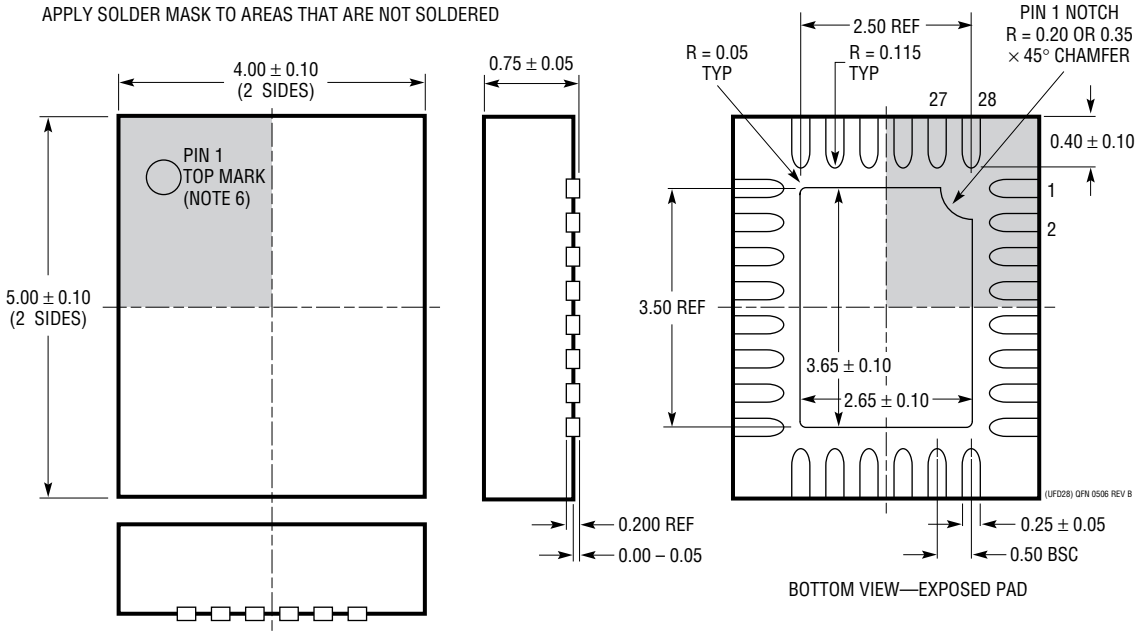
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

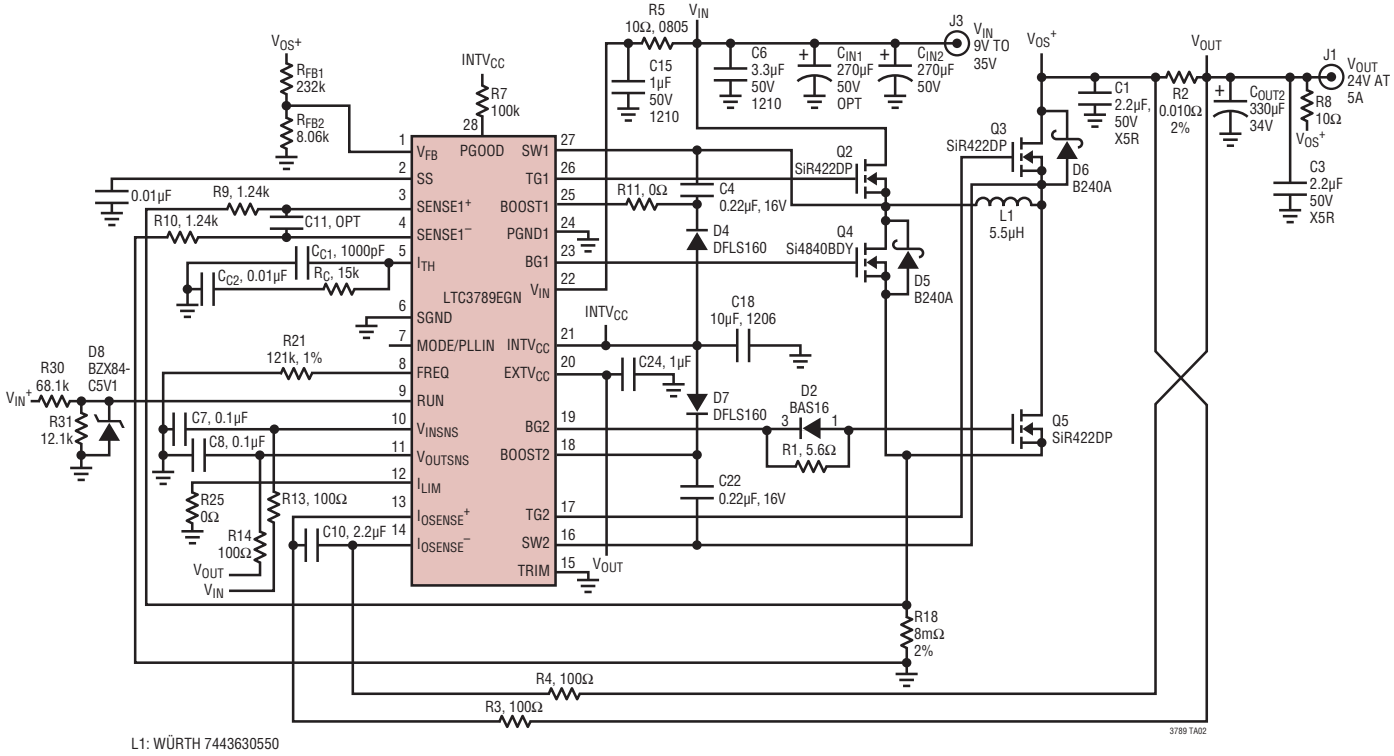


NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

24V/5A Buck-Boost Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3780	High Efficiency (Up to 98%) Synchronous, 4-Switch Buck-Boost DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 30V, 5mm × 5mm QFN-32 and SSOP-24 Packages
LTC3785	High Efficiency (Up to 98%) Synchronous, 4-Switch Buck-Boost DC/DC Controller	2.7V ≤ V_{IN} ≤ 30V, 2.7V ≤ V_{OUT} ≤ 10V, 4mm × 4mm QFN-24 Package
LTM4605	High Efficiency Buck-Boost DC/DC µModule™	4.5V ≤ V_{IN} ≤ 20V, 0.8V ≤ V_{OUT} ≤ 16V, 15mm × 15mm × 2.8mm LGA Package
LTM4607	High Efficiency Buck-Boost DC/DC µModule	4.5V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 25V, 15mm × 15mm × 2.8mm LGA Package
LTM4609	High Efficiency Buck-Boost DC/DC µModule	4.5V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 34V, 15mm × 15mm × 2.8mm LGA Package
LTC3533	2A Synchronous Buck-Boost Monolithic DC/DC Converter	1.8V ≤ V_{IN} ≤ 5.5V, 1.8V ≤ V_{OUT} ≤ 5.25V, I_Q = 40µA, I_{SD} < 1µA, 3mm × 4mm DFN-14 Package

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