OPTIMIZED Bluetooth® 5.0 LOW-ENERGY COMPANION OR SOC

Description

The EM9304 is a tiny, low-power, integrated circuit (IC) optimized for *Bluetooth® 5.0* low energy enabled products. The flexible architecture of the EM9304 allows it to act as a companion IC to any ASIC or MCU-based product, or as a complete System-on-Chip (SoC). Custom applications can execute from one-time-programmable (OTP) memory, and digital peripherals (SPI or I2C) can be used to interface with external devices such as sensors, memory, display, or touch drivers. A floating point unit can be exploited to implement advanced algorithms such as sensor fusion.

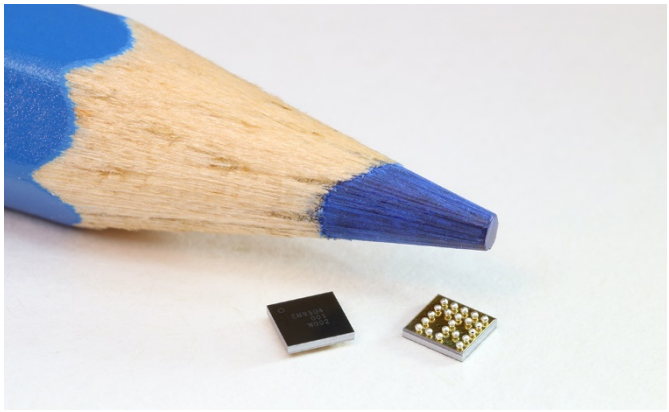
Included in ROM is a Bluetooth 5.0 link layer with a Host Controller Interface (HCI), a Bluetooth stack with proprietary Application Controller Interface (ACI), several profiles, and over-the-air firmware (FOTA) updating routines. The Bluetooth low energy controller and host can be configured to support up to eight simultaneous connections. Secure connections and extended packet length are also supported.

The EM9304 includes a sophisticated on-chip power management system with automatic configuration for 1.5V or 3V batteries. Current consumption is minimized for all modes of the application utilizing an efficient scheduler and memory manager. Several memory configuration options allow for optimum performance for any given application. A stable, low-power sleep oscillator (RC or crystal based) minimizes power consumption while in a connected state.

The EM9304 features a state-of-the-art 2.4GHz transceiver: an extremely low-power receiver with excellent sensitivity/selectivity, and a programmable transmitter for optimized output power and current consumption.

The PCB footprint and cost is minimized with a very low external component count and several package options. The circuit is offered in a WLCSP25 wafer level chip-scale package, a plastic QFN-28 package, and bare die/ wafer form. The device and reference design is qualified over the industrial temperature range.

Customer support for PCB design, and FCC/CE certification are available. A hardware and software development kit are available, including commercially available tools with IDE and debugger. A website and forum are also available to help with your custom developments.



Main Features

System-on-Chip:

- Energy efficient, industry standard, ARC EM4, 32-bit MCU running at 24MHz
- Floating-point unit for sensor processing
- 136kB ROM including link layer and stack
- 128kB OTP for parameters, profiles, and applications – 24MHz execution speed
- 48kB instruction RAM and 28kB data RAM
- 4, 8, or 20kB with selectable data retention
- Universal, sleep, and protocol timers
- I2C and SPI master interfaces
- Up to 12 GPIO

Bluetooth 5.0 Low Energy Technology:

- BT 5.0 Controller Subsystem (QD ID 93999)
- Bluetooth stack (QD ID 84268) in ROM
- SPI and UART HCI/ACI Transport Layers
- Up to eight simultaneous connections supported
- Extended PDU length and enhanced security

Security Features:

- True Random Number Generator
- AES-128 Hardware Encryption Engine
- Key Generation (ECC-P256)

Firmware Over-the-Air Updating

- Per application, function, or configuration

Sophisticated Power Management System:

- Digital step-up/down DCDC operation
- Supports 1.5V and 3.0V batteries
- Scheduler and memory manager
- Low frequency RC or crystal oscillator time base

Low Current Consumption at 3V:

- 3.0mA typical peak receiver current
- 5.2mA typical peak transmitter current at 0.4dBm
- 1.0µA connected sleep mode
- 5nA chip disable mode

High Performance RF:

- -94dBm Bluetooth low energy receiver sensitivity for 1Mpbs operation and 37 byte payload
- -34 to +6.1dBm transmitter output power range

Low Component Count and Cost:

- 3 DC caps, 1 DCDC coil, 1 ferrite bead
- Single ended 50Ω antenna pin (no balun)
- 48MHz XTAL, 32kHz XTAL (optional)

Packaging:

- QFN-28 (4x4mm), WLCSP25, and bare-die/wafer

Industrial Operating Temperature Range: -40C to +85C

Customer Support:

- Hardware, software development kits
- FCC/CE certification support
- Forum for hardware and software support

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Typical Applications

Bluetooth low energy applications such as:
Beacons
Wearables and Sports Equipment
Healthcare Monitoring
Remote Sensing
Motion and Tracking Devices
Home Automation
Light Control Applications
Wireless Mice and Keyboards
Alarms and Security System
Toys
Enabled by the mobile phone as access-point to the Internet.

Typical Application Diagrams

The EM9304 is the ideal Bluetooth low energy companion IC for any MCU or ASIC application, as illustrated in Figure 1. It may be easily connected with:

- standard 3V MCU's within the very rich catalog of any microprocessor vendor;
- standard 1.5V MCU's such as ultra-low-power watch microprocessors from EM Microelectronic;
- any custom sensor processing ASIC for customers requiring a simple add-on function.

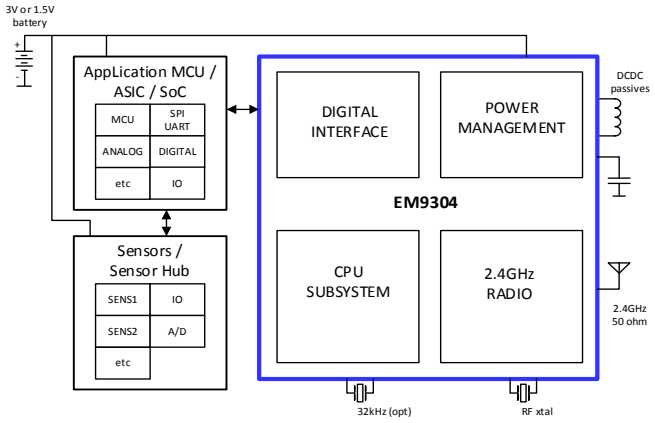


Figure 1: Typical Application Schematic – Bluetooth Low-Energy Companion IC to any MCU or ASIC

The EM9304 is a flexible solution which may also be used without an external MCU for simple applications such as beacons. As illustrated in Figure 2, it may be directly connected to external digital sensors which may exploit the EM9304's internal 32-bit processing capability, or with sensor hubs such as from EM's SENtral platform. Other applications using A/D converters, EEPROMs, display and/or touch interfaces can also be implemented.

The EM9304 can be supplied from a 3V battery (e.g. Lithium coin-cell). In such case, the DCDC converter is put into step-down configuration. The EM9304 can also be supplied from a 1.5V battery (e.g. Alkaline, Silver-Oxide, or Zinc-Air single cells). In such case, the DCDC converter is put into step-up configuration.

Finally, configurations are also possible without the DCDC converter (no inductor required), for systems already with power management, or for systems that require the lowest bill of materials.

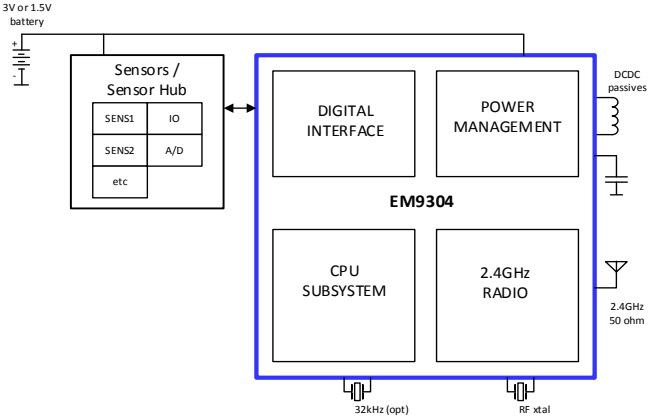


Figure 2: Typical Application Schematic – EM9304 Connected With Digital Sensors / Sensor Hubs

Package Information

The versions below are considered standards and should be readily available. Please make sure to give the complete part number when ordering.

WLCSP25, 5x5 array, 0.4mm pitch, 2.3x2.2mm

QFN-28, 0.4mm pitch, 4x4mm

Bare die in wafer format

Please contact EM Microelectronic-Marin S.A. for more information.

Product and Developer Support

The following product support is available:

Hardware Development Kit (DVK)

Software Development Kit (SDK)

- Getting Started guide and PC Tools
- Integrated Development Environment (IDE) for ARC Metaware and MetawareLite Tools
- Reference designs with schematics, PCB layouts, and bill-of-materials
- Developer forum for hardware and software support
- www.emdeveloper.com

PCB Antenna Design Support

FCC/CE Test Support

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1 Overview

1.1 Introduction

The EM9304 is a 2.4 GHz RF system on chip with the following target applications:

- **Bluetooth Controller Mode**
  - Host connect to controller via Host Controller Interface (HCI)
  - HCI interface implemented via SPI or UART transport layer
  - Link layer implemented in ROM
  - Up to 8 simultaneous connections supported
  - Long packet lengths (payload up to 255 bytes) supported

- **Bluetooth Companion Mode**
  - Interface to host with proprietary Application Controller Interface (ACI)
  - ACI interface implemented via SPI or UART transport layer
  - Bluetooth 4.2 certified stack and standard profiles and services implemented in ROM
  - Additional profiles and services can be loaded and stored in OTP
  - Secure connections including key-exchange supported
  - All other Controller Mode features supported except HCI

- **Bluetooth Application Mode**
  - Application hosting
    - Low energy applications such as proximity or sensor beacons using Bluetooth are easily implemented
    - Connections to digital peripherals through SPI, I2C, UART, and GPIOs allow for data collection, storage, or display for example.
  - Software development platform
    - Application Program Interface (API) available for all levels of firmware
    - Full featured development tools (Metaware/MetawareLite and GCC)
    - Development and debugging using JTAG interface
    - Programs can be developed in RAM and then moved to OTP
    - Programs stored in OTP can execute from RAM or OTP
  - All Controller Mode and Companion Mode features supported

The chip architecture is described in Section 1.2. A 32-bit MCU efficiently controls the movement of data between the RF modem, memory, and the digital interfaces. Digital interfaces include UART, SPI, and I2C which are mapped to GPIO as required by the application. Other peripherals include an interrupt manager, timers, and encryption engines. The RF and Power Management blocks are described in separate sections. The firmware is implemented in a power efficient manner using a scheduler, memory manager, hardware drivers, link layer, and stack implemented in a single ROM. The state can be retained in 4kB, 8kB, or 20kB retention memory selectable to optimize features versus memory leakage. And a one-time programmable (OTP) memory is used for trimming, unique identification numbers, profiles, patches, and application storage.

The firmware can be updated or “patched” through SPI, UART, JTAG, or using firmware-over-the-air (FOTA). Patches can be loaded into and executed from RAM or OTP. (Note, JTAG cannot be used to directly write to OTP.) Patches can be loaded from external memory via SPI, UART, or I2C interfaces.

The RF modem is described in Section 1.3. A very sensitive RF front-end achieves a -94dBm typical sensitivity for 1Mbps operation with 37 byte payloads, while dissipating very low current (3.0mA peak) at 3V. An efficient transmitter at 0.4dBm output power and dissipates only 5.2mA at 3V. Programmable RF power levels from -34dBm up to +6.1dBm are possible. A connection to a 50 ohm antenna with appropriate matching circuit. Fast mode transition times and extremely low sleep current (1μA) enable very low energy application implementations.

An advanced power management system is described in Section 1.4. Power consumption and battery life are optimized in all conditions. Most common 1.5V and 3.0V primary battery cell technologies are directly supported including Lithium, Alkaline, Zinc-Air and Silver Oxide. For 1.5V batteries, the on-chip DCDC converter steps up the voltage to the required internal levels. For 3.0V batteries, the on-chip DCDC converter steps the voltage down internally for efficient power consumption. Very few external components are necessary for the DCDC converter operation; however, it is also possible to operate without the converter or using an external converter to minimize component count even further.

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Packaging options are described in Section 4. Several types are offered for various application constraints. A wafer chip-scale package (WLCSP25) is offered for minimum PCB footprint 2.340mm x 2.206mm; a QFN-28 package compatible with standard PCB technology is offered with additional GPIOs; and bare die in wafer format is offered for i.e. chip-on-board (COB) applications.

The package pins are described in Section 1.6. The GPIO configuration is described in Section 1.7. The reference schematics are described in Section 1.8 with required and optional external components.

1.2 Chip Architecture

The chip architecture is shown in Figure 3. In Figure 3a, the hardware architecture is shown. A 32-bit MCU efficiently controls the movement of data between the RF modem, memory, and the digital interfaces. The 32-bit MCU includes a floating point unit (FPU) for efficient implementation of sensor algorithms, for example. A CRC coprocessor is also included for efficient verification of program memory, for example. Memories are included for the following functions (size shown in parentheses):

- ROM (136kB) – used for the start-up sequence, Bluetooth low energy link layer, and stack
- iRAM (48kB) – used for application development
- dRAMs (4, 4, and 12kB) – used for data with optional state retention
- dRAM (8kB) – used for data without state retention
- iRAM (4kB) – used for the subroutine jump table
- OTP (128k) – used for configuration data, Bluetooth profiles, and applications

The memory architecture is divided into several different power domains for power consumption optimizations. When a memory is not being used, it can be switched off to reduce current consumption. During Bluetooth connected sleep mode the entire MCU subsystem can be shut off and only the power management system and required state retention memories (if any) need to be powered. The power management system will properly wakeup the MCU subsystem when it is needed. The RF modem is also on a separate supply domain and is turned on and off as needed in order to minimize energy consumption.

Digital interfaces including UART, SPI slave, SPI master, and I2C master are mapped to GPIO as required by the application. When the chip is used as a peripheral to a host application, then the SPI slave and UART can be used for communication. The standard Host-Controller Interface (HCI) is implemented for communicating with the link layer, and a proprietary Application-Controller Interface (ACI) is implemented for communicating with the stack and profiles. When the chip is used as an application host, then the SPI master or I2C master can be used to talk with most standard digital peripherals. Other peripherals include an interrupt manager and three timers for low power implementations, and an AES-128 encryption engine for security implementation. A NIST compliant true random number generator is also included for key generation.

The software architecture is shown in Figure 3b. The firmware is implemented in a power efficient manner using a basic scheduler and memory manager. The EM9304 implements a Bluetooth 5.0 compliant link layer at the bottom of the stack and accessed through the standard HCI interface. Peripherals are accessed through hardware drivers. Bluetooth HCI commands are implemented and additionally some vendor specific commands are implemented. The link layer is designed to optimize power consumption in each role. The CPU is normally halted and is only activated when a task needs to be accomplished. When sleeping, states and connection information are properly stored in the retention memory and all other memories and peripherals are turned off. A low power timer is used to properly wakeup the system. The EM9304 is certified by the Bluetooth SIG as Bluetooth Low Energy 5.0 Controller Subsystem (QD ID 93999).

The Bluetooth 4.2 low energy stack (QD ID 84268) is accessed through a proprietary Application Controller Interface (ACI) in ACI mode or Application Programming Interface (API) in application mode. The stack includes the L2CAP, Security Manager, ATT, GAP, and GATT. Standard Bluetooth profiles such as Proximity and Find-Me are also included in this ROM, as well as proprietary data-exchange and Firmware-Over-the-Air updating procedures to help manage data and program transfer.

The EM9304 can be customized using the one-time programmable (OTP) memory. Specific Bluetooth profiles can be loaded depending on the application. Simple applications can be implemented including sensor interfaces. Package configuration, production trim parameters and unique identification numbers can also be stored here.

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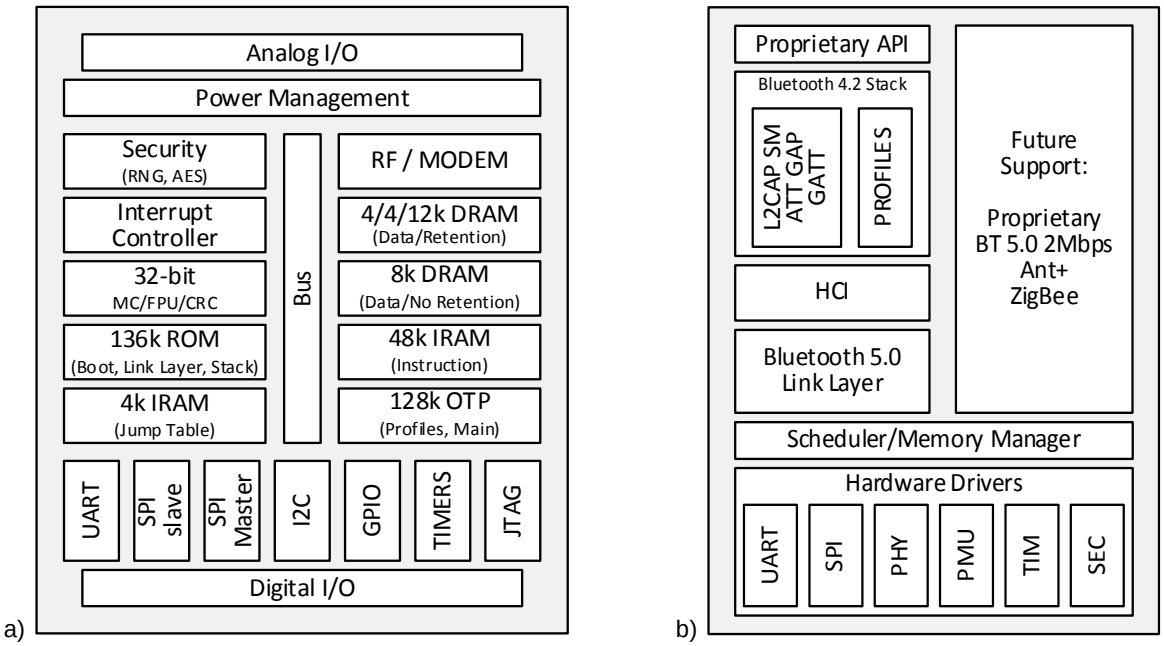


Figure 3: a) Hardware Architecture, b) Software Architecture

1.3 RF Description

The RF transceiver exceeds the specifications and requirements of the Bluetooth 5.0 PHY specification.

The main features of the RF transceiver are the following:

- Ultra-low-power: The peak current in receive mode is 3.0 mA and in transmit mode is 5.2mA at 0.4dBm and 3.0V in DCDC Step-Down Configuration at room temperature.
- Excellent RF performance: including -94dBm sensitivity for 1Mbps operation with 37 byte payload and a programmable output power range from -34dBm to +6.1dBm
- Low-voltage: Operation from 3.6V down to 1.05V
- Very high degree of integration: small footprint with few external components

The RF transceiver block diagram is shown in Figure 4.

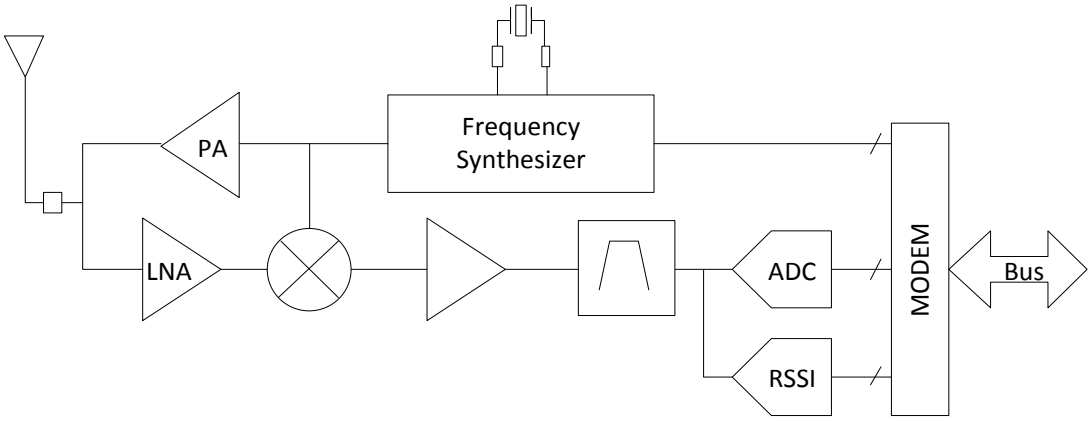


Figure 4: RF Transceiver Block Diagram

The RF transceiver is based on a low-IF architecture and comprises the following building blocks:

- Single-ended 50 Ohm RF port with on-chip harmonic filter
- High gain, low power, LNA and mixer
- Power Amplifier with programmable output power range
- Low-IF receiver with 5th order channel filter and ADC converter
- Fully integrated frequency synthesis with fast settling time and digital modulation
- 48MHz XTAL reference with finely trimmable internal loading capacitor

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- Fully integrated FSK-based modem, with programmable pulse shape, data rate and modulation index
- Digital baseband (DBB) with link layer functionalities, including automatic packet handling with preamble & sync, CRC, separate Rx and Tx 128-bytes FIFOs, support of long packets, early signalling of incoming packet, integrated CCM-AES encryption, and supporting multiple simultaneous connections.

The RF specifications are detailed in Section 2.8.

1.4 Power Management Description

An advanced power management system is implemented on the EM9304. Key low-power circuits include a configurable and highly-efficient DCDC converter, low noise bandgap references, low drop-out regulators (LDOs), a high frequency RC oscillator for efficient MCU operation, and a high accuracy, low frequency, RC oscillator for sleep mode control. A sophisticated digital control system optimizes power consumption and battery life in all conditions. There are four possible power management configurations: DCDC Step-Down, DCDC-Step-Up, DCDC Off, and External DCDC. The configuration is automatically detected from the PCB, but a minimum supply voltage ramp-up must be maintained.

The most common application configurations are shown in Figure 5. In Figure 5a, DCDC Step-Down Configuration, a typical arrangement is shown for connecting a 3V battery (1 Lithium or 2 Alkaline cells, for example) to the EM9304 and an external 3V MCU. The battery is applied to VBAT1, which powers the DCDC converter and OTP, and VBAT2, which powers key analog circuits in the power management. Using the SW pin, a coil and capacitor, the DCDC converter efficiently steps-down the battery voltage to generate 1.25V on the VCC pin. This is the main supply voltage for the rest of the IC during normal operation. During sleep mode the DCDC operation is off and an optional charging circuit is used to maintain VCC.

In Figure 5b, DCDC Step-Up Configuration, a typical arrangement is shown for connecting a 1.5V battery (1 Alkaline, Zinc Air or Silver Oxide cell, for example) to the EM9304 and an external 1.5V MCU. The battery is applied to VCC, which is the main supply for the IC including the RF portion, and VBAT2, which powers key analog circuits in the power management. Using the SW pin, a coil and capacitor, the DCDC converter steps-up the battery voltage to generate 2.6V on the VBAT1 pin to supply the OTP. During sleep mode the DCDC operation is off.

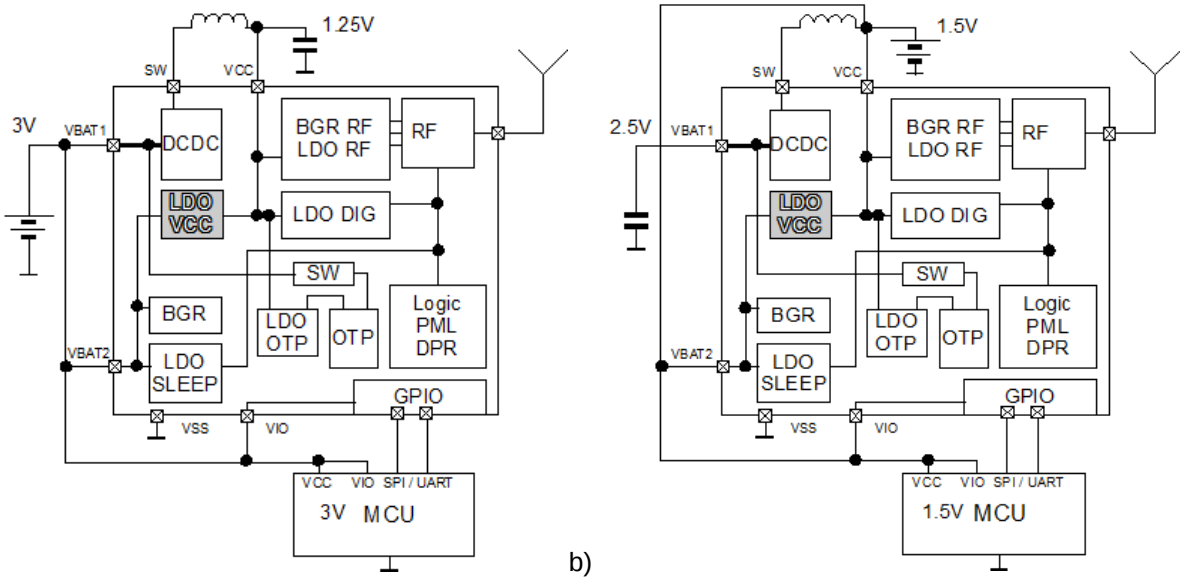


Figure 5: a) DCDC Step-Down Configuration, b) DCDC Step-Up Configuration

Other possible configurations are shown in Figure 6 which have the minimum possible external components. In Figure 6a is the DCDC Off Configuration. In this case, a 3V battery source is required and applied directly to VBAT1 and VBAT2. An internal LDO is then used to generate 1.25V on the VCC pin. The DCDC converter is not used in this arrangement and is turned off. Since the 1.25V is generated by a linear regulator instead of a switching regulator, more power is consumed in this arrangement.

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In Figure 6b, External DCDC Configuration, the configuration shown utilizes an external DCDC converter from an external 1.5V MCU. In this case, the 1.5V battery is applied to the VBAT2 and VCC pins of the EM9304 and the MCU. The DCDC converter on the 1.5V MCU, for example, then generates the required 2.6V for the OTP and applies it to VBAT1. This is less efficient than the configuration described in Figure 5b in terms of power consumption because the sleep modes cannot be optimized; however, it does reduce the overall system component count.

Other configurations could be possible, but please review with EM Microelectronic before proceeding.

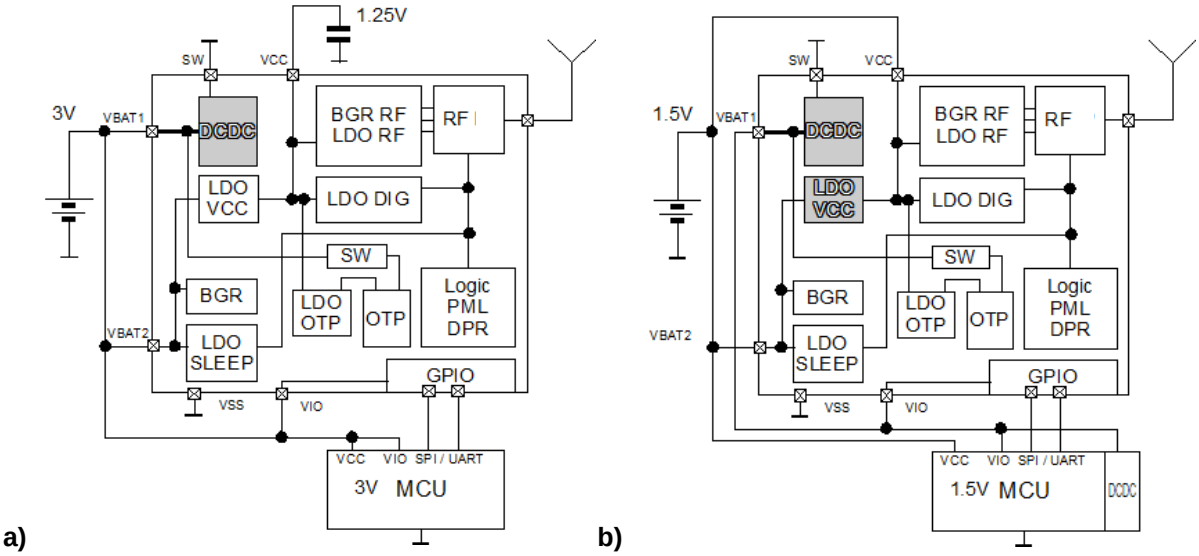


Figure 6: a) DCDC Off Configuration, b) External DCDC Configuration

A summary of the four configuration options and voltage ranges is shown in Table 1. Here is a brief description of each configuration:

- In the DCDC Step-Down Configuration, the battery voltage is applied to VBAT2, VBAT1, and VIO, and can have an operating range of 1.9V – 3.6V. Then 1.25V is generated on VCC by the DCDC voltage.
- In the DCDC Step-Up Configuration, the battery voltage is applied to VBAT2, VCC and VIO, and can have a range of 1.05 to 1.9V. The DCDC generates 2.6V on VBAT1.
- In the DCDC Off Configuration the battery voltage is applied to VBAT2, VBAT1, and VIO and can have a range from 1.9V to 3.6V. Then 1.25V is generated on VCC by the internal LDO.
- In the External DCDC Configuration, the battery voltage is applied to VBAT2 and VCC with an operating range of 1.05V to 1.9V. The external DCDC generates a voltage of 2.6V (up to 3.6V) which is applied to VBAT1 and VIO. In External DCDC Configuration, VBAT1 voltage must be connected at the same time as VBAT2 voltage. If it is not possible, the device must be kept in chip disable mode (ENABLE = '0') till VBAT1 voltage reaches the specified value.
- If VIO is not directly connected to VBAT1/VBAT2, the condition VIO>=VBAT2 must be fulfilled.

Table 1: DCDC Configuration Options

Configuration	VBAT1	VBAT2	VCC	VIO
DCDC Step-Down	VBAT2	1.9V – 3.6V	1.25V, DCDC	VBAT2
DCDC Step-Up	2.6V, DCDC	1.05V – 1.9V	VBAT2	VBAT2
DCDC Off	VBAT2	1.9V – 3.6V	1.25V, LDO	VBAT2
External DCDC	2.6V, MCU DCDC	1.05V – 1.9V	VBAT2	VBAT1

See section 2.3 for the minimal battery supply voltage for RF operations.

The EM9304 can directly be used with the battery types listed in Table 2, for example. Most common 1.5V and 3.0V primary battery cell technologies are directly supported including Lithium, Alkaline, Zinc-Air and Silver Oxide. Other battery types are also supported, for example carbon-printed batteries, but additional decoupling capacitors may be necessary to supply the peak current without the battery level decreasing below the minimum voltage.

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Table 2: Typical Battery Types

Type	Nominal Voltage (V)	Minimum Voltage (V)	Capacity (mAh)
CR1225/CR2032 Li/MnO_2	3.0	2.0	48/225
LR44/AAA Alkaline (Zn/MnO_2)	1.5	0.9	115/1000
ZincAir ZA675	1.4	1.1	650
Silver Oxide (Zn/Ag_2O) 357	1.55	1.2	190

1.5 Operating Modes

The chip has several modes of operation including several active, standby and sleep modes. These modes are described in detail in Section 3.4. Power consumption is optimized in each of these modes. The lowest power mode while maintaining an active connection dissipates 950nA if a 32kHz crystal is used, or 1µA if the internal sleep RC oscillator is used. Additionally, a deep sleep mode is provided with typical current consumption of 650nA, and a chip disable mode is provided with typical current consumption 5nA.

Note that special circuitry is added to keep peak currents to the battery typically less than 12.5mA when transmit power is set to 0.4dBm or lower.

1.6 Pin Description

The pins of the EM9304 are described in Table 35. For the QFN-28 package, the 28 pins and the die attach are described. For the WLCSP25, 21 pins are described (4 unused) and 6 fewer GPIO than QFN.

Analog pins include voltage supply pins, pins for crystal oscillators, and an antenna pin for the RF. Power is supplied through VBAT1, VBAT2, VIO, and VCC depending on the power management configuration described in Section 1.4. Ground is connected to the various V_{SS} pins. Impedance of these connections should be minimized for low noise performance. Ideally they should be connected directly to a ground plane on the PCB using multiple vias where possible. Two pins are provided for the 48MHz crystal (XIN, XOUT) and two are provided for the optional 32kHz crystal (LF_XIN, LF_XOUT). If there is already a 32kHz crystal in the system, the LF_XIN pin can be used to receive a reference signal. The RF antenna is connected to the ANT pin.

Digital pins include general purpose I/O pins (GPIO) and a dedicated input pin for chip enable. There are 12 GPIO pins available on the QFN-28 package and in die form. There are 6 GPIO available on the WLCSP25. Configuration of the GPIO is described in Section 1.7. The chip enable pin (ENABLE) is provided to achieve the lowest possible power consumption (5nA) of the device. The chip is not operational when this pin is low, and then it is initialized when this pin is raised high. VIO supplies the GPIO pins.

1.7 GPIO Configuration

The EM9304 has the digital serial interfaces listed in Table 3, and a complete function list shown in Table 24. These interfaces are available through General Purpose I/O pins (GPIO). These include SPI slave and a UART for an HCI or ACI application interface. The UART can also be used for a test interface and for debug. A SPI master and I2C master are provided for interfacing to external memory or digital sensors for beacon type applications, for example. A JTAG interface is provided for programming and debug.

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Table 3: Digital Interfaces

Interface	Pads	Comment
SPI Slave 16MHz, VIO >=1.9V 8MHz, VIO < 1.9V 5 wires, 8-bit Flow control on dedicated pad	Programmable	HCI/ACI application interface
UART, 9.6kbaud- 1.84Mbaud	Programmable	HCI/ACI test interface
SPI Master 6MHz, VIO >=1.9V 3MHz, VIO < 1.9V 3 or 4 wires, 8-bit	Programmable	External memory or sensors
I2C Master Standard (up to 100kbps) and Fast modes (up to 400kbps)	Programmable	External memory or sensors
JTAG	Fixed	4-pin interface supported

1.8 QFN Reference Schematics and External Components

The typical reference design for a 2-layer PC board for the QFN packaged device in the DCDC step down configuration is shown in Figure 7. The schematic is shown in Figure 7a. The battery voltage is supplied on VBAT2, which can be combined with VIO in most applications. The value of CBAT2 is optimized for CR2032 batteries, for example, but can be adjusted for other battery or power supply types depending on the application. Combined with FB1 and CBAT1, a pi-filter is formed to reduce supply noise generated on VBAT1 by the DCDC converter. This filtering protects the battery from voltage spikes which could reduce battery lifetime. CIO provides additional filtering of high-frequency energy generated by GPIO switching. The inductor LDCDC is used by the DCDC converter to generate the voltage VCC and CVCC filters the switching noise to an acceptable level.

An optional 32kHz crystal (X32M) is shown for the lowest possible sleep mode consumption. Alternately the on-chip RC oscillator can be used with a minor increase in current consumption including required frequency calibration. The 48MHz crystal (X48M) shown is required by the RF for frequency channel accuracy. Other suitable crystals are available but in some cases a frequency offset would need to be trimmed by configuration in OTP. Final selection should be confirmed with EM Microelectronic for correct performance.

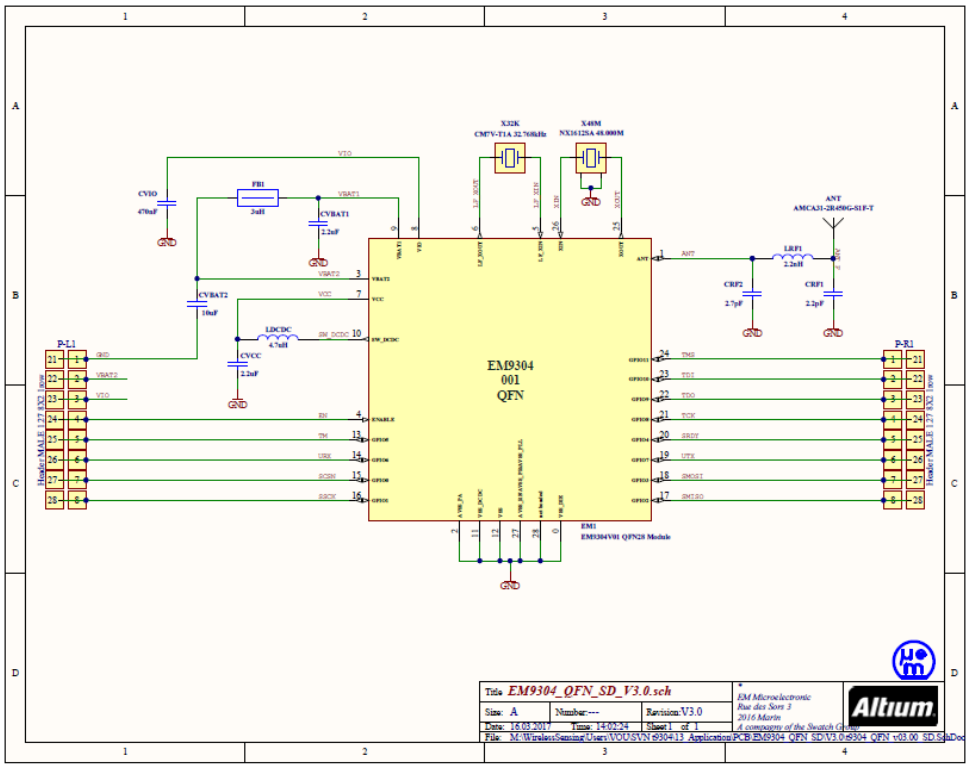
The RF components CRF1, LRF1, and CRF2 are optimized for additional filtering of RF harmonics and matching to the antenna. For custom PCB layout and antennas, these components may need modification. The best cost and performance antenna was chosen for the module. However, other 50ohm Bluetooth or WiFi antennas optimized for the 2.4 GHz ISM band can be used, including custom PCB trace or punched antennas. All PCB designs need to conform to regulatory requirements and relevant certifications need to be obtained (FCC, CE, etc.). Consult EM Microelectronics for additional information.

The reference design layout shown in Figure 7b is a 14x16mm module with all required I/O brought out to pin headers for use on the DVK with castellations for soldering to PCBs. When soldering to other PCBs, care must be taken to keep noisy signals from under the module and away from the RF section. It is required to keep all signals including ground plane from underneath the antenna area. It is preferred to keep the antenna either off of the application PCB or on a corner of the PCB with no ground plane underneath. Preferably the PCB should be removed from under the antenna area. Metal, plastic and other materials (i.e. batteries) shall be kept as far away from the antenna as possible in order not to affect the RF performance.

The module height is < 2.0mm. The module bottom layer has a ground plane. The EM9304 is shown with the QFN-28 pinout. This layout has been optimized for performance and should be used directly on the application PCB with the IO pins removed. The RF and analog sections shall not be modified without careful review by the EM Microelectronics team. The PCB thickness of 0.8mm and 5mil space and trace rules shall also be respected.

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a)



b)

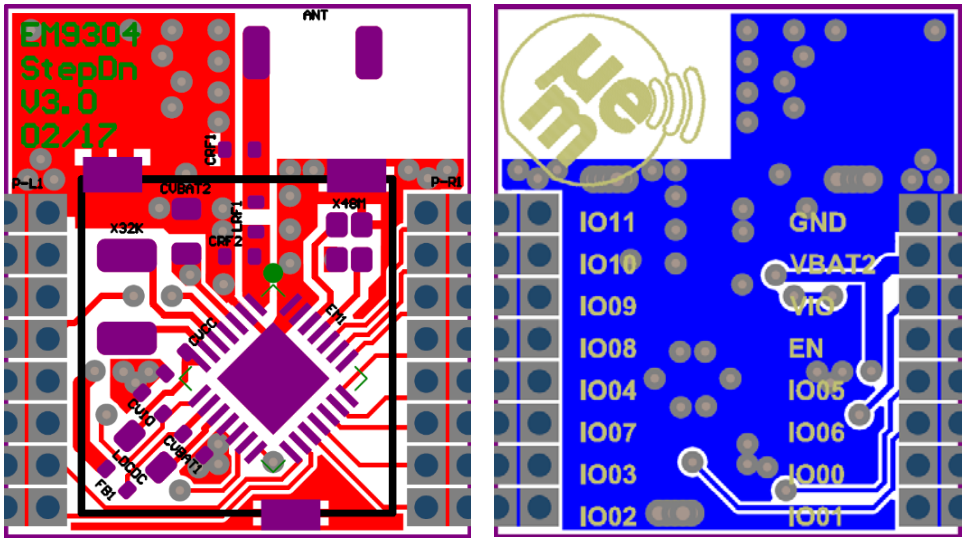


Figure 7: QFN DCDC Step-Down Configuration a) Schematic; b) Layout (Top, Bottom)

A list of recommended components to be used on the reference design is given in Table 4. The required components for the DCDC converter have a very small footprint.

The 470nF and 2.2µF ceramic capacitors are available in an 0402 size. The ferrite bead is also available in an 0402 size, and the DCDC coil is available in an 0603 size. The crystal sizes were chosen for lowest cost, although other suitable crystals are available in a variety of sizes (including smaller ones). A three component RF matching network is shown with 0402 components. This network has been carefully design to optimize RX sensitivity, TX output power, and additional filtering of the second harmonic at 4.8GHz in order to meet FCC requirements at the maximum output power setting. Modification to this network should not be done without consulting EM Microelectronics. Each end product should be verified for compliance with the applicable regulatory requirements and certified by the Bluetooth SIG.

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Altium design files for this and the other power configurations are available upon request.

Table 4: Recommended Component List for the Reference Design

Name	Component	Vendor	Part Number	Specification	Size
U1	Radio	EM Micro	EM9304V01LF28B+	QFN-28	4x4mm
CBAT1	Capacitor	muRata	GRM155R61C225KE11	2.2µF Ceramic 16V X5R	0402
CBAT2	Capacitor	muRata	GRM188R61C106MAAL	10µF Ceramic 16V X5R	0603
LBAT	Ferrite bead	muRata	BLM15HG601SN1	FERRITE BEAD 600 OHM @100MHz	0402
CVCC	Capacitor	muRata	GRM155R61C225KE11	2.2µF Ceramic 16V X5R	0402
LDCDC	Inductor	muRata	LQM18PN4R7MFRL	4.7µH FIXED IND 620MA 550 MOHM	0603
CVIO	Capacitor	muRata	GRM155R61A474KE15D	470nF Ceramic 10V X5R	0402
Q1	Quartz	Micro-Crystal	CM7V-T1A	32.768kHz, 6pF, +/-20ppm	3.2x1.5x0.65 mm
Q2	Quartz	NDK	NX1612SA 48MHz EXS00A-CS10127	48MHz, 10pF, 10ppm	1.6x1.2x0.3 mm
CRF1	Capacitor	muRata	GJM1555C1H2R2BB01	CAP CER 2.2PF 50V NP0	0402
LRF1	Inductor	muRata	LQP15MN2N2B02	INDUCTOR 2.2nH FIXED 300MA 180MOHM	0402
CRF2	Capacitor	muRata	GJM1555C1H2R7BB01	CAP CER 2.7 PF 50V NP0	0402
ANT	Antenna	Abricon	AMCA31-2R450G-S1F-T	2.45GHz, 90MHz BW, -1dBi	3.2x1.6x1.2 mm

1.9 WLCSP Reference Schematics and External Components

The typical reference design for a 2-layer PC board for the WLCSP packaged device in the DCDC step down configuration is shown in Figure 8, with the schematic shown in Figure 8a and PCB layout shown in Figure 8b. The reference design shown is a 10x12mm module. The active portion of the design if the 32kHz crystal and antenna are removed is 5x8mm.

The design is similar to the QFN version previously shown with some important differences. Fewer GPIO are available on the CSP package. GPIO5 is brought out for test reasons, however, if not used in the final application this signal can be left buried. This enables lower cost PCB space and trace design rules (5mil instead of 3mil). Another significant difference is that VBAT1 and VIO have been merged into a single battery voltage to minimize the IO pins on the module. The RF matching network components are also different:

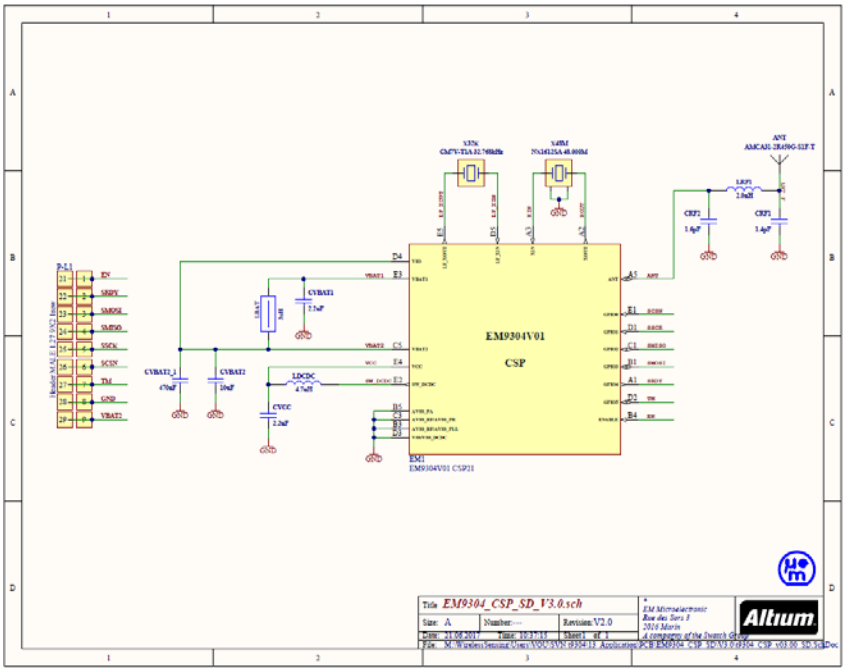
- CRF1 = 1.4pF (GJM1555C1H1R4BB01)
- LRF1 = 2.0nH (LQP15MN2N0B02)
- CRF2 = 1.6pF (GJM1555C1H1R6BB01)

This network has been carefully design to optimize RX sensitivity, TX output power, and additional filtering of the second harmonic at 4.8GHz in order to meet FCC requirements at the maximum output power setting. Modification to this network should not be done without consulting EM Microelectronics. Each end product should be verified for compliance with the applicable regulatory requirements and certified by the Bluetooth SIG.

Altium design files for this and the other power configurations are available upon request.

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a)



b)

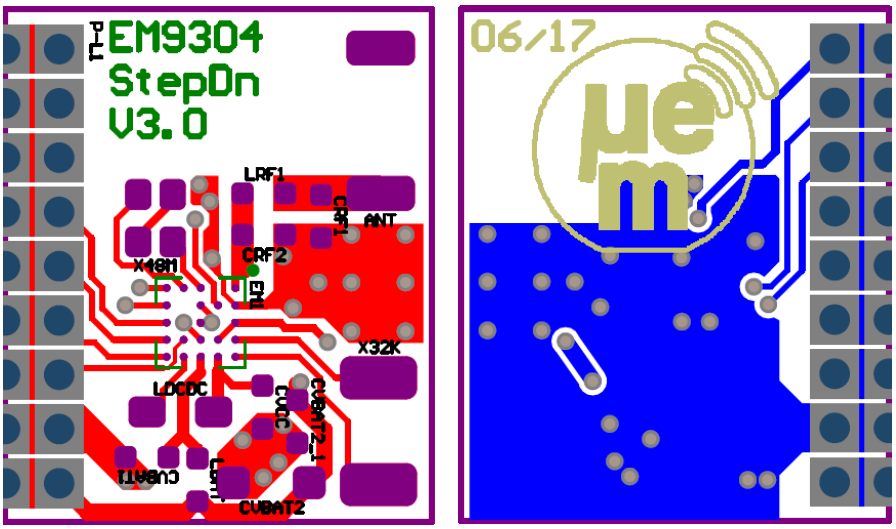


Figure 8: WLCSP DCDC Step-Down Configuration a) Schematic; b) Layout (Top, Bottom)

1.10 Related Documents

The EM9304 was designed to comply with the following Bluetooth specifications published by the Bluetooth Special Interest Group (SIG) on www.bluetooth.org:

[1] Bluetooth Core Specification, Version 5.0, *Bluetooth* SIG, 6.12.2016

[2] Bluetooth RF PHY Test Specification, Version 5.0.0, Bluetooth SIG, 13.12.2016

[3] Bluetooth Link Layer Test Specification, Version 5.0.0, Bluetooth SIG, 13.12.2016

[4] Bluetooth Host Controller Interface (HCI), Version 5.0.0, Bluetooth SIG, 13.12.2016

Customers are however required to test the compliance of their final systems incorporating or embedding the EM9304 with these or other standards as they may apply and to obtain all necessary licenses and authorizations.

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2 Electrical Specifications

2.1 Absolute Maximum Ratings

Table 5 summarizes the absolute maximum ratings for the EM9304. Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Voltage at any ground pin	V_{GND}	-0.2	0.2	V
Battery voltage 1	V_{BAT1}	-0.2	3.9	V
Battery voltage 2	V_{BAT2}	-0.2	3.9	V
Analog Supply Voltage	V_{CC}	-0.2	3.9	V
Voltage at any remaining pin	V_{PIN}	-0.2	3.9	V
RF input power	P_{IN}	---	18	dBm
Storage temperature	T_{st}	-50	150	°C
Electrostatic discharge referred to VSS HBM according to Jedec JS-001	V_{ESDHBM}	-2000	2000	V
Electrostatic discharge referred to VSS CDM according to Jedec JS-002	V_{ESDCDM}	-500	500	V
Maximum soldering conditions	As per Jedec J-STD-020 standard			

2.2 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level unless otherwise specified.

2.3 General Operating Conditions

Table 6 shows the general operating conditions for the EM9304. While the chip is operational down to 1.05V, the output power levels are only guaranteed at the supply voltages specified in the table.

Table 6: General Operating Conditions

All DC voltages are referred to the absolute voltage at the pin VSS.

Parameter	Symbol	Min	Max	Unit
Operating temperature range	T_{op}	-40	85	°C
Operating temperature for OTP write	T_{op_otpw}	-40[1]	85	°C
Battery voltage 1	V_{BAT1_OTP}	2.3[2]	3.6	V
Battery voltage, TX Power Level 0-14	V_{BAT2}	1.05	3.6	V
Battery voltage, TX Power Level 15	V_{BAT2_15}	1.25[3]	3.6	V
Battery voltage, TX Power Level 16	V_{BAT2_16}	1.45[3]	3.6	V
Battery voltage, TX Power Level 17	V_{BAT2_17}	1.7[3]	3.6	V
Analog supply voltage	V_{CC}	1.05	1.9	V

Note 1: Increased write error possible below -20C, rewriting may be required
Note 2: Minimum voltage required for OTP write operation.
Note 3: Output power will decrease automatically if supply voltage drops below this value

The battery voltage is always connected to VBAT2, and alternatively to VBAT1 and VCC; see Figure 6.

The maximum battery ramp-up slope is 3.6V/1µs. The minimum ramp-up slope is 1V/5ms. Care should be taken to avoid a slow Vbat ramp in case of battery bounce type effects.

The minimum slope is not limited in low-voltage configurations.

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2.4 Electrical Characteristics

Unless otherwise specified:

- All DC voltages are referred to the absolute voltage at the pin VSS.
- Typical values are measured at 25°C; minimal and maximal values are measured from -40°C to +85°C.

2.5 DC Characteristics

2.5.1 DCDC Step-Down Configuration

Table 7 shows the DC characteristics in DCDC Step-Down Configuration with 3.0V applied to VBAT2, no OTP usage, and GPIO not toggling. DCDC efficiency is 85%.

Table 7: DC Characteristics, DCDC Step-Down Configuration, VBAT2=3.0V

Parameter	Min	Typ	Max	Unit
RX Mode		3.0		mA
TX mode, TX Power Level 0		2.2		mA
TX mode, TX Power Level 1		2.4		mA
TX mode, TX Power Level 2		2.8		mA
TX mode, TX Power Level 3		2.9		mA
TX mode, TX Power Level 4		3.0		mA
TX mode, TX Power Level 5		3.1		mA
TX mode, TX Power Level 6		3.2		mA
TX mode, TX Power Level 7		3.3		mA
TX mode, TX Power Level 8		3.4		mA
TX mode, TX Power Level 9		3.6		mA
TX mode, TX Power Level 10		3.8		mA
TX mode, TX Power Level 11		4.1		mA
TX mode, TX Power Level 12		4.3		mA
TX mode, TX Power Level 13		4.6		mA
TX mode, TX Power Level 14		5.2		mA
TX mode, TX Power Level 15		5.6		mA
TX mode, TX Power Level 16		7.5		mA
TX mode, TX Power Level 17		9.9		mA
Active RC[1]		0.2		mA
Active XTAL[1]		0.4		mA
ECC ROM execution in a loop		0.7		mA
Coremark test from IRAM1		1.2		mA
Coremark test from OTP		1.6		mA
Sleep mode, LF RC		1.0		µA
Sleep mode, LF XTAL		0.95		µA
Deep Sleep mode		0.65		µA
Chip Disable		5		nA
Battery peak current[2]		10.3		mA

Note 1: CPU halted
Note 2: Typical value using pi-filter in reference schematic. Valid for TX power levels of 0dBm and below.

2.5.2 DCDC Step-Up Configuration

Table 8 shows the DC characteristics in DCDC Step-Up Configuration with VBAT2=1.5V, no OTP usage, and GPIO not toggling, except where indicated.

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Table 8: DC Characteristics, DCDC Step-Up Configuration, VBAT2=1.5V

Parameter	Min	Typ	Max	Unit
RX Mode		5.8		mA
TX mode, TX Power Level 0		4.1		mA
TX mode, TX Power Level 1		4.5		mA
TX mode, TX Power Level 2		5.3		mA
TX mode, TX Power Level 3		5.5		mA
TX mode, TX Power Level 4		5.7		mA
TX mode, TX Power Level 5		5.8		mA
TX mode, TX Power Level 6		6.1		mA
TX mode, TX Power Level 7		6.3		mA
TX mode, TX Power Level 8		6.6		mA
TX mode, TX Power Level 9		6.9		mA
TX mode, TX Power Level 10		7.3		mA
TX mode, TX Power Level 11		7.8		mA
TX mode, TX Power Level 12		8.3		mA
TX mode, TX Power Level 13		8.8		mA
TX mode, TX Power Level 14		9.9		mA
TX mode, TX Power Level 15		10.7		mA
TX mode, TX Power Level 16		12.7		mA
TX mode, TX Power Level 17[1]		14.8		mA
Active RC[2]		0.3		mA
Active XTAL[2]		0.7		mA
ECC ROM execution in a loop		1.3		mA
Coremark test from IRAM1		2.4		mA
Coremark test from OTP		3.2		mA
Sleep mode, LF RC		1.0		µA
Sleep mode, LF XTAL		0.95		µA
Deep Sleep mode		0.65		µA
Chip Disable		5		nA
Battery peak current		21.2		mA

Note 1: Tx Power Level 17 requires a minimum VBAT=1.7V
Note 2: CPU halted

2.5.3 DCDC Off Configuration and External DCDC Configuration

Typical currents in DCDC Off Configuration and External DCDC Configuration are similar to those in Step-Up Configuration shown in Table 8 except for battery peak current.

2.6 Digital Pin Characteristics

2.6.1 GPIO Pin Characteristics

The GPIO pin characteristics are described in Table 9. Functions implemented are a digital input, push-pull output, selectable pull-down/pull-up resistors, 3.3V standard protections against VSS and VIO.

Table 9: GPIO Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Schmidt trigger hysteresis	Vhys		0.05*VIO			V
Input low level	Vil	VIO >= 1.9V			0.3*VIO	V

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		VIO < 1.9V			0.15*VIO	V
Input high level	Vih	VIO >= 1.9V	0.7*VIO			V
		VIO < 1.9V	0.85*VIO			V
Output voltage low	Vol_low1	IOUT=3mA VIO=1.9V			0.4	V
Output voltage low	Vol_low2	IOUT=0.8mA VIO=1.05V			0.21	V
Output voltage high	Voh_high1	IOUT=-3mA VIO=1.9V	1.5			V
Output voltage high	Voh_high2	IOUT=-0.8mA VIO=1.05V	0.84			V
Pull up/down resistor GPIO5	Rpull5		8	10	18	kΩ
Pull up/down resistor other GPIO	Rpull		70	100	130	kΩ

Output parameters for I2C mode are shown in Table 10.

Table 10: I2C Output Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output voltage low	Vol_low1	IOUT=3mA VIO=1.9V	0.1			V
Output voltage low	Vol_low2	IOUT=2mA VIO=1.05V	0.21			V

2.6.2 I2C Timing

The timing characteristics for GPIO pins capable of an I2C interface (GPIO0-1 and GPIO4-9) are according to I2C Specification V3.0. Otherwise these pins have the timing specification described in Table 11 I2C Capable GPIO Timing Characteristics.

Table 11: I2C Capable GPIO Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output delay, falling edge (VBAT =1.05V to 3.6V)	t_{ODEL_F}	Output load 25pF Output load 150pF Output load 400pF			500 520 540	ns ns ns

2.6.3 SPI Timing

The SPI timing signals are shown in Figure 9. The SPI timing specification for VBAT > 1.9V (ie Step-Down and DCDC-Off Configuration) is shown in Table 12. The SPI timing specification for VBAT < 1.9V (ie Step-Up or External DCDC Configuration) is shown in Table 13.

To achieve the required SPI maximum frequency, the SPI slave is changing the MISO value at the opposite edge compared to industry practice (on the same edge when value sensing is done). All known SPI masters require MISO hold time < 10ns, so the device is working in all applications. Nevertheless, this change could cause SPI protocol detection problem in some standard logic analysers with sampling frequency below 100MHz.

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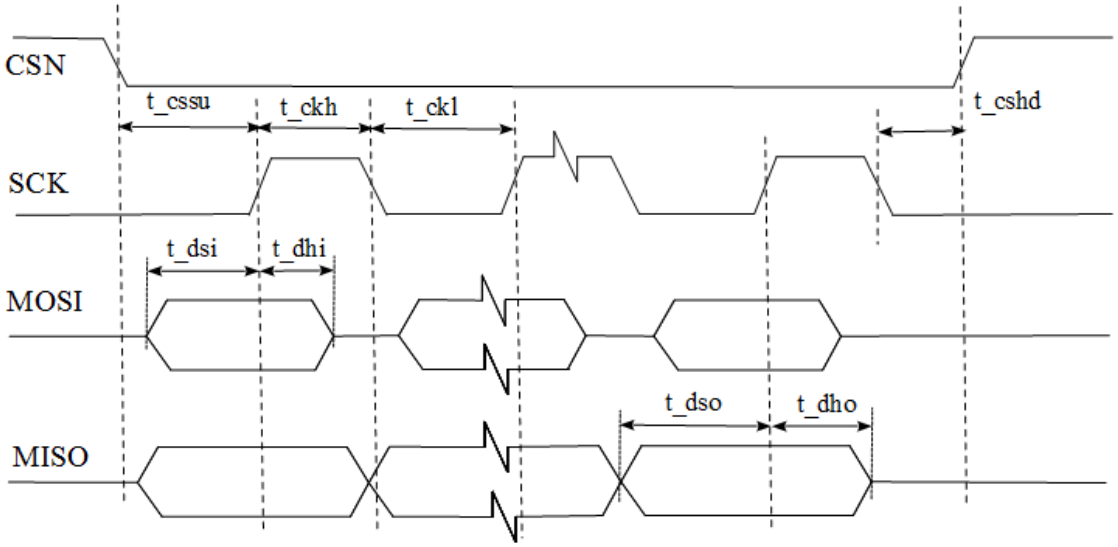


Figure 9: SPI Timing

Table 12: SPI Timing Specification for VBAT > 1.9V

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency Slave	t_frq_s			16	MHz
Clock frequency Master	t_frq_m			6	MHz
Data setup time (input)	t_dsi	10			ns
Data hold time (input)	t_dhi	10			ns
Data setup time (output)	t_dso	(1/t_frq) - 46ns			ns
Data hold time	t_dhd	13			ns
CSN setup time	t_cssu	100			ns
CSN hold time	t_cshd	100			ns
Data setup time Master (input)	t_dsim	35			ns
Data hold time Master (input)	t_dhim	10			ns

Table 13: SPI Timing Specification for VBAT < 1.9V

Parameter	Symbol	Min	Typ	Max	Unit
Clock frequency Slave	t_frq_m			8	MHz
Clock frequency Master	t_frq_s			3	MHz
Clock pulse width low	t_ckl	0.4/t_frq			µs
Clock pulse width high	t_ckh	0.4/t_frq			µs
Data setup time (input)	t_dsi	10			ns
Data hold time (input)	t_dhi	10			ns
Data setup time (output)	t_dso	(1/t_frq) - 46ns			ns
Data hold time	t_dhd	13			ns
CSN setup time	t_cssu	100			ns
CSN hold time	t_cshd	100			ns
Data setup time Master (input)	t_dsim	60			ns
Data hold time Master (input)	t_dhim	10			ns

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2.6.4 Enable Pin Characteristics

Enable pin characteristics are shown in Table 14.

Table 14: Enable Pin Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input voltage low	Vil				0.4*VBAT2	V
Input voltage high	Vih		0.6*VBAT2			V

2.7 Power Management Characteristics

2.7.1 Low Frequency Crystal Oscillator Specifications

The general specifications for the low frequency crystal oscillator are shown in Table 14.

Table 15: Low Frequency Crystal Oscillator Specifications

Parameters	Comments	Symb.	Min	Typ	Max	Units
Crystal frequency	Fundamental	f_{LFXTAL}		32.768		kHz
Crystal deviation	Including frequency tolerance, stability over temperature, aging, and total tolerances of external capacitances	$df0/f0_{LFXTAL}$	-300[1,2]	-20		ppm
Typical supported crystal parameters	Equiv. series Res.	ESR_{LFXTAL}		55	100	kΩ
	Differential equivalent load capacitance (13)	CL_{LFXTAL}		6		pF

Note 1: Valid for crystal specified in Table 4
Note 2: Much better precision can be obtained using the on-chip calibration system

2.7.2 Timing Characteristics

The typical start-up time for each power configuration is listed in Table 16. Start-up time is defined as ENABLE pin high until RDY pin high, when the device is ready to receive an HCI/ACI command. The times listed assume a SPI transport layer is used and only trimming information is stored in OTP and no other patches are stored in OTP. The times assume the components listed in Table 4 are used. When a 32kHz crystal or external input is used, a cold start counter runs for 1 second before releasing the CPU for general usage.

Table 16: Start-Up Characteristics

Configuration	Comment	Min	Nom	Max	Units
Step-Down, DCDC Off	VBAT=3.0V, ramp=0.3V/µs, LF RC		3.6		ms
Step-Up	VBAT=1.5V, ramp=0.3V/µs, LF RC		5.0		ms
External-DCDC	VBAT=1.5V, ramp=0.3V/µs, LF RC		3.2		ms
Any	32kHz crystal or external signal is used		1.2		s

Timing characteristics from sleep to active modes are listed in Table 17. The transition is started by a wake-up event (pad or sleep timer) and finishes when the device is ready to receive an HCI/ACI command. The times listed assume only trimming information is stored in OTP and no other patches are stored in OTP. The times assume the components listed in Table 4 are used.

Table 17: Timing Characteristics

Mode 1	Mode 2	Comment	Min	Nom	Max	Units
Sleep	Active XTAL	HCI/ACI command RDY Depends on crystal Q		1.1		ms

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2.8 RF Characteristics

All the RF parameters are measured using the reference design presented in Section 1.8. Parameters are compliant to [1] (Bluetooth Core Specification Version 5.0, Volume 6, Part A). Measuring conditions and device configuration are specified in [2] (RF PHY Bluetooth Test Specification: RF-PHY.TS.5.0.0) for PHY parameters and in [3] (Link Layer Bluetooth Test Specification: LL.TS.5.0.0) for LL parameters.

2.8.1 General RF Characteristics

General RF characteristics are listed in Table 18.

Table 18: General RF Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
RF input impedance	Single ended	Z_{IN}		50[1]		Ω
Input reflection coefficient	All channels	S_{11}			-8	dB
Data rate	BT LE 1M PHY	R_{BT}		1000		Kbps

Note 1: The impedance is measured at the antenna port of the QFN reference design in Section 1.8 and WLCSP reference design in Section 1.9. The RF matching network has been optimized for RX sensitivity, TX output power, and spurious emissions of the second harmonic at 4.8GHz at the maximum output power setting.

2.8.2 High Frequency Crystal Oscillator Specifications

The general specifications for the high frequency crystal oscillator are shown in Table 19.

Table 19: High Frequency Crystal Oscillator Specifications

Parameters	Comments	Symb.	Min	Typ	Max	Units
Crystal frequency	Fundamental	f_{XTAL}		48[1]		MHz
Crystal deviation	Including frequency tolerance, stability over temperature, aging, and total tolerances of external capacitances	df0/f0			±50	ppm
Typical supported Xtal parameters	Equiv. series Res.	ESR_{XTAL}	20		80	Ω
	Differential equivalent load capacitance (13)	CL_{XTAL}[2]	6	8	10	pF

Note 1: The crystal oscillator center frequency should be trimmed to exactly this frequency in the final application
Note 2: The crystal oscillator startup current should be adjusted based on the crystal load capacitance chosen
Contact EM Microelectronic for more information on how to make these adjustments

2.8.3 Transmitter Characteristics

Transmitter characteristics are shown in Table 20.

Table 20: Transmitter Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
Output power	TX Power Level = 0[1]	P_{TX0}		-33.5		dBm
	TX Power Level = 1[1]	P_{TX1}		-29.0		dBm
	TX Power Level = 2	P_{TX2}		-17.9		dBm
	TX Power Level = 3	P_{TX3}		-16.4		dBm
	TX Power Level = 4	P_{TX4}		-14.6		dBm
	TX Power Level = 5	P_{TX5}		-13.1		dBm
	TX Power Level = 6	P_{TX6}		-11.4		dBm
	TX Power Level = 7	P_{TX7}		-9.9		dBm
	TX Power Level = 8	P_{TX8}		-8.4		dBm
	TX Power Level = 9	P_{TX9}		-6.9		dBm
	TX Power Level = 10	P_{TX10}		-5.5		dBm
	TX Power Level = 11	P_{TX11}		-4.0		dBm

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Parameters	Comments	Symb.	Min	Typ	Max	Units
	TX Power Level = 12	P_{TX12}		-2.6		dBm
	TX Power Level = 13	P_{TX13}		-1.4		dBm
	TX Power Level = 14	P_{TX14}		0.4		dBm
	TX Power Level = 15	P_{TX15}		2.5		dBm
	TX Power Level = 16	P_{TX16}		4.6		dBm
	TX Power Level = 17	P_{TX17}		6.2		dBm
Power in 2nd harmonic[2]	Output power step = 17 50 Ω for "Typ" value. PT for "Max" value Matching network defined in sections 1.8 and 1.9.	P_{TX2}		-50		dBm
Power in 3rd harmonic[2]		P_{TX3}		-60		dBm
Power in 4th harmonic[2]		P_{TX4}		-60		dBm
Deviation from the channel center frequency		Δf_c	-150		150	kHz
Frequency drift for any packet length		Δf_{c_pkt}			50	kHz
Drift rate		$\Delta f_c/\Delta T$			400	Hz/µs
Modulated frequency deviation		Δf_{mod}		±250		kHz
In-band spurious emission, power transmitted outside the selected channel, at a frequency offset f_{offs}	$\lvert f_{offs} \rvert$ = 2MHz	P_{out} (f_c+f_{offs})			-20	dBm
	$\lvert f_{offs} \rvert$ ≥ 3MHz				-30	dBm

Note: All measurements as described in RF PHY Bluetooth Test Specification Version 5.0.0
Note 1: TX Power Level 0 and 1 do not comply with BT PHY requirements and should be used at risk only after complete evaluation in the desired application
Note 2: Measured on DCDC Step-Down Configuration reference module described in Section 1.8.

2.8.4 Receiver Characteristics

Receiver characteristics are shown in Table 21.

Table 21: Receiver Characteristics

Parameters	Comments	Symb.	Min	Typ	Max	Units
Sensitivity	1Mbps, 37 byte payload			-94		dBm
	1Mbps, 255 byte payload			-93		dBm
Maximum input power	1Mbps, 255 byte payload			0		dBm
In-band blocking (-67dBm desired signal)	Co-channel interference (i.e.0MHz)	C/I_{0_MHz}		6		dB
	Adjacent ±1MHz interference	$C/I_{\pm1_MHz}$		-4		dB
	Adjacent +2MHz interference	C/I_{+2_MHz}		-25		dB
	Adjacent -2MHz interference (image)	C/I_{-2_MHz}		-18		dB
	Adjacent +3MHz interference	C/I_{+2_MHz}		-33		dB
	Adjacent -3MHz interference (next to image)	C/I_{-2_MHz}		-32		dB
	Adjacent ≥±4MHz and ≤±10MHz interference	C/I_{4-10_MHz}		-35		dB
	Adjacent ≥±10MHz interference	$C/I_{\geq10_MHz}$		-43		dB
Out-of-band blocking (-67dBm desired signal)	30MHz – 2000MHz		-30			dBm
	2003MHz – 2399MHz (excepted for f_{RF}-96MHz)		-35			dBm
	2484MHz – 2997MHz (excepted for f_{RF+}96MHz)		-35			dBm
	3000MHz – 12.75GHz		-30			dBm
Intermodulation	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm3$MHz			-45		dBm
	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm4$MHz			-45		dBm
	$f_{RX}=2*f_1-f_2$ and $f_2-f_1=\pm5$MHz			-45		dBm
Spurious emissions	F=30MHz – 88MHz				-57.4	dBm

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	F=88MHz-1GHz				-57	dBm
	F=1GHz-12.75GHZ				-47	dBm

Note: All measurements as described in RF PHY Bluetooth Test Specification Version 5.0.0

An RSSI circuit with 60 dB nominal range is available and suitable for use in some applications. However, the accuracy is not guaranteed and should be thoughoughly evaluated in the final application to ensure it meets the desired needs. Typically the RSSI value should be ignored in most applications.

3 Functional Description

This section provides a functional description of the EM9304. A block diagram of the IC is described in Section 3.1. There are subsections on the digital processing capability, CPU, memories, applications and patch loading, peripherals, and security. Peripherals are described in detail in Section 3.2. The power management is described in Section 3.3, including subsections on the power supply domains, the DCDC converter function, power supply monitoring, chip enable, and the reset structure. The operating modes are described in Section 3.4, including a description of the start-up procedure and the sleep mode store and restoration procedures. The clock structure is described in Section 3.5.

3.1 Block Diagram

A block diagram of the EM9304 is shown in Figure 10 with the power management configured in DCDC Step-Down Configuration. The main blocks are the Digital Processing Block (DPR), the RF block, the Power Management Logic (PML), the Power Management Blocks, and the General Purpose Input Output blocks (GPIO).

The Power Management Blocks are scattered throughout the design and will be described first. The battery is connected to VBAT1 and VBAT2. The DCDC block generates VCC through the switching node and external filter. (VCC is optionally generated by the LDO_VCC block if the external filter is not present.) A number of power management blocks are connected to VBAT2 including a low-power bandgap voltage reference circuit (BGR_PWR), a supply voltage level detector (SVLD), a low drop-out regulator for the one-time programmable (OTP) memory (LDO_OTP), a low-frequency RC oscillator (LF_RC), a low-frequency crystal oscillator (LF_XTAL), a temperature dependant bias generator (PTAT), and a power-on-reset (POR) block. OTP writing requires 2.25V minimum to operate and so the OTP is also connected to VBAT1 through a switch. The SVLD uses a precision bandgap (BGR_PWR) voltage reference for accurate voltage level. The main low drop-out regulators for the IC are connected to VCC, which include three regulators for the RF block (LDO_PA for the power amplifier, LDO_PLL for the frequency synthesizer, and LDO_RF for the remaining RF circuits), the DPR block (LDO_DIG), and a linear regulator used for sleep mode (LDO_SLEEP). The DPR uses BGR_PWR for a voltage reference, while the RF regulators use a low-noise bandgap circuit (BGR_RF) which is only powered when the RF block is active. The LF_XTAL block operation is optional but requires an external 32.768kHz quartz crystal if used.

The power management logic (PML) is powered from LDO_DIG when the EM9304 is in active mode and by LDO_SLEEP when in sleep mode. (The modes of the EM9304 are described in Section 3.4.) The PML block includes digital control circuits for the clock, reset, pads, DCDC converter, analog circuits, and other system functions. The sleep timer is also included in the PML and is driven by the active low-frequency oscillator (LF_RC or LF_XTAL) to track when it is time to come out of sleep mode.

The DPR includes the central processing unit (CPU), memory, and peripherals. Memories includes 2 x 4kB and one 12kB SRAM for data and retention, one 8kB SRAM for data without retention, one 4k SRAM for the dynamic program jump table which is optionally retained, one 48k SRAM for program development and debug, and a 128k instruction ROM plus 8kB data ROM for the dedicated chip firmware (contains the start-up program, hardware drivers, scheduler, memory manager, Bluetooth link-layer, and the Bluetooth stack). Peripherals include two timers (a protocol timer and a universal timer), a UART, an SPI master, SPI slave, I2C master, and GPIO control. The DPR is powered from LDO_DIG, but has several power domains for each memory. The GPIO themselves are shown as a separate block because they are powered by a separate supply voltage (VIO) and can drive an external load.

The RF block operates at 2.4GHz and includes a transmitter (TX) with a programmable power amplifier (PA), a receiver (RX), and a phase-locked loop (PLL) frequency synthesizer. The PLL includes a high frequency crystal oscillator (HF_XTAL), which requires an external 48MHz quartz crystal. The RF has a significant portion implemented in logic including the modem, packet processing, and encryption, which is interfaced to the DPR CPU bus.

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Level shifters (LS) are included between the various power domains to prevent cross-domain currents.

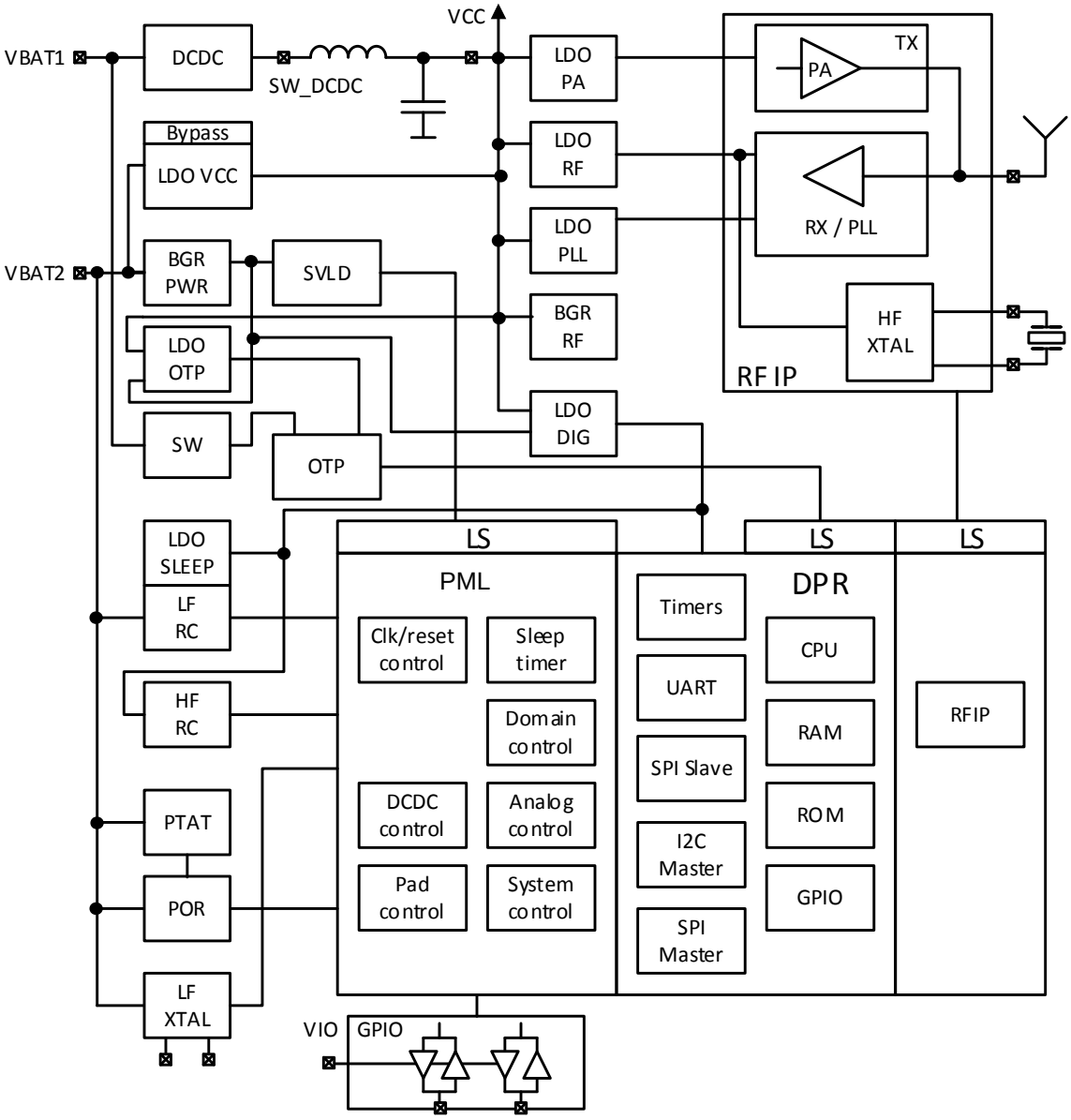


Figure 10: Block Diagram Configured In Step-Down Configuration

3.1.1 Digital Processing

The digital process block (DPR) is designed as CPU based system with closed coupled instruction and data memories and peripherals connected as slaves to a bus. All data and control transactions are done by register access without DMA control. The RF block is connected as a peripheral device.

3.1.2 CPU

The CPU is a 32-bit ARC EM4 V3.2 by Synopsys, with an integrated floating point unit (FPU), which is optimized for area, power, and performance efficiency. The ARC's RISC pipe-lined architecture with mostly single-cycle operations is approximately 30% more efficient than other popular 32-bit CPUs. Effective use of the sleep instruction minimizes power consumption. The CPU is awakened on an interrupt, quickly executes the required functions with a 24MHz clock, and returns to sleep. A hardware interrupt handler is implemented with several interrupt levels in order to define high and low priority functions.

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There are four additional CPU coprocessors: 1) an AES-128 crypto engine, 2) LOG2, 3) JLI_Rebase, and 4) a CRC calculator. Dedicated CPU instructions are defined to run AES encryption/decryption, calculate a log2() function, a function to help with rebasing the JLI table, and a function to calculate CRC values respectively.

The ARC processor is supported with a commercially available MetaWare toolkit (compiler, linker, debugger, etc.) and free GCC tools. An integrated development environment (IDE) and software development kit (SDK) customized for the EM9304 implementation, can easily be used to link to functions embedded in ROM, implement patches, implement code in RAM or OTP, and execute code from RAM or OTP. A 4-wire JTAG interface is provided in the QFN package format for debugging.

3.1.2.1 Floating Point Unit

The ARC also includes a Floating Point Unit (FPU) compliant with the IEEE 754-2008 specification:

- Full support for quiet and signaling NaN, infinity and sub-normals
- Support for all IEEE specified rounding modes

The FPU has single precision hardware support for multiply, add, subtract, integer/float conversions, compare, divide, and square root. All FPU operations are supported by the Metaware compiler for ARC EM4

3.1.3 Memories

Code memory is split to ROM, RAM and OTP and use is optimized for power consumption. In sleep mode ROM can be shut off without losing its contents while RAM will lose its contents and needs to be reloaded. Therefore all critical functions for Bluetooth low energy controller and host are implemented in the ROM.

48kB RAM is available for application and patch development. These can then be moved into OTP for production. The patching system is based on using instruction index tables and dedicated CPU instructions. (Refer to Section 5.3.1.4) All functions that are to be patched must use index table call. The index table is loaded from ROM into RAM and rebuilt during the boot process. It is also rebuilt when waking from sleep mode if IRAM0 is not specified for retention.

28kB of RAM is provided for data. Either 4kB, 8kB, or 20kB of that data RAM can be specified as retention memory which is kept active during sleep mode at the expense of additional leakage current. Data in non-retention memory is lost during sleep mode.

128kB OTP is available for instructions or data. Trimming, configuration data, Bluetooth profiles and services, an application, and code patches can be installed into OTP during manufacturing or at a later time in the field using the over-the-air firmware (FOTA) updating mechanism. Code can be executed from OTP or copied to RAM for execution, whichever is more power efficient.

The EM9304 memories are described in Table 22. Refer to Section 5.2.1 for more details.

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Table 22: Memories

Name	Type	Size	Usage	RAM Retention	Address Range
IROM	ROM	128kB	CPU program, boot, LL, Host		0x000000 0x01FFFF
IRAM1	SRAM	48kB	CPU program, to be loaded from OTP or serial interface	No	0x020000 0x02BFFF
IRAM0	SRAM	4kB	CPU instruction index table	Optional	0x030000 0x030FFF
Empty					0x031000 0x0FFFFF
OTP	OTP	128kB	CPU program, profiles, applications	N/A	0x100000 0x11FFFF
Empty					0x120000 0x7FFFFF
DRAM0	SRAM	4kB	CPU data, unique ID, configuration	Yes	0x800000 0x800FFF
DRAM1	SRAM	4kB	CPU data	Optional	0x801000 0x801FFF
DRAM2	SRAM	12kB	CPU data	Optional	0x802000 0x804FFF
DRAM3	SRAM	8kB	CPU data	No	0x805000 0x806FFF
Empty					0x807000 0x807FFF
DROM	ROM	8kB	SW constants		0x808000 0x809FFF

3.1.4 Peripherals

Peripherals include an I2C master, SPI master, UART, SPI slave, GPIO, and timers. These are discussed in detail in Section 3.2.

3.1.5 Applications and Patch Loading

The DPR can be configured as a Bluetooth controller or host, software can be developed in RAM, and software can be permanently installed in OTP.

3.1.5.1 Bluetooth Controller

When configured as a Bluetooth controller, the GPIO is configured as an SPI slave as the HCI transport layer by default. Alternatively the GPIO can be configured as a UART to be used for the HCI transport layer. In this configuration, the EM9304 responds to all valid HCI commands on the activated transport layer and generates the proper HCI events.

3.1.5.2 Bluetooth Host

When configured as a Bluetooth host, the GPIO is configured as an SPI slave as the ACI transport layer by default. Alternatively the GPIO can be configured as a UART to be used for the ACI transport layer. In this configuration, the EM9304 responds to all valid ACI commands on the activated transport layer and generates the proper ACI events.

3.1.5.3 Software Development

When configured for software development, software can be developed with the ARC EM4 Metaware IDE and downloaded into SRAM using the proper JTAG programmer (not included). A software development kit (SDK) can be obtained from EM Microelectronic with supporting functions, API, and examples. Note the WLCSP version does not have the proper JTAG pins for software development; only the QFN version can be used. A hardware development kit (DVK) can be obtained from EM Microelectronic with the proper package version and a configurable PCB.

Additionally, software can be loaded into RAM from external EEPROM or Flash through the I2C or SPI interface, or from an external microcontroller.

3.1.5.4 Software Installation

After proper software development and verification, the object code can be loaded into OTP using tools supplied by EM Microelectronic. Object code examples include link-layer or stack patches,

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user defined functions (vendor specific HCI commands, for example), Bluetooth profiles, or a small Bluetooth application such as a sensor beacon.

3.1.6 Security

The security features are implemented in a combination of digital hardware and software functions which are described in Table 23. A hardware based true random number generator is implemented which complies with the NIST 800-90A standard. Packet encryption and decryption is implemented in hardware with an AES-128 core embedded in-line with the RF packet processor block which allows the operation to be performed on the fly. (A second AES-128 block is included for non-real-time operation.) Finally, the EEC P-256 function is implemented in software for key generation.

Table 23: Security Features

Feature	Bluetooth Specification	Implementation
Random data generation	Vol 2, Part H, Section 2	True RNG based on logic Pseudo RNG: NIST, Recommendation for Random Number Generation Using Deterministic Random Bit Generators, Special Publication 800-90A, January 2012 Variant with block cipher (AES)
Packet encryption and authentication	Vol 6, Part E	HW block in RF IP packet processor with AES core embedded to compute MIC and encrypt/decrypt a packet on the fly
Key generation	Vol 3, Part H, Section 2.4	Implemented in SW included ECC P-256 function

3.2 Peripherals

Peripherals include an I2C master, SPI master, UART, SPI slave, GPIO, and timers. The SPI slave includes flow control for maximum transfer efficiency. The I2C master and SPI master have 16 byte buffers. The UART slave and SPI slave have FIFOs implemented with the following features:

- 64 byte FIFOs for reception (RX) and transmission (TX)
- 1, 2, 3 or 4 byte register reads from RX FIFO or writes to TX FIFO
- FIFO status register information:
  - TX FIFO empty
  - TX FIFO exceeds user defined limit
  - RX FIFO exceeds user defined limit
  - RX FIFO full
  - Number of bytes in each FIFO.
- Individual FIFO flush commands to remove all content
- Interrupt vectors:
  - TX interrupts:
    - Byte sent
    - TX FIFO empty
    - TX FIFO limit
    - TX FIFO underflow
  - RX interrupts:
    - Byte received
    - RX FIFO full
    - RX FIFO limit
    - RX FIFO overflow
  - Additional UART interrupts
    - Frame error detected (wrong stop bit)
    - Parity error detected

3.2.1 I2C Master

The I2C master peripheral supports following features in addition to the FIFOs:

- Supported speeds:
  - Standard mode (up to 100 kbps)

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    - Fast mode (up to 400 kbps)
    - Speed is configurable by register
- Clock stretching
- Addressing modes:
    - 7-bit device addressing mode
- I2C enable/disable
- 16 byte RX buffer for reception and 16 byte TX buffer for transmission
- I2C transactions:
    - Write: 1) start bit, 2) device address, 3) memory/register address to write, 4) data to write (N bytes), 5) stop bit
    - Simple read: 1) start bit, 2) device address, 3) data to read (N bytes), 4) stop bit
    - Complex read: 1) start bit, 2) device address, 3) memory/register address to read, 4) repeated start bit, 5) device address, 6) data to read (N bytes), 7) stop bit
    - I2C Device address in separate register with configurable length (7 or 10 bits)
    - Memory/register address to read/write in separate register, 1 bytes, configurable length
    - Number of bytes to send/receive can be 1-256; sending/receiving started by writing to control register
- Number of bytes sent/received in last transaction
- Stopping current transaction (after finishing current byte)
- Status flags:
    - I2C transaction status (busy flag)
    - Start condition detected
    - Stop condition detected
    - No ACK detected
    - Clock stretching by slave
- IRQs:
    - End of sequence

3.2.2 SPI Master

The SPI master peripheral supports following features in addition to the FIFOs:

- 3 wire SPI interface (SCK, MISO, MOSI)
    - Note: CSN should be generated through GPIO by software
- Full duplex communication
- Configurable clock speed derived from system clock by power of 2, starting at 6MHz
- Clock rates up to 3MHz VIO < 1.9V, and 6MHz VIO>= 1.9V
- Motorola compliant, all 4 SPI clock polarity/phase configurations supported (CPOL = 0,1; CPHA = 0,1)
- SPI enable/disable
- 16 byte RX buffer for reception and TX buffer for transmission
- One shot mode: Number of bytes to send/receive is configured (1-16 bytes).
    - Sending/receiving is started by a register write
- Status flags:
    - Busy
- IRQs:
    - End of transaction
- Configurable bit order (LSB first or MSB first)

Note the SPI Master must set a pull resistor to MISO till RDY=1 or tolerate a High-Z state on MISO.

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3.2.3 UART

The UART peripheral supports following features in addition to the FIFOs:

- 2 wire interface without flow control (TX, RX)
- 4 wire interface with flow control (TX, RX, CTS, RTS)
- Full duplex communication
- 1 start bit, 8 data bits, and 1 stop bit
- Even, odd, or no parity
- Configurable speed
  - Supported speeds: 9600Bd, 14400Bd, 19200Bd, 28800Bd, 38400Bd, 57600Bd, 76800Bd, 115200Bd, 230400Bd, 460800Bd, 921600Bd, 1843200Bd
  - Other “non-standard” speeds also supported
  - Default speed 115200Bd
- Flow control (CTS, RTS signals) enable/disable
- Separate TX/RX enable
- Configurable bit order (LSB first or MSB first).

3.2.4 SPI Slave

The SPI slave peripheral supports following features in addition to the FIFOs:

- 4 wire SPI interface (SCK, CSN, MISO, MOSI) with flow control (RDY output signal)
- Half duplex communication, write or read determined by a control byte
- Clock rates up to 8MHz VIO < 1.9V, and 16MHz VIO>= 1.9V
- Motorola compliant:
  - clock polarity CPOL = 0 (clock is inactive low)
  - clock phase CPHA = 0 (data is valid on clock rising edge)
- All 4 SPI clock polarity/phase configurations
- SPI enable signal
- Flow control enable/disable
- Configurable bit order (LSB first or MSB first)
- Multi byte transactions (without de-asserting CSN between bytes)

3.2.4.1 SPI Slave Flow Control

The SPI Slave flow control can be used in two different ways depending on the SPI Master capability or preferences. In all cases the RDY signal is needed and it shall be connected on the SPI Master side as an input pin preferably with interrupt capability. The beginning of a SPI transaction is always same: the SPI Master asserts CSN to '0', waits until RDY is at '1' and then sends 2 header bytes and reads the status bytes STS1 and STS2. The rest of the SPI transaction is different depending on the way flow control is used on the SPI Master.

3.2.4.2 Flow Control Using RDY

In this case RDY is used as information from EM9304 indicating SPI buffer ready status. The SPI Master has to check RDY after each transmitted byte. If RDY is at '1' SPI Master can transmit another byte. If RDY is at '0' SPI Master may not transmit another byte and SPI Master has to wait until RDY goes to '1'. Once RDY is at '1' again SPI Master can continue to transmit additional byte(s). This approach allows SPI Master to send/receive unlimited number of bytes in single SPI transaction thanks to RDY providing updated status of SPI buffer after each transmitted byte.

An example of write transaction using RDY as a flow control during transaction is shown in Figure 11.

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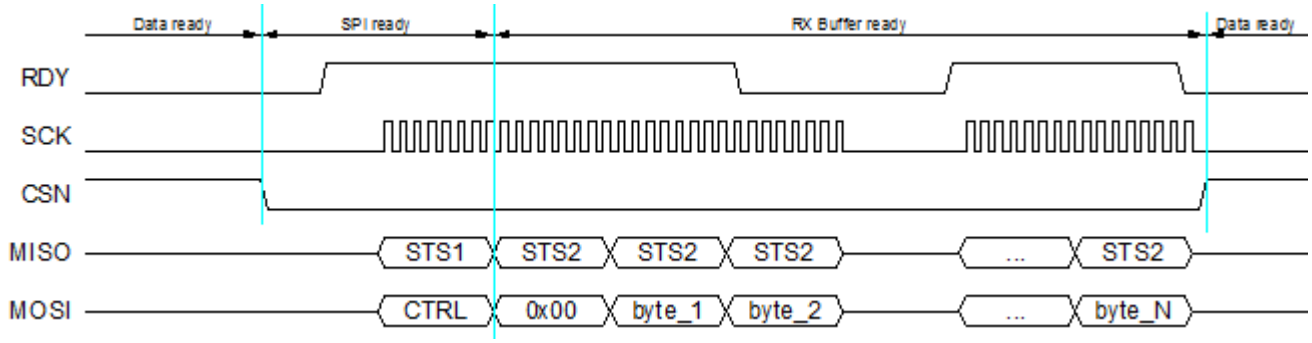


Figure 11: SPI Slave Write Transaction with Active Flow Control by Means of RDY

In this approach, the RDY signal has to be checked by the Master after each transmitted byte which may insert gaps into SPI transaction. In case the SPI Master uses DMA, this method might be difficult or impossible, unless the DMA can be triggered by the RDY pin.

3.2.4.3 Flow Control Using Status Byte STS2

A Master with DMA, using the status byte STS2, can run an SPI transaction without interruptions. In this case SPI Master can ignore RDY during the SPI transaction and use instead the status byte STS2 to determine the maximum length of the SPI transaction. Once maximum length of SPI transaction is known (from STS2), the SPI Master can configure the DMA to realize the rest of the SPI transaction. After transmitting the given number of bytes (less than or equal to maximum length determined from STS2) SPI transaction shall be finished by de-asserting CSN. A new SPI transaction shall start by asserting CSN and reading status bytes to determine maximum length of this new transaction.

Examples of transactions ignoring RDY are shown in Figure 12 and Figure 13.

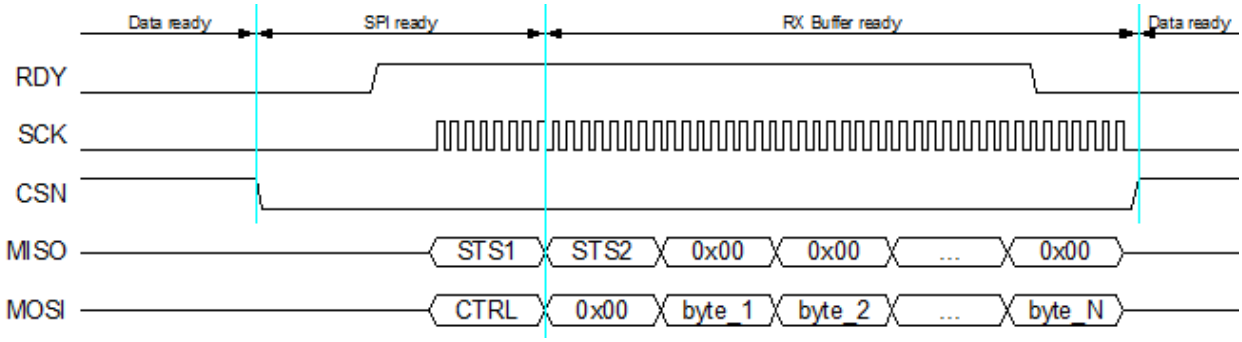


Figure 12: SPI Slave Write Transaction

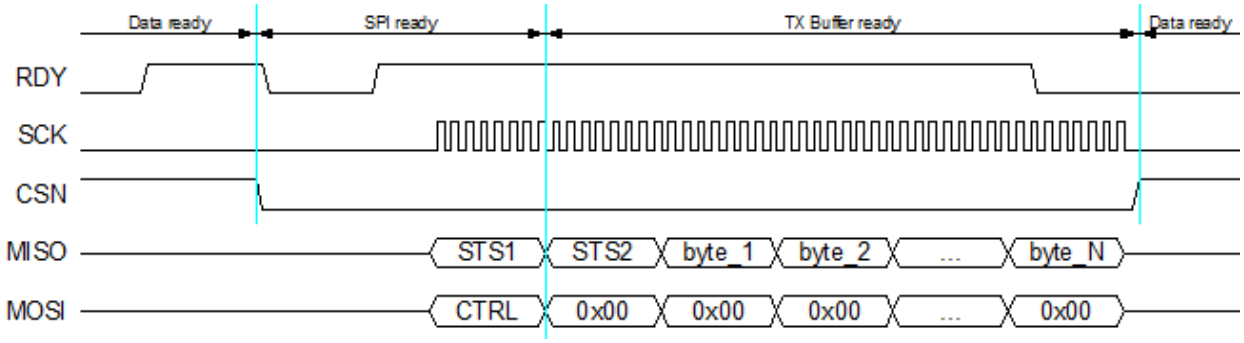


Figure 13: SPI Read Transaction

3.2.4.4 SPI Operation

Each SPI transaction starts by activating CSN. After setting CSN to '0' RDY goes to '0' to indicate that SPI interface is not ready for transfer. Once RDY is at '1' it indicates that SPI interface is ready for transaction and header bytes can be sent.

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The control byte (CTRL) sent on MOSI defines type of transaction (read or write). The second byte on MOSI is dummy to align with read status data from the Slave and reads 0x00.

The status byte STS1 on MISO indicates general status of device. The status byte STS2 on MISO indicates buffer capacity and it depends on read or write transaction. In case of write transaction STS2 contains the number of bytes which can be written into Slave RX buffer. In case of read transaction STS2 contains the number of bytes which can be read from Slave TX buffer.

After receiving header bytes (STS1 and STS2), the SPI Master knows how many bytes can be transferred via SPI in the current transaction (read or write) and the rest of SPI transaction is standard.

An SPI transaction can be terminated by the SPI Master at any time. The SPI Master can send only a header in order to get the status of the RX/TX buffer and then stop the SPI transaction.

The type of transaction (read or write) in half duplex mode is defined by CTRL, the 1st byte sent by the Master:

- CTRL = 0x81 for a read transaction.
- CTRL = 0x42 for a write transaction.

The STS1 byte contains the status of the SPI slave.

- STS1 = 0xC0 when slave is ready.

The STS2 byte contains the maximum number of bytes which can be written into RX FIFO without RX FIFO overflow during a write transaction, or the maximum number of bytes which can be read from TX FIFO without TX FIFO underflow during a read transaction.

3.2.4.5 SPI Slave RDY

RDY signal has following meaning depending on SPI transaction phase:

1. Data ready (when CSN = '1')
   - RDY at '1' indicates SPI Slave has some data to send.
   - RDY at '0' indicates SPI Slave has no data to send.

2. SPI ready (between CSN falling edge and end of 1st header byte)
   - RDY at '1' indicates that SPI Slave is ready and SPI transaction can start.
   - RDY at '0' indicates that SPI Slave is not ready and SPI transaction cannot start. SPI master has to wait until RDY is at '1'.

3. Buffer ready (between end of 1st header byte and CSN rising edge)
   - RDY at '1' indicates that buffer is ready and byte can be written/read
   - RDY at '0' indicates that buffer is not ready and byte cannot be written/read. SPI master has to wait until RDY is at '1'.

After asserting CSN and before sending first byte SPI Master checks if RDY is at '1'. This check shall be done at least T_RDY (100ns) after asserting CSN. If RDY is at '1' SPI transaction can start, if RDY is at '0' SPI master has to wait until RDY is at '1'.

3.2.5 GPIO

The GPIO are standard input/output structures with high-drive and pull-up or pull-down capability. Level shifters are provided between VIO and the internal supply voltage. An optional input debouncer is clocked by the LF RC oscillator divided by a selectable value between 16 and 2048. Any GPIO can interrupt the CPU on any input value and are maskable.

The GPIO functions are listed in Table 24. Available peripherals are UART, SPI slave, SPI master, I2C master, timer start/stop and capture, RF active, PA enable, PML mode, 32kHz input, and JTAG. The peripherals can be mapped to several different pins in order to optimize the PC board layout when connecting it to an external MCU, sensor, or other devices to avoid crossed wires when routing the board.

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Table 24: GPIO Functions

Blocks	Pads	Comment
GPIO	all	General IO function input, output, pull down, pull up
SPI Slave	CSN, SCK, MISO, MOSI, RDY	Programmable mapping
UART	RX, TX, CTS, RTS	Programmable mapping
SPI Master	CSN, SCK, MISO, MOSI	Programmable mapping
I2C Master	SCK, SDA	Programmable mapping
Timer start/stop	GPIO0 to GPIO11	HW start/stop of Universal timer
Timer capture	GPIO0 to GPIO11	HW capture of Universal timer
Timer clock input		External clock of Universal timer
Timer output		Output of Universal Timer
RF activity	GPIO0 to GPIO11	Output, SW controlled, RF activity monitor
PA enable	GPIO0 to GPIO11	For switching external PA on during TX
JTAG	TCK, TMS, TDI, TDO	ARC debugging port

The GPIO configuration options are detailed in Table 25. The peripherals can typically be mapped to several possible GPIO. If a GPIO can be configured as an input it is marked with an “IN” at the appropriate column and the function is shown in the corresponding row. Likewise, if a GPIO can be configured as an output it is marked with an “OUT”, and if it can be both an input and output it is marked as “INOUT”. Note: to achieve minimum current consumption, no enabled GPIO should be left as a floating input.

The default configuration highlighted in orange uses the GPIO functionsfor GPIO 0-7 and JTAG for GPIO 8-11. JTAG is only available on the QFN, which is recommended for development. The default software configuration selects SPI slave on GPIO0-4 which can be overridden in OTP. Note, the default hardware GPIO configuration is applied briefly during startup and after chip reset until the new configuration is read from OTP and applied to the GPIO. This may have unintended consequences to your application such as additional current consumption or incorrect logic function.

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Table 25: GPIO Configuration

Peripheral	Function	GPIO0	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8	GPIO9	GPIO10	GPIO11
SPI Slave	CSN_S	IN	0	0	0	IN	0	0	0	0	IN	0	IN
SPI Slave	SCK_S	0	IN	0	0	0	0	0	IN	0	0	0	0
SPI Slave	MISO_S	0	0	OUT	OUT	0	0	0	0	0	OUT	OUT	0
SPI Slave	MOSI_S	0	0	IN	IN	0	0	0	0	0	IN	IN	0
SPI Slave	RDY	0	OUT	0	0	OUT	0	OUT	OUT	0	0	0	0
UART	Rx	IN	IN	IN	IN	IN	0	IN	0	0	0	0	0
UART	Tx	OUT	OUT	OUT	OUT	0	0	0	OUT	OUT	0	0	0
UART	nCTS	0	IN	IN	IN	IN	0	0	0	IN	IN	IN	0
UART	nRTS	OUT	OUT	OUT	OUT	0	0	0	OUT	0	0	OUT	0
SPI Master	SCK_M	0	OUT	0	0	OUT	0	0	OUT	0	OUT	OUT	0
SPI Master	MISO_M	0	0	IN	IN	0	0	0	0	0	IN	IN	0
SPI Master	MOSI_M	0	0	OUT	OUT	0	0	0	0	OUT	0	OUT	OUT
I2C Master	SCL	INOUT	0	0	0	INOUT	0	INOUT	0	0	INOUT	0	0
I2C Master	SDA	0	INOUT	0	0	0	INOUT	INOUT	INOUT	INOUT	0	0	0
SW	RF_Activity	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
RF	PA_Enable	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
GPIO	GPIO	INOUT	INOUT	INOUT	INOUT	INOUT	INOUT_PD	INOUT	INOUT	INOUT	INOUT	INOUT	INOUT
Timer2	Start/Stop	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer3	Start/Stop	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer2	Capture	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer3	Capture	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer2	Clock	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer3	Clock	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN
Timer2	Output	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
Timer3	Output	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
PML	Mode	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT
JTAG	TMS	0	0	0	0	0	0	0	0	0	0	0	IN
JTAG	TDI	0	0	0	0	0	0	0	0	0	0	IN	0
JTAG	TDO	0	0	0	0	0	0	0	0	0	OUT	0	0
JTAG	TCK	0	0	0	0	0	0	0	0	IN	0	0	0

3.2.6 Timers

The EM9304 has 3 types of timers in the system. The first timer is a 32-bit timer driven by the 32kHz crystal oscillator or low-frequency RC oscillator (divided by 12) and is dedicated to the sleep function which controls when the CPU is woken up. The second timer is a 32-bit timer driven by the 48MHz crystal oscillator or 24/48MHz RC oscillator and used by the link layer for higher-speed protocol related timing. The third timer is a universal timer, which can be used by the application.

There are two universal timers with the following features:

- 32-bit up counter, selectable auto-reload
- clock source: system clock, GPIO
- 7-bit pre-scaler
- SW start/stop
- HW start/stop
- input capture on HW events (GPIO)
- input capture on SW event
- limit value
- compare value
- output to GPIO; maximal frequency 12MHz, minimal duty cycle 45/65
- interrupt on limit value, compare and input capture

3.3 Power Management

This section describes the EM9304 power management. The DCDC converter is a single-output, step-up/down converter with a simple bang-bang regulation. The output voltage is monitored with a supply voltage level detector (SVLD) circuit and the regulation is adjusted accordingly. In sleep mode, the DCDC converter is off but the output capacitor can optionally be kept charged.
The power management can be configured in several different modes:

- In DCDC Step-Down Configuration, the battery is connected to VBAT1 and VBAT2. The DCDC switching output is connected to VCC.
- In DCDC Step-Up Configuration, the battery is connected to VCC, and VBAT2. The DCDC switching output is connected to VBAT1.
- In DCDC Off Configuration, the battery is connected VBAT1, and VBAT2. The DCDC switching output is connected to ground, and VCC is connected to a 2.2µF decoupling capacitor. There

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is a dedicated linear regulator (LDO VCC) between VBAT1 and VCC which creates 1.25V on VCC.

- In External-DCDC Configuration, the battery is connected to pads VBAT2, and VCC. The DCDC switching output is connected to ground, and VBAT1 is connected to an externally supplied voltage with a minimal level of 2.6V.

3.3.1 Supply Domains

The supply domains in the device are described in Table 26.

Table 26: Supply Domains

Supply	Configuration	Range [V]	Description
VBAT2	All	1.05 - 3.6V	Input from battery
VBAT1	Step-Down DCDC Off	1.9 - 3.6V	Input from battery
	Step-Up	1.9 - 3.4, +/- 100mV	Generated from DCDC switch, external inductor and external capacitor
	External DCDC	1.9 - 3.6	Input from external DCDC converter
VCC	Step-Down	1.05 – 1.7, +/- 50mV	Generated from DCDC switch, external inductor, and external capacitor
	Step-Up External DCDC	1.05 – 1.9V	Input from battery or external DCDC converter
	DCDC Off	1.25, +/- 25mV	Output of LDO VCC, external decoupling capacitor

3.3.2 Logic Power Domains

The logic power domains are described in Table 27 and shown in Figure 14.

Table 27: Logic Power Domains

Domain	Voltage	Blocks	Control	Description
VDD_P	VDD_P or VDD	PML, DRAM0	Always on	System controller, reset controller, clock controller, pad controller, DC/DC control, data RAM
VDD0	VDD	DRAM2	By PML	Can be used for retention
VDD1	VDD	DPR, IROM, DRAM3	By PML	The minimal set for CPU running
VDD2	VDD	RF	By CPU	The complete set for RF operation VDD1 must be on at the same time
VDD3	VDD	IRAM0	By CPU	Can be used for retention
VDD4	VDD	IRAM1	By CPU	VDD1 must be on at the same time
VDD5	VDD	DRAM1	By CPU	Can be used for retention
VDD6	VDD_OTP	OTP	By CPU	OTP core voltage VDD1 must be on at the same time

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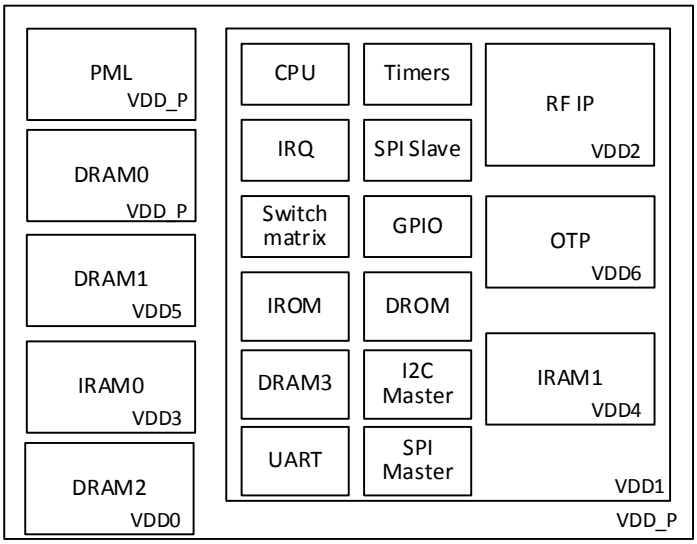


Figure 14: Logic Power Domains

3.3.3 Supply Monitoring

The power management configuration is automatically detected by the power management logic and setup appropriately. This is accomplished with use of an internal supply voltage level detector (SVLD) that can be applied to the following supply domains: VBAT1, VCC, AVDD_RF (internal RF supply), and SW_DCDC. The SVLD supply domains are described in **Table 28** VBAT1 is used to monitor the battery voltage in DCDC Step-Down Configuration or the DCDC control loop in DCDC Step-Up Configuration. VCC is used to monitor the battery voltage in DCDC Step-Up Configuration or the DCDC control loop in DCDC Step-Down Configuration. AVDD_RF is used to monitor the voltage on the RF IP. In case of low-voltage an event is issued.

Table 28: SVLD Supply Domains

Supply	Range	Step	Comment/Configuration
VBAT1	1.9 – 3.4V	100mV 4 bits	Used for battery voltage monitoring Step-Down, DCDC Off: battery monitoring Step-Up: DCDC control loop External DCDC: DCDC voltage monitor
VCC	0.95 – 1.7V	50mV 4 bits	“0010” → 1.05V Step-Up, External-DCDC: battery monitoring Step-Down: DCDC control loop DCDC Off: LDO voltage monitor
AVDD_RF	0.94, 0.99V	1 bit	Used for RF supply monitoring CPU will use the information to inform Host about battery level

3.3.4 Chip Disable

There is a specific device mode called chip disable mode, which is activated if the pad ENABLE is low or '0'. In this mode all GPIO are floating (Hi-Z), and the supply current is reduced to absolute minimum (5nA). Note, when the chip is disabled, digital outputs are put to a Hi-Z condition and the logic states are not maintained. This may lead to a misleading state on the RDY pin. The firmware is also reset.

3.3.5 Reset Structure

The power management reset structures are shown in Table 29. When the battery is inserted, a power-on-reset is generated at 470mV and the entire logic is reset. Additionally, the DPR can be reset in 4 different ways:

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1) VDD power-on-reset
2) VDD power check
3) CPU watchdog
4) Software reset is issued

Table 29: Reset Structures

Name	Condition	What is reset	Description
VDD POR	VDD> (470;670) mV	The whole logic	VTH based reference
VDD PWR-CHK	VDD < 0.83V	DPR and RF logic	Static comparator
WATCHDOG	CPU watchdog	DPR and RF logic	ARC request processed in PML
SW	SWReset register	DPR and RF logic	Writing 0xCAFEABAB,0xCDCDBEEF to the register RegPmlRes.SWReset

3.4 Operating Modes

3.4.1 Mode Descriptions

The EM9304 operating modes are described in Table 30. Operating modes are designed to optimize the power consumption during operation.

Table 30: Operating Modes

Mode	VDD supply	Clock	Description
Active RC (active mode)	Full, high load DC/DC on	RC 48MHz	CPU enabled, logic power domains controlled by CPU
Active XTAL (active mode)	Full, high load DC/DC on	XTAL 48MHz	CPU enabled, logic power domains controlled by CPU, RF controlled by CPU
Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered-down; VCC optionally charged (on by default) DCCM0 and optionally DCCM1, DCCM2, and ICCM0 in retention mode LF RC oscillator with normal precision, PML clock reduced to 250kHz
Deep Sleep (sleep mode)	DC/DC off	RC 250kHz	CPU powered down, VCC not charged DCCM0 and optionally DCCM1, DCCM2, and ICCM0 in retention mode LF RC oscillator in low precision operation, PML clock reduced to 250kHz
Chip Disable	None	None	Chip disabled

When the CPU is active, two modes are possible. Active RC mode is used with a high-frequency (HF) RC oscillator for fast turn-on and turn-off performance. This can be used to service the peripherals, for example. When the RF is required, active XTAL mode is used with a high-accuracy crystal oscillator for channel frequency precision required by the RF standards. The crystal oscillator takes longer to turn on than the RC oscillator and more energy is consumed when in use.

In the sleep and deep sleep modes, the sleep timer clock (device timing reference) can be connected either to the digitally calibrated RF low-frequency (LF) RC oscillator or to the low-frequency crystal (LF XTAL) oscillator. If the LF crystal oscillator is used, the LF RC oscillator is switched to a relaxed mode with less supply current and less accuracy. LF RC runs all the time since it is used for the power management logic. The LF crystal option brings higher clock accuracy (about 10 times), which requires a shorter RF window in time for TDMA functions, hence lower average current. However, it requires an external crystal component.

Chip disable mode is provided as the lowest power mode possible with the battery voltage still applied to the IC but all functions are disabled.

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3.4.2 Mode Transitions

The mode transition diagram is shown in Figure 15. When the chip is powered from the OFF mode, enabled from chip disabled mode, or woken from sleep or deep sleep modes, it enters the active RC mode. Active XTAL mode is then entered if the radio is to be used to send or receive data or the HF crystal is required for other reasons. (It is also entered when coming out of sleep mode.) When no CPU tasks are pending the CPU is halted. If there is enough time before the next pending CPU task sleep mode is entered. Note, when the chip is enabled, it will enter sleep mode until a command is received, and so this could be considered the default mode. Alternatively, deep sleep mode can be entered by issuing the appropriate command. Sleep mode can be disabled by software (during software development, for example) in which case the chip will remain in the active state with the CPU halted. The chip can be woken up by the sleep timer (scheduled by the link-layer) or from pad activity such as an HCI command and enters active RC mode as previously described. Chip disable mode is entered at any time by setting the ENABLE pin to logic 0.

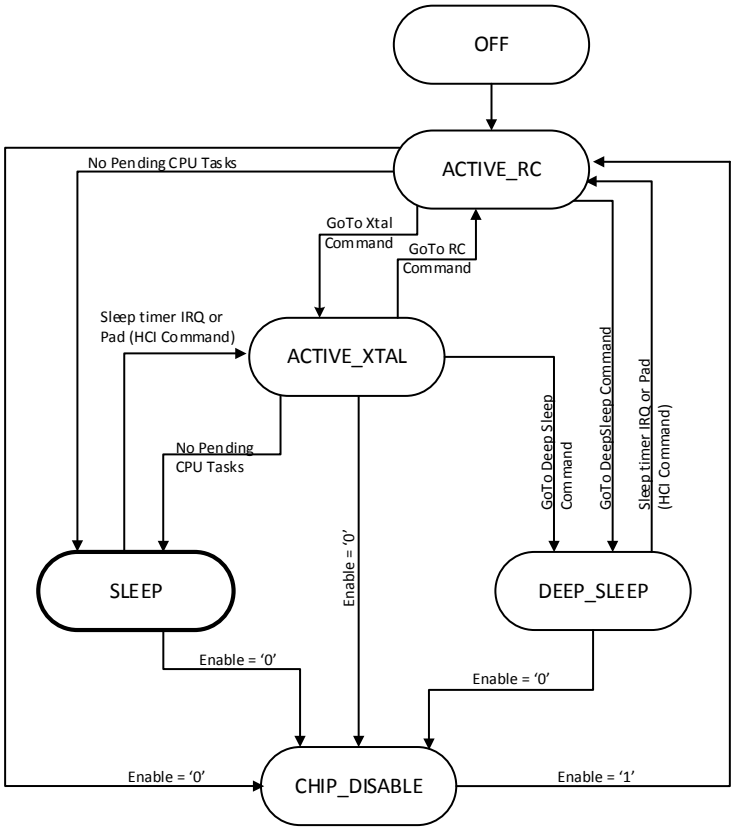


Figure 15: Mode Transitions

3.5 Clock Structure

The device has the following clock sources as shown in Table 31. By default the EM9304 is configured to use the internal RC oscillator (lf_rc_clk) as the sleep clock source with frequency calibration enabled. If a different sleep clock source is desired (32kHz crystal or external source) a configuration patch is necessary to load into OTP.

Table 31: System Clocks

Name	Oscillator, frequency	Accuracy	Description
lf_rc_clk	RC, 500kHz	-/+ 10% after trimming 500 ppm after calibration	PML system clock when sleep timer needed (on during power up) 2-bit trim from 420-615kHz
lf_rc_lp_clk	RC, 500kHz	+/-40%	PML system clock when sleep timer not needed or running on LF XTAL
hf_rc_clk	RC, 48MHz	-/+ 2% at 25C	Used as system clock
clk_xtal	XTAL, 48MHz	20 ppm	Output of RF IP, used as system clock
lf_xtal_clk	LF XTAL, 32kHz (32.768kHz)	50 ppm after calibration	Used for Sleep timer External oscillator signal can also be applied.
clk_spi	SPI slave clock, 16MHz	N/A	SPI (HCI) slave clock

3.5.1 LF XTAL Modes

The low-frequency crystal (LF XTAL) block can operate in 3 different modes or disabled, as described in Table 32. In the first mode, a crystal is connected between LF_XIN and LF_XOUT pads. In the second mode, a full swing logic signal is applied to LF_XIN and the internal amplifier is turned off. In the third mode, an analog sine wave is applied to LF_XIN and the internal low-noise amplifier is used to amplify the signal to the internal logic level. If LF_XIN or LF_XOUT are not used, they shall be left floating.

Table 32: LF XTAL Modes

RegPmlMode.LFXtal	lf_xtal_clk	Description
0	'0'	LF XTAL disabled. LF_XIN and LF_XOUT to be left open.
1	clock	LF XTAL enabled, XTAL connected to LF_XIN and LF_XOUT
2	clock	LF XTAL disabled, 12pF load capacitor disconnected, external full swing square wave clock signal connected to LF_XIN
3	clock	LF XTAL amplifier enabled, 12pF load capacitor disconnected, external sine wave clock signal connected to LF_XIN

3.5.2 LF Clock Calibration

Bluetooth requires a minimum of +/-500ppm timing precision for a connected state. The actual communication timing precision is calculated based on the precision of both master and slave devices. Better timing precision allows for longer sleep time in between communication slots, resulting in lower average power consumption, especially for longer connection intervals.

Before using the low-frequency (LF) RC clock for protocol timing, it must be calibrated against the high-frequency crystal (HF XTAL). Typically the HF XTAL has better than +/-50 ppm versus offset, temperature and aging, but this should be confirmed with the specification of the actual crystal used. Frequency trimming of the HF XTAL may be required for each application since the PCB layout parasitics vary between designs. The EM9304 comes trimmed with the frequency centered based on the reference design. The accuracy achieved depends on the length and of

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the calibration, the frequency of the calibration and the expected maximum temperature gradient of the application. The length and frequency of calibration can be adjusted in the configuration of the EM9304.

Additionally, if a low-frequency crystal is used, the frequency accuracy can also be improved with calibration. A typical low cost crystal is centered at room temperature, but can drift to -200ppm at both -40 and 85C. These calibration parameters can also be adjusted in the configuration of the EM9304.

Contact EM Microelectronic for further guidance in setting the low-frequency clock calibration parameters for your application.

4 Ordering information

The EM9304 is available in one version.

Table 33: Versions

	Version	Description /Features	Applications / Comments
1	Standard version	Bluetooth Low Energy 5.0 IC Integrated PHY, Link Layer, Stack and Profiles 128kB One-Time-Programmable Memory	HCI, ACI, and SOC use cases supported Software development kit available for on-chip applications

4.1 Ordering information

Table 34: Ordering Information

Ordering Code	Description	Packaging	Container	Units per Container
EM9304V01LF28B	Bluetooth Low Energy SoC	QFN-28	Tape on reel	2,500
EM9304V01CS25B	Bluetooth Low Energy SoC	WLCSP25	Tape on reel	4,000
EM9304V01WW31	Bluetooth Low Energy SoC	Tested wafer	Wafer container	12,000 est.
EMDVK9304	Development Kit		Box	1

4.2 Pin List

The EM9304 Pin List is shown in Table 35.

Table 35: Pin List

QFN-28 Pin #	WLCSP25 Pin #	Name	Type	Description
0		DIE_PAD		Die attach pad, connect to VSS on PCB
1	A5	ANT	ANT	RF single ended antenna
2	B5	AVSS_PA	SUP	PA ground
3	C5	VBAT2	SUP	Battery voltage
4	B4	ENABLE	DIG	Chip enable
5	D5	LF_XIN	XTAL	32kHz XTAL
6	E5	LF_XOUT	XTAL	32kHz XTAL
7	E4	VCC	SUP	Analog supply
8	D4	VIO	SUP	GPIO voltage level
9	E3	VBAT1	SUP	Battery voltage for DCDC, mode detection
10	E2	SW_DCDC	DCDC	Coil; mode detection
11		VSS_DCDC	DCDC	Ground of DCDC switches
12	D3	VSS	SUP	Logic ground
13	D2	GPIO5	DIG	Logic input/output

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QFN-28 Pin #	WLCSP25 Pin #	Name	Type	Description
14		GPIO6	DIG	Logic input/output
15	E1	GPIO0	DIG	Logic input/output
16	D1	GPIO1	DIG	Logic input/output
17	C1	GPIO2	DIG	Logic input/output
18	B1	GPIO3	DIG	Logic input/output
19		GPIO7	DIG	Logic input/output
20	A1	GPIO4	DIG	Logic input/output
21		GPIO8	DIG	Logic input/output
22		GPIO9	DIG	Logic input/output
23		GPIO10	DIG	Logic input/output
24		GPIO11	DIG	Logic input/output
25	A2	XOUT	XTAL	48MHz XTAL
26	A3	XIN	XTAL	48MHz XTAL
27	B3/C3	AVSS_RF	SUP	RF ground
28			NC	Connect to RF ground

4.3 QFN Package Marking

The EM9304 QFN package markings are shown in Table 36. Line A indicates the product number. Code B1-3 indicates the product version, code B4 indicates year of assembly, and code B5-6 indicates package information. Additional marking in line C are used for lot traceability.

Table 36: QFN-28 Package Marking

	1	2	3	4	5	6
A	E	M	9	3	0	4
B	0	0	1			
C						

4.4 QFN Package Information

EM9304 is available in a QFN-28 4mm x 4mm package. The QFN-28 package mechanical drawing is shown in Figure 16.

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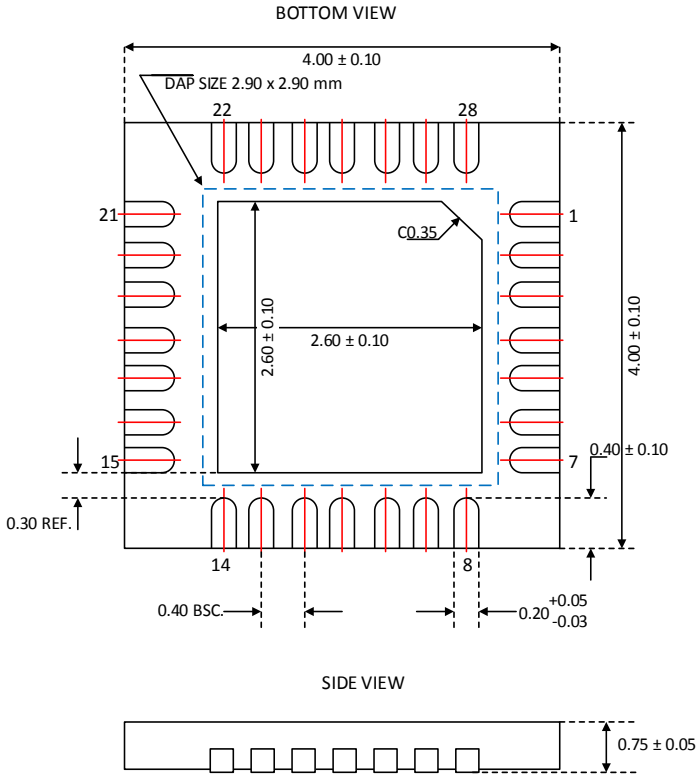


Figure 16: QFN-28 Mechanical Drawing

4.5 WLCSP Package Information

The EM9304 is available as a Wafer Level Chip Scale Package (WLCSP25). The package has in a 2.340mm x 2.206mm a 5x5 ball array with 0.4mm pitch. Several balls are not in the array to avoid interference with the RF performance. The mechanical drawing is summarized in Figure 17.

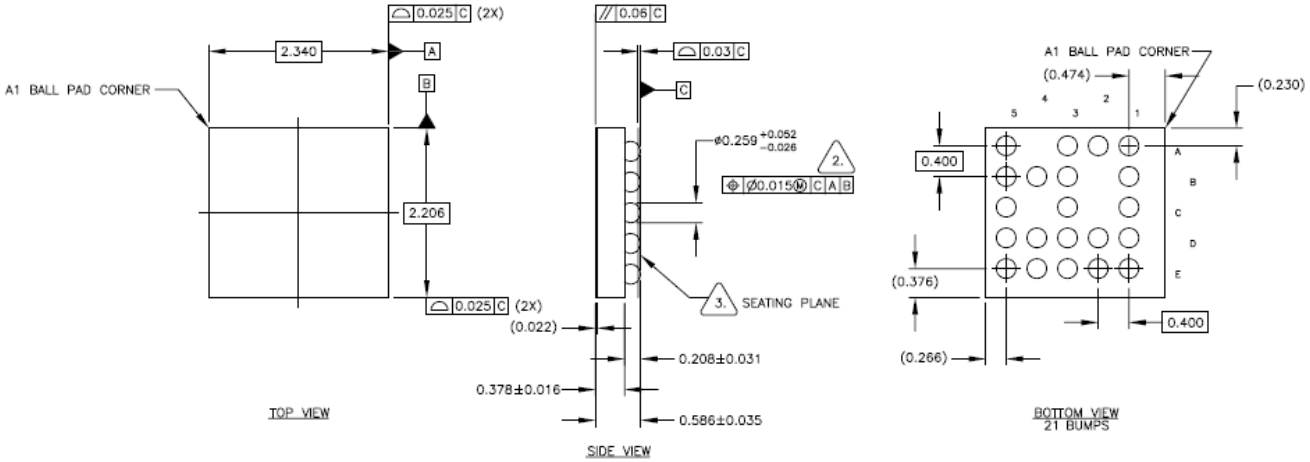


Figure 17: WLCSP25 Mechanical Drawing

4.6 WLCSP Package Marking

The EM9304 WLCSP package markings are shown in Table 37. Line A indicates the product number. Code B1-3 indicates the product version, code B4 indicates year of assembly, and code B5-6 indicates package information. Additional marking in line C are used for lot traceability.

Table 37: WLCSP25 Package Marking

	1	2	3	4	5	6
A	E	M	9	3	0	4
B	0	0	1			
C						

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4.7 WLCSP Package Reflow

Figure 18 shows the typical Temperature / Time Reflow profile for lead-free solder (SnAgCu) with recommended parameter values. The specification details are in Table 38. The optimum profile may depend on many factors such as the oven type, the solder type, the temperature difference across the board, the oven temperature / thermocouples tolerance etc. and must be fine-tuned to establish a robust process.

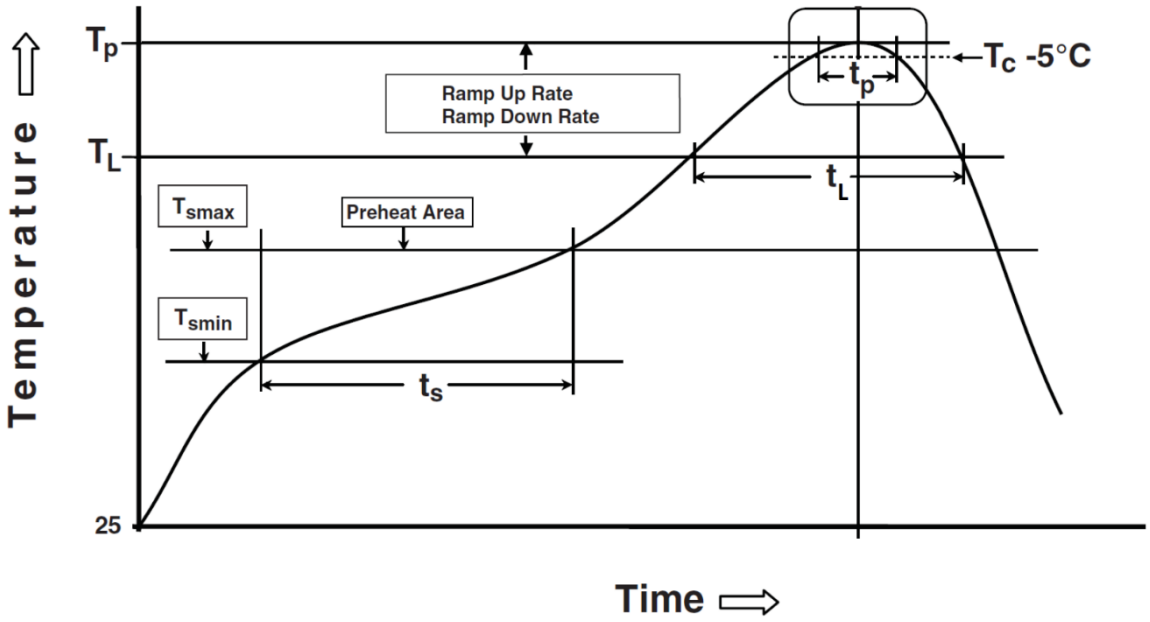


Figure 18: WLCSP Temperature/Time Reflow Profile

Table 38: WLCSP Temperature/Time Reflow Specification

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150 °C 180 °C 60-180 seconds
Ramp-up rate (T_L to T_p)	3 °C/second
Liquidous temperature (T_L) Time (t_L) maintained above T_L	220 °C 30-90 seconds
Peak package body temperature (T_p)	260 °C
Time (t_p) within 5 °C of the specified Peak package body temperature (T_p)	10-20 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.

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5 Embedded Software

5.1 Overview

The EM9304 embedded software or firmware provides an embedded application framework to support Bluetooth connectivity and communication when coupled with a link layer and Bluetooth stack. The core firmware presents a hardware abstraction layer (HAL) to support a fully integrated stack, and an application framework to add optional user applications. The HAL, application framework, and other associated functionality is referred to as the core firmware, which excludes the stack.

The core firmware supports four primary usage modes of operation as described in Table 39.

Table 39 Modes of Operation

Usage Modes	Description
Controller	EM9304 controller is used with an external host where the user application and the host layers of the stack reside in the external processor or host controller. Interaction with the EM9304 controller occurs through the HCI.
Companion	EM9304 controller is used with an external host where the user application resides in the external host, and the stack resides in the EM9304. Interaction with the EM9304 controller occurs through the ACI.
Application	The user application and entire stack reside in the EM9304 controller.
Production Test Mode (PTM)	The production test mode of operation provides functionality to support production test during manufacturing. PTM supports a limited number of HCI commands since the stack and Link Layer are not available when in PTM.

Diagram 1 of Figure 19 shows the usage mode where no user application is present and the Bluetooth connectivity is accessed through the HCI by an external host. In this instance, the stack and the user application reside in a host controller, so the upper layers of the stack in the EM9304 are not used.

Diagram 2 of Figure 19 shows the companion mode where the full stack is accessed through ACI by an external host.

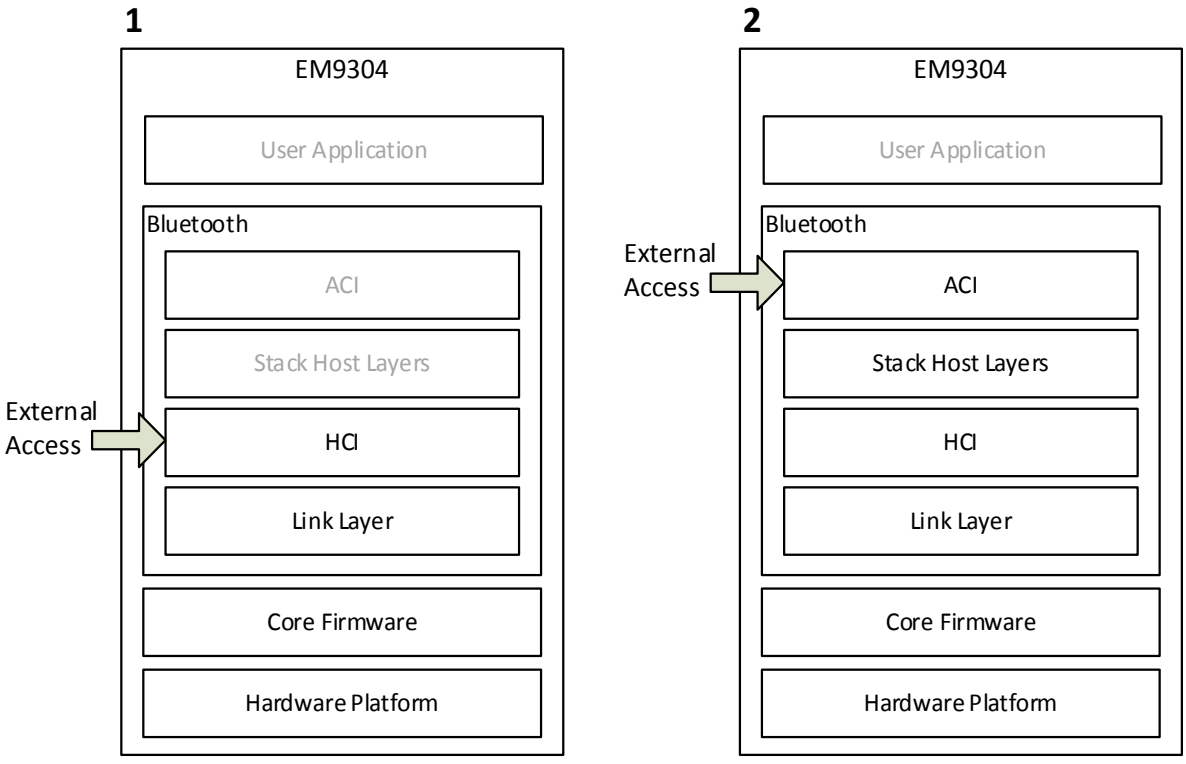


Figure 19 Controller and Companion Usage Modes

The SOC mode of operation is shown in Diagram 3 of Figure 20 shows the scenario where a user application is present in the EM9304 controller, which provides the full stack. In this configuration, a host is not needed since the complete user application is captured in the EM9304.

Diagram 4 of Figure 20 shows the Production Test Mode (PTM) usage where the EM9304 is configured to support production test during the manufacturing process. PTM is independent of Bluetooth DTM, which is a standard Bluetooth mode that allows testing of the radio's Physical Layer by transmitting and receiving sequences of test packets. PTM allows for test or support functions to be executed through HCI or for custom test applications to be executed from within the EM9304.

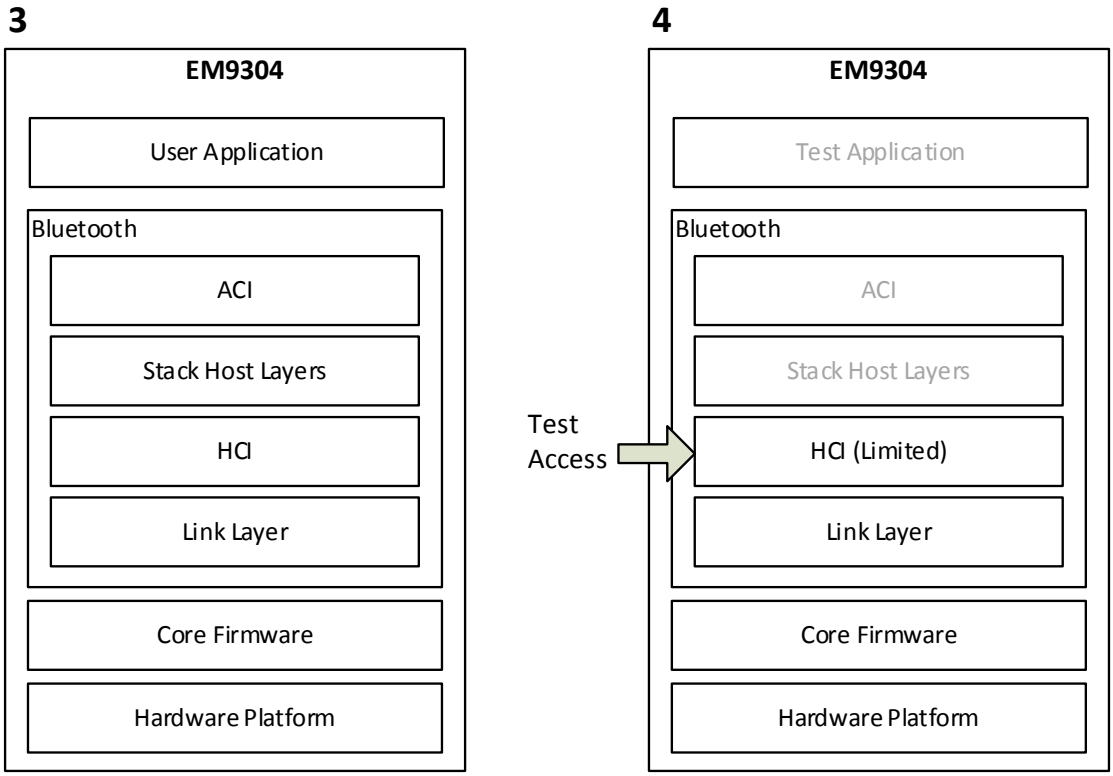


Figure 20 Application and Production Test Modes of Operation

5.2 Hardware Platform

The core firmware executes on the Synopsys DesignWare ARC EM4 processor operating at 24MHhz connected to a 32-bit AHB-Lite bus. The ARC EM supports two types of closely coupled memories: Instruction Closely Coupled Memory and Data Closely Coupled Memory (DCCM). The DCCM is accessed by the processor core through load/store memory references, whereas the ICCM is accessible for instruction fetch as well as load/store references.

Although the ARC architecture has physically separate instruction and data paths, the instruction and data memories, and the peripheral addresses are mapped to the same address space. The peripheral address space provides memory mapped access to peripherals on the AHB bus. The auxiliary address space is a separate address space, which is used by the security and encryption libraries.

5.2.1 Memory Organization

The memory address space is mapped to IROM, DROM, OTP, DRAM, IRAM, and the peripheral register address space.

Table 22 shows the memory map of the EM9304 controller.

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5.2.1.1 Instruction Address Space

The instruction address space is mapped into lower half of addressable space. The instruction Closely Coupled Memory (ICCM) consists of three memory types: IROM, IRAM0 and IRAM1. The OTP memory is an instruction memory on the AHB-Lite bus.

The OTP, IRAM, and DRAM memories can be used for data storage. Access to data in IRAM0/1 is accomplished using the load and store instructions as is done with the DCCM. However, the data access time of IRAM0/1 is longer than the access time of DRAM0/1. This is due to IRAM0/1 residing on the same physical bus as IROM, so instructions and data access are interleaved decreasing system performance.

The core firmware configures IRAM0 to be non-retention and is dedicated to the JLI table.

5.2.1.2 Data Address Space

The dedicated data memory address space is mapped to DRAM0, DRAM1, DRAM2, DRAM3, and the DROM. The DRAMs reside at the beginning of the upper half of the address space. DRAM0 is a retention memory and DRAM1 and DRAM2 are optionally retention memory. DRAM3 is a non-retention memory. The memory manager enables persistence for DRAM1 and DRAM2 as required to support the requested memory allocation. The DROM contains constants used by the EM Core, link layer, and Bluetooth stack software.

5.2.1.3 Peripheral Address Space

The peripheral address space is located at the end of the address space. The peripheral address space provides access to the memory mapped peripheral registers connected to the AHB-Lite bus.

The peripheral memory map is available upon request to EM Microelectronic.

5.2.2 Embedded Software Memory Usage

The IROM contains the core firmware, HAL, security and encryption libraries, Bluetooth 5.0 link layer, stack, the FOTA profile and the following four Bluetooth services:

- Immediate Alert Service
- Link Loss Service
- Transmit Power Service
- Alpwise Data Exchange Service

The DROM contains constant data used by the core firmware, HAL, link layer, and stack software.

The OTP can be used for firmware patches are needed for new functionality, updating exiting ROM functionality, adding new initialization or calibration data, profiles, and user data such as data logs. If no firmware code patches are present in the OTP, the OTP is turned off, so it consumes no power after the firmware power up process is complete.

DRAM contains the following retention data:

- Stack buffers and retention data when the stack is enabled
- Link layer buffers and retention data
- Driver retention data

The minimal Bluetooth link layer configuration with the Bluetooth stack disabled, requires only DRAM0 to be retention, so DRAM1 and DRAM2 do not consume power while in sleep mode.

5.3 Software Architecture

The core firmware and the hardware abstraction layer reside between the hardware and the stack and the user application as shown in Figure 21. The embedded software application framework consists of the TSOS that provides task prioritization and scheduling, interrupt handling functionality, timer functionality, and utility functions such as the firmware update or patch manager. The (HAL) consists of

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the boot functionality, power manager, and a number of hardware drivers that provide an API to the underlying hardware components.

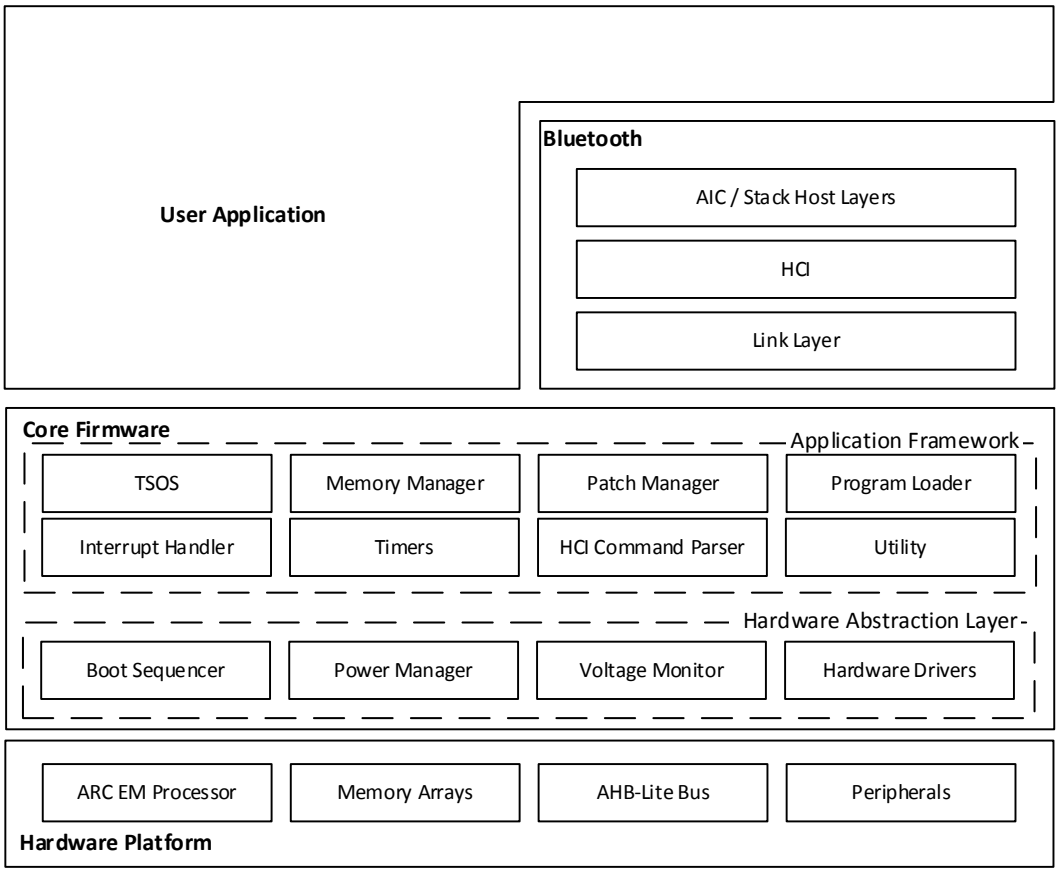


Figure 21 Simplified System Overview

The software architecture is composed of a number of functional blocks, which can be divided into two categories: application framework functionality or hardware abstraction layer functionality.

5.3.1 Application Framework

The application framework provides functional blocks to the support the stack and user applications. The application frameworks consists of the TSOS, interrupt handler, timer management, and utility functionality such as the firmware patch manager, test mode manager, and standard C runtime libraries.

5.3.1.1 TSOS

The TSOS is the task management software framework, QP-nano ported to the ARC processor with minor customizations and optimizations. TSOS is a run-to-completion, pre-emptive, cooperative operating system that is optimized for speed with a minimal ROM footprint. It contains a pre-emption kernel with up to 8 levels of priority. Each priority must run a single task that may consist of 1 or more finite state machines (FSM). These tasks must be defined before TSOS is started.

Pre-emption

TSOS uses two forms of pre-emption: synchronous and asynchronous. Pre-emption occurs when an event is posted from an ISR or within the currently running task.

Synchronous Pre-emption

Synchronous pre-emption occurs when a task issues an event that is handled by a higher priority task. In this case, the event will be added to the event queue and the task scheduler is immediately called to run the higher priority task. Once all higher priority tasks complete, execution resumes in the original task.

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Asynchronous Pre-emption

Asynchronous pre-emption occurs when the interrupt handler issues an event handled by a higher priority task. In this case, the event will be added to the event queue and the task scheduler will run after all interrupts are handled that are higher priority than the tasks. For this, a context switch is required to save the state of the previous task and another context switch is required to restore the previous task after all higher priority tasks are complete.

Context Switching

Context switching is achieved through the use of 8 software interrupts. These correspond to the 8 priority levels for the TSOS. When asynchronous pre-emption occurs (even in the case where the CPU is sleeping and no tasks are in the run queue), the software interrupt for the corresponding priority of the event that will be received by a task is triggered. Remember that asynchronous pre-emption occurs when a hardware ISR issues an event. Each software interrupt is given a unique priority that has no overlap with any other interrupt. All 8 software interrupts are lower priority than all other interrupts so that execution may be paused while a hardware event is processed.

Note that when a synchronous pre-emption occurs, the corresponding software interrupt for the new priority is not triggered. The TSOS will simply note the new priority and prevent any hardware ISR from triggering the higher priority (but even higher priorities may still be triggered asynchronously) until the priority drops again. In this case, the event will be processed (again in the lower priority software interrupt) after the task currently running at that priority is completed. This produces the minimal amount of software interrupts and context switches.

The other method of handling context switching is to trigger a single software interrupt (again at the lowest priority) that will execute the scheduler and run the new task upon exit. This is achieved by modifying the stack pointer and return address. Once the task is complete a second interrupt is triggered to switch back to the previous task. At this time, the context restoring interrupt will remove itself from the stack so that when the interrupt returns, the task returned to is the previous pre-empted task. Unfortunately, this requires time to be consumed saving the state of the CPU for the context restoring interrupt, only for it to be popped off the stack immediately upon entry.

Since the TSOS only contains a maximum of 8 priority levels and the two interrupt (ARM) approach requires more time to context switch, 8 software interrupts were used instead. This produces less context switching code and allows for a simpler and assembly free solution. An added benefit of the assembly free solution is that any architecture changes (like another register that must be saved) on the ARC will not require a change of the context switching code.

5.3.1.2 Interrupt Handler

The interrupt handler provides a default interrupt handler for all interrupt vectors. The default interrupt handler for a specific interrupt vector is overwritten to provide specific functionality to handle to the specific interrupt.

5.3.1.3 Memory Manager

The memory manager provides functionality to dynamically allocate memory from a memory pool composed of the optionally retention DRAM memories. The persistence option is only enabled once a retention memory allocation is made in that memory. Once the persistence option is enabled for a DRAM it is not disabled during operation. Functionality is provided to allocate either retention or non-retention memory with or without 32-bit alignment enforced. To eliminate the complexity and non-determinism of garbage collection, de-allocating or freeing memory is not supported. Retention is maintained in sleep mode, but not in deep sleep mode.

5.3.1.4 Firmware Patch Manager

The firmware patch manager primarily enables the ROM firmware functions to be updated or replaced by writing the updated functionality to the OTP memory and updating the JLI (Jump and Link Indexed) table. The JLI table is part of the code-density option in the ARCv2 core that is similar to a lookup table mapping a function identifier (index) to an indirect call. All normal function calls are replaced with a JLI instruction where the address of the destination function

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is defined in the JLI table. The JLI table can accommodate 1024 entries where each entry is 4 bytes in size. Figure 22 depicts an example prior to the application of the firmware patch.

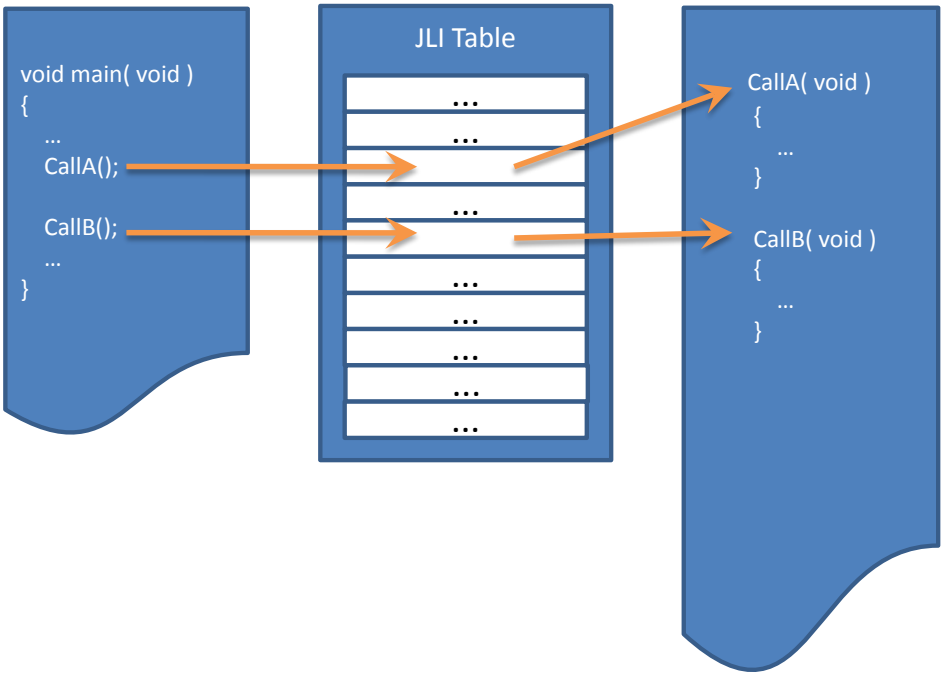


Figure 22 JLI Table Example Prior to Firmware Patch

Figure 23 depicts an example after the firmware patch is applied.

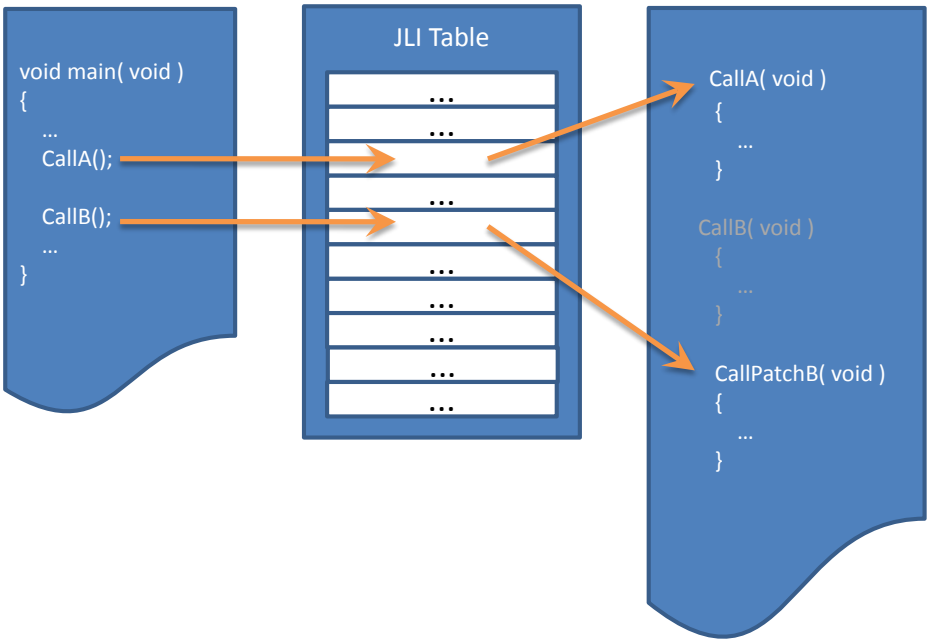


Figure 23 JLI Table Example After Firmware Patch

The firmware patch manager handles the transfer of containers to OTP and applies the firmware patches found in the OTP or IRAM memory. A container is a block of data formatted in the EM container format that may contain firmware patch information, configuration data, and other data. The following sequence is performed by the patch manager during the boot process.

1. Beginning at the start of the OTP memory, read the contents of the OTP sequentially searching for the container signature
2. If the patch file container contains a valid checksum, update the JLI table from the contents of the patch file.
3. If the patch file container does not contain a valid checksum, go to step 1.

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4. Continue to iterate through the OTP until no valid patch containers are found
5. Repeat the patch process for the IRAM.

As newer patch files are identified in the OTP or IRAM, JLI table entries will be overwritten. Since OTP memory is in separate power domain, the OTP memory power domain must be enabled before accessing the OTP memory. As specified in the boot sequence, the presence of content in the OTP must be noted to ensure the power domain remains enabled and is re-enabled when resuming from sleep.

Since the JLI table contents in IRAM will be lost in sleep mode, the JLI table must be reconstructed when resuming from sleep. However, it is critical to minimize the time it takes to resume from sleep. To minimize the time spent reading the OTP, the following steps are required:

1. During the construction of the JLI table during the boot process, the patch manager will construct a list of valid containers for reference when resuming from sleep. This eliminates reading the OTP to locate containers.
2. Processing the OTP will be terminated when the end of the OTP is reached or after 1024 erased bytes are read. This eliminates unnecessarily reading large sections of erased OTP.

The EM container format is an extensible format specification created to accommodate all data stored in the OTP memory while optimizing the identification and processing of that data. Table 40 defines the format of the container header. The header is 32-bit aligned and the packet size must be a multiple of 32 bits. The table column labelled “Offset” shows the offset in bytes of each entry.

Table 40 Container Header Format

Offset	Name	Size (Bits)	Description
0	Signature	32	Container signature used for search for a container. Signature = 0x656D3933 or ASCI “em93”
4	Size	32	Size of the entire container in bytes and used to index to next container.
8	Format version	8	Container format version used to identify supported format features. The initial value is 0x00 and is incremented for each subsequence version revision.
9	Container type	8	Identifies the contents of container. 0x00 = undefined 0x01 = configuration data 0x02 = random data 0x03 = random byte 0x04 = block data 0x05 = patch file 0x06 = unstructured data (user defined) 0x07 = unstructured data byte 0x08 = block byte 0x09 = transfer patch OTP version execute from OTP 0x0A = transfer patch IRAM version executed from IRAM 0x0B = configuration data byte
10	Container identifier	8	Container identifier that is unique for a given container type.
11	Container header length	8	Length of the container header in bytes.
12	Build number	16	Firmware build number – used to determine precedence of patched functions.
14	User build number	16	User defined number used to determine precedence of patched functions.

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16	CRC32	32	CRC32 of the entire container. If the checksum is invalid, the entire container is disregarded.

The container type defines the type of data encapsulated in the container. Table 41 summarizes the container types

Table 41 Container Types

Type	Name	Description
0x00	Undefined	This container type is reserved.
0x01	Configuration Data	Contains software configuration options in 32-bit format.
0x02	Random Data	Contains random data consisting of address and 32-bit value pairs where the 32-bit value is written to the given address.
0x03	Random Byte	Contains random data consisting of address and 8-bit value pairs where the 8-bit value is written to the given address using a read/modify/write sequence.
0x04	Block Data	Contains a single address followed by a block of 32-bit values where the block of data is written to the given address.
0x05	Patch File	Contains a code patch.
0x06	Unstructured Data	Contains 1 or more 32-bit values. This data is user defined and is available for access through the patch manager API following the boot process.
0x07	Unstructured Data Byte	Contains 1 or more 8-bit values. This data is user defined and is available for access through the patch manager API following the boot process.
0x08	Block byte	Contains a single address followed by a block of 8-bit values where the block of data is written to the given address.
0x09	Transfer Patch OTP version	OTP version of the transfer patch that executes only if transfer patches are not allowed.
0x0A	Transfer Patch IRAM version	IRAM version of the transfer patch that executes if transfer patches are allowed.
0x0B	Configuration Data Byte	Contains software configuration options in 8-bit format.

Note that since the header length is given in the container header, additional entries can be added to the header following the checksum entry which simplifies the addition of user defined entries. Additional entries must be a multiple of 4 bytes.

The container identifier field is used to uniquely identify containers of a given type. For instance, if more than one configuration data containers are desired, a unique identifier can be used to distinguish between two independent containers versus one container that is intended to replace another container.

The user build number is zero for EM firmware containers. A nonzero user build number identifies the container as a user container.

If the CRC in the header is invalid, the entire packet is disregarded, and the search for a new container begins at the next memory address after the last container signature found.

The transfer patch type applies to code containers only and provides a means to programmatically execute the code from IRAM. During the boot process and when resuming from sleep mode, the transfer patch container is copied from OTP to IRAM and the software code within is executed from IRAM. This provides the benefit of operating with the OTP

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powered off in active mode and both the IRAM and OTP powered off during sleep mode. Thus, transfer patches reduce the overall current consumption. Transfer patches only apply to HCI and ACI modes where application code is not executing from the OTP.

5.3.2 Hardware Abstraction Layer

The HAL provides hardware abstraction of the 9304 hardware platform in the form of a boot sequencer, power manager, and hardware drivers.

5.3.2.1 Boot Sequencer

The boot sequencer is the functional block that executes after the following conditions:

- Transition from powered off to powered on (boot state) – the value of all memory is undefined.
- Reset (reset state) – the value of all memory is retained from prior to the reset
- Exit from sleep mode (resume state) – retention memory is retained from prior to sleep, but all non-retention memory is unknown.

5.3.2.2 Power and Sleep Management

The power manager primarily determines if a sleep mode can be entered. The firmware identifies three sleep modes, CPU sleep, sleep, and deep sleep. In CPU sleep mode, the CPU is placed in sleep mode with the other system components power on. In sleep mode, the CPU is placed in sleep mode, and many of the system components are powered off. Deep sleep mode is executed by the core firmware unless specifically commanded through a vendor specific HCI command.

The following sequence of events are executed prior to entering sleep mode.

1. TSOS enters the idle state.
2. TSOS calls the power manager's sleep function.
3. The sleep function determines if all conditions have been met to enter sleep mode as defined below.
4. The store functions of all driver modules are called to store the configuration data.
5. Retrieve and store the next protocol timer transaction from the linker layer to determine if the radio should be powered on when resuming from sleep.
6. The sleep function executes the sleep sequence as defined in the "Power Modes" section of this datasheet.

All of the following requirements must be met prior to entering sleep mode:

- TSOS has entered the idle state
- No UART transactions are active or pending
- No SPI transaction are active or pending
- Maximum sleep time reported by the link layer (link layer API) is greater than the minimum allowed sleep time plus overhead. The minimum allowed sleep time is defined as 15ms plus overhead and derived by the sum of the following time periods.
  - Time to store the configuration
  - Time to restore the configuration
  - Time to start HF XTAL
  - Additional margin

When in sleep mode, the JTAG function of the device is powered off, which will result in the Metaware debugger disconnecting from the device. The embedded software provides a configuration bit is provided that forces the embedded software to substitute CPU sleep for sleep. Since CPU sleep does not power off the JTAG function, the debugger will remain connected for software debugging.

5.3.2.3 Voltage Monitor

The voltage monitor is responsible for providing power level status to the core firmware and link layer to limit the use of or disable the power-level sensitive hardware components. The voltage monitor is executed after resuming from sleep mode and when commanded by the voltage monitor IRQ. It is also executed when starting the RF power domain, although only if the previous result is older than 0.5ms. An IRQ from voltage monitor is trigged whenever the

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voltage drops below a defined limit. The voltage monitor provides functions to identify the following conditions:

- Voltage level sufficient to support OTP operations
- Voltage level sufficient to support Bluetooth radio operations

If the supply voltage drops below a specific level the voltage monitor issues a system notification.

5.3.2.4 Device Drivers

The device drivers provide a layer of abstraction of the underlying hardware generally through memory-mapped registers. All interaction with a hardware component is accomplished through the device driver. Table 42 lists all required hardware drivers and the hardware component the driver manages.

Table 42 Device Driver List

Firmware Driver	Hardware Component	Description
AES	AES	Advanced Encryption Standard for Bluetooth encryption, decryption, and authentication
GPIO	GPIO Top	General Purpose IO control
I2C Master	I2C Master	I2C master interface controller (available with code patch)
Interrupt Handler	Interrupt Manager	Interrupt controller
Power Control	PML	Power Management Logic controls the power
Protocol Timer		Used for BLE protocol timing
OTP	OTP Controller	One Time Programmable memory controller
Sleep Timer	Sleep Timer	The only timer active in deep sleep mode
Radio	icyTRX	Bluetooth radio controller
RC Calibration	RC Calibration System	Calibration system for the RC calibration system
RNG	RNG	Random Number Generator used for Bluetooth authentication and encryption
SPI Master	SPI Master	SPI master interface controller (available with code patch)
SPI Slave	SPI Slave	SPI slave interface
UART	UART	UART interface controller
Universal Timer	Universal Timer	General purpose timer active in the active power mode

5.4 Production Test Mode (PTM)

PTM is a mode of operation that does not apply configuration options from the OTP or IRAM and does not execute any application code. It provides a reduced function set allowing patches in the OTP to be safely invalidated. This is particularly useful to regain access to the EM9304 when an errant user application has eliminated other means of interacting with the EM9304.

PTM is entered when GPIO5 is toggled at a 30 KHz rate during the boot process. When PTM is entered, all interrupts are disabled except those required for PTM operations. The TSOS is not active, but the hardware modules have been initialized through the drivers with default parameters.

PTM will support a subset of the vendor specific HCI commands listed in the “Vendor Specific HCI Commands” section of the document. The PTM operates independent of the link layer. Because the link layer will not be active prior to entering PTM, PTM contains functionality to process and execute Bluetooth 5.0 compliant HCI commands, and produce the Command Complete Event. The HCI transport defaults to SPI in PTM.

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Programming the EM9304 is supported by PTM, which allows the OTP or IRAM to be written through the HCI interface using the vendor specific HCI commands for programming, EM_WritePatchStart, EM_WritePatchContinue, and EM_WritePatchAbort. The programming state is entered when EM_WritePatchStart is called, and is terminated by resetting or power down.

5.5 Software Configuration Options

The Bluetooth link layer and stack (platform) are configurable through the software configuration options. The default values define the configuration that requires the minimum amount of retention memory yielding the lowest power consumption. Table 43 lists the platform options.

Table 43 Software Platform Configuration Options

Option	Default	Value Range
Maximum link layer connections supported	1	1 = minimum 8 = maximum
Maximum packet payload length	27	27 = minimum 251 = maximum
Bluetooth stack enabled	0	False = HCI enabled True = ACI enabled
Maximum bonds supported	0	0 = minimum 8 = maximum
Bluetooth company ID	0x005a	0x0000 = minimum 0xFFFF = maximum
Bluetooth address	Unique	0x000000000000 = minimum 0xFFFFFFFFFFFF = maximum

If the maximum number of bonds supported is set to zero, Bluetooth bonding is disabled. A unique 6 byte Bluetooth address is programmed into OTP for each EM9304.

5.6 Vendor Specific HCI Commands

All of vendor specific HCI commands are supported by the link layer, and a subset of the commands are supported in firmware PTM. The vendor specific HCI command OGF, OCF, and op codes are defined to be compatible with those defined for the EM9301 device.

The EM core firmware provides an API that abstracts the implementation details from the link layer unless the HCI command is fully handled by the link layer.

Table 44 summarizes the vendor specific HCI commands. The column labelled “PTM Support” indicates whether the command is supported in firmware PTM. Command names ending in “Ex” are an extension of an EM9301 device vendor specific HCI command.

Table 44 Vendor Specific HCI Commands

HCI Command	OGF	OCF	Opcode	PTM Support
EM_SetPublicAddress	0x3F	0x002	0xFC02	No
EM_SetUartBaudRate	0x3F	0x007	0xFC07	No
EM_TransmitterTest	0x3F	0x011	0xFC11	No
EM_TransmitterTestEnd	0x3F	0x012	0xFC12	No
EM_ReadAtAddress	0x3F	0x020	0xFC20	Yes
EM_ReadContinue	0x3F	0x021	0xFC21	Yes
EM_WriteAtAddress	0x3F	0x022	0xFC22	Yes

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HCI Command	OGF	OCF	Opcode	PTM Support
EM_WriteContinue	0x3F	0x023	0xFC23	Yes
EM_SetPowerModeEx	0x3F	0x024	0xFC24	Yes
EM_SetRfActivitySignalEx	0x3F	0x025	0xFC25	No
EM_SetRfPowerLevelEx	0x3F	0x026	0xFC26	Yes
EM_WritePatchStart	0x3F	0x027	0xFC27	Yes
EM_WritePatchContinue	0x3F	0x028	0xFC28	Yes
EM_WritePatchAbort	0x3F	0x029	0xFC29	Yes
EM_SetClockSource	0x3F	0x02A	0xFC2A	Yes
EM_SetMemoryMode	0x3F	0x02B	0xFC2B	Yes
EM_GetMemoryUsage	0x3F	0x02C	0xFC2C	Yes
EM_SetSleepOptions	0x3F	0x02D	0xFC2D	Yes
EM_SvldMeasurement	0x3F	0x02E	0xFC2E	Yes
EM_SetEventMask	0x3F	0x02F	0xFC2F	Yes
EM_CpuReset	0x3F	0x032	0xFC32	Yes
EM_CalculateCrc32Ex	0x3F	0x033	0xFC33	Yes
EM_PatchQuery	0x3F	0x034	0xFC34	Yes

5.6.1 EM_SetPublicAddress

Set the device public address.

Parameter	Size (Bytes)	Description	Opcode: 0xFC02
Address	6	Device public address.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the completion of this command.

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5.6.2 EM_SetUartBaudRate

Set the UART baud rate to the specified value. After issuing the Command Complete Event, the UART baud rate will be changed.

Parameter	Size (Bytes)	Description	Opcode: 0xFC07
Baud Rate	1	Baud rate selection. 0x00 = Reserved 0x01 = Reserved 0x02 = Reserved 0x03 = 9600 Baud 0x04 = 14400 Baud 0x05 = 19200 Baud 0x06 = 28800 Baud 0x07 = 38400 Baud 0x08 = 57600 Baud 0x09 = Reserved 0x0A = 115200 Baud 0x0B = 230400 Baud 0x0C = 460800 Baud 0x0D = 921600 Baud 0x0E – 0xFF reserved	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the success reception of this command.

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5.6.3 EM_TransmitterTest

Configure and execute the transmitter test. The transmitter test mode, channel number, packet length and payload type are configurable. The command is only accepted if there is no Bluetooth activity (no advertising, scanning or connection) currently in progress.

Parameter	Size (Bytes)	Description	Opcode: 0xFC11
Transmitter Test Mode	1	Test mode selection. 0x00 = EM transmitter test 0x01 = CM (continuously modulated) 0x02 = CW0 (continuous wave at bit '0') 0x03 = CW1 (continuous wave modulated) 0x04 = CWC (continuous wave at center frequency) 0x05 - 0xFF Reserved	
Channel Number	1	0x00 – 0x27 = Bluetooth RF channel number (0 – 39) 0x28 – 0xFF = Reserved	
Packet Length	1	0x00 – 0xFF = Length in bytes of the test packet	
Packet Payload Type	1	Packet payload type for EM and CM transmitter test modes. 0x00 = Pseudo-Random bit sequence 9 0x01 = Pattern of alternating bits '11110000' 0x02 = Pattern of alternating bits '10101010' 0x03 = Pseudo-Random bit sequence 9 0x04 = Pattern of All '1' bits 0x05 = Pattern of All '0' bits 0x06 = Pattern of alternating bits '00001111' 0x07 = Pattern of alternating bits '01010101' 0x08 – 0xFF = Reserved	
Return Parameters			
Status	1	Standard BT error code.	

EM transmitter test mode (0x00) is similar to the standard transmitter test mode with one added benefit. When test mode is terminated with the vendor specific HCI command, EM_TransmitterTestEnd, the number of packets transmitted is returned as an event parameter.

The Bluetooth frequency range is 2402 to 2480 MHz where the frequency for a specific channel is

$f_n = 2402 + 2n$ MHz where n is the channel number.

A command complete event is generated after the transmitter test is initiated. This command is not supported in PTM.

5.6.4 EM_TransmitterTestEnd

Terminate the transmitter test mode and return the number packets sent during the test for EM and CM transmitter test modes. The command is only accepted if there is no Bluetooth activity (no advertising, scanning or connection).

Parameter	Size (Bytes)	Description	Opcode: 0xFC12
None	0	This command contains no parameters.	
Return Parameters			
Status	1	Standard BT error code.	

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Packet Count	2	Number of packets transmitted during the test.

A command complete event is generated after the completion of this command.

5.6.5 EM_ReadAtAddress

Read one or more bytes at the given address. If the specified data length is greater 64 bytes, an invalid parameter error will be returned.

Parameter	Size (Bytes)	Description	Opcode: 0xFC20
Start Address	4	Address to start reading.	
Data Length	1	Number of bytes to read up to 64 bytes.	
Return Parameters			
Status	1	Standard BT error code.	
Data	Data Length	Data read from the specified address.	

A command complete event is generated after the completion of this command.

5.6.6 EM_ReadContinue

Read one or more bytes beginning from where the previous read command ended. This allows for continuous reads without supplying the address. If the specified data length is greater 64 bytes, an invalid parameter error will be returned.

Parameter	Size (Bytes)	Description	Opcode: 0xFC21
Data Length	1	Number of bytes to read up to 64 bytes.	
Return Parameters			
Status	1	Standard BT error code.	
Data	Data Length	Data read from the specified address.	

A command complete event is generated after the completion of this command.

5.6.7 EM_WriteAtAddress

Write one or more bytes at the given address. The number of bytes to write is inferred from the HCI packet size and cannot be over 64 bytes.

Parameter	Size (Bytes)	Description	Opcode: 0xFC22
Start Address	4	Address to start reading.	
Data	Data Length	Data to write to the specified address (up to 64 bytes).	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the completion of this command.

5.6.8 EM_WriteContinue

Write one or more bytes beginning from where the previous write command ended. The number of bytes to write is inferred from the HCI packet size and cannot be over 64 bytes.

Parameter	Size (Bytes)	Description	Opcode: 0xFC23
Data	Data Length	Data to write (up to 64 bytes).	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the completion of this command.

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5.6.9 EM_SetPowerModeEx

Enter the specified power mode. If active mode is already active, this command has no effect on the power mode.

Parameter	Size (Bytes)	Description	Opcode: 0xFC24
Power mode	1	0x00 = Active 0x01 = CPU sleep 0x02 = Sleep 0x03 = Deep sleep	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated prior to issuing the sleep operation, and after entering the active power mode.

5.6.10 EM_SetRfActivitySignalEx

Enable or disable the RF activity signal on the specified GPIO pin. The activity signal is active when the radio is transmitting or receiving a packet. The activity signal can be programmed to be active low or active high.

Parameter	Size (Bytes)	Description	Opcode: 0xFC25
RF Signal Enable	1	0x00 = RF activity signal disabled 0x01 = RF activity signal enabled active high 0x02 = RF activity signal enabled active low 0x03 – 0xFF reserved	
RF Signal GPIO Output	1	GPIO pin number to output the RF activity signal, e.g. 0 = GPIO0, 1 = GPIO1, etc. Allowed range is 0 to the maximum number of GPIOs.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the baud rate has been updated.

5.6.11 EM_SetRfPowerLevelEx

Set the radio transmit power level. The RF output power level cannot be changed when the radio is active. If the command is received while the radio is active, the power level will be changed once the radio activity is complete.
The maximum allowed power level may be limited due to the voltage supply level. The maximum allowed transmit power level is returned by this command.

Parameter	Size (Bytes)	Description	Opcode: 0xFC26
Transmit Power Level	1	Transmit output power level defined in steps from 0 to 17 (0x11) Values 0x12 – 0xFF are reserved. See the data sheet for power step definitions	
Return Parameters			
Status	1	Standard BT error code.	
Max Power Level	1	Maximum allowed power level. The returned power level is provided as a power step as defined above.	

A command complete event is generated after the completion of this command.

5.6.12 EM_WritePatchStart

Write a patch into the desired memory. This command may only be called if one of the following conditions is true:

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- *EM_WritePatchStart* has not been called since the chip has rebooted.
- The last *EM_WritePatchStart* or *EM_WritePatchContinue* command has returned the *patch applied* status.
- The *EM_WritePatchAbort* command is sent and returns the command complete successful status.

Parameter	Size (Bytes)	Description	Opcode: 0xFC27
Destination Memory	1	0x00 = The patch should be written into IRAM1. 0x01 = The patch should be written into OTP. 0x02 - 0x0FF = Reserved.	
CRC32	4	CRC32 of the patch data parameter to ensure correct read of this vendor command.	
Data	X	First portion of the patch data that may not exceed 59 bytes (X <= 59).	
Return Parameters			
Status	1	Standard BT error code.	
Patch Status	1	Status code for the patch process (see table below).	

A command complete event is generated after the completion of this command.

Status Code	Name	Meaning
0x01	Patch Applied	Patch has been successfully and completely written into the destination memory. No more action is required.
0x02	Patch Continue	Patch data has been received and more is needed to complete the patching process.
0x03	Bad CRC32	The CRC32 check of the sequence number and/or data failed. The command should be re-sent with the same data to continue the patch process. This could indicate one or more corrupt bits were read from the transport.
0x04	Corrupt Patch	CRC calculation of the container has failed. The patch data sent was incorrect and has been written into the destination memory in its incorrect form.
0x05	RAM Allocation Error	The code patch is unable allocate the requested number of RAM bytes. The patch has been partially written into the destination memory.
0x06	Corrupt Container	The container does not conform to the required format. The destination memory is not altered.
0x07	Container Allocation Error	A free location could not be found in the desired memory to store the container. The destination memory is not altered.
0x08	Write Error	A write to the desired memory has failed. The container is partially written into the destination memory and is corrupt.
0x09	Bad Sequence	The patching system saw an incorrect order of vendor commands or sequence numbers. This could indicate EM_WritePatchStart was called in the middle of an upload or an invalid sequence number was provided.
0x0A	OTP Upload Disallowed	An OTP patch may not be uploaded if patches are present in IRAM.
0x0B	Unknown	An unknown error has occurred during the upload process. The destination memory may or may not be corrupt.

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5.6.13 EM_WritePatchContinue

Continue to write a patch into the desired memory.

Parameter	Size (Bytes)	Description	Opcode: 0xFC28
Sequence Number	2	Number for the patch data chunk. The sequence number must start at 1 for a new patch and increment only when the *patch continue* status is returned. The sequence may only return to 1 for another patch after the *EM_WritePatchStart* command completes successfully.	
CRC32	4	CRC32 of the sequence number and patch data parameters to ensure correct read of this vendor command.	
Data	X	A portion of the patch data that may not exceed 58 bytes (X <= 58).	
Return Parameters			
Status	1	Standard BT error code.	
Patch Status	1	Status code for the patch process (see table in the *EM_WritePatchStart* command).	
Patch Address	4	When the *patch applied* status code is returned, this field contains the address where the patch was written.	

A command complete event is generated after the completion of this command.

5.6.14 EM_WritePatchAbort

Abort the write of a patch. Depending on the progress of the patching process and the destination memory, a half-written patch may be permanently written into the memory. It is recommended to never issue this command unless an unrecoverable patch error occurs.

Parameter	Size (Bytes)	Description	Opcode: 0xFC29
Code Value	4	The code 0xDEADC0DE must be provided to this vendor command for successful completion. Upon successful completion, the patch process is reset and a new patch may be applied with the *EM_WritePatch* vendor command.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the completion of this command.

5.6.15 EM_SetClockSource

Select the clock source.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2A
Clock Source	1	0x00 = High Frequency RC. 0x01 = High Frequency crystal.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the baud rate has been updated.

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5.6.16 EM_SetMemoryMode

Change the state of the selected memory.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2B
Memory Attribute	1	0x00 = Power off OTP. 0x01 = Power on OTP. 0x02 = Disable DRAM1 memory retention. 0x03 = Enable DRAM1 memory retention. 0x04 = Disable DRAM2 memory retention. 0x05 = Enable DRAM2 memory retention. 0x06 = Power off IRAM1. 0x07 = Power on IRAM1. 0x08 – 0xFF reserved	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the specified memory attribute has been set.

5.6.17 EM_GetMemoryUsage

Select the high frequency clock source.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2C
None	0	This command contains no parameters.	
Return Parameters			
Status	1	Standard BT error code.	
Memory Pool Size	4	Total size of the memory pool in bytes.	
Retention Memory Used	4	Retention memory used in bytes.	
Non-retention Memory Used	4	Non-retention memory used in bytes.	
Retention Memory Reserved	4	Size in bytes of memory reserved as retention memory.	

Memory reserved as retention memory can be used for non-retention data, but the data will be maintained in sleep mode. A command complete event is generated containing the memory usage statistics.

5.6.18 EM_SetSleepOptions

Enable or disable sleep mode.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2D
Sleep Options Settings	1	0x00 = Disable automatic sleep mode. 0x01 = Enable automatic sleep mode. 0x02 – 0xFF reserved	
Return Parameters			
Status	1	Standard BT error code.	

A command completion event is generated after setting the sleep option.

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5.6.19 EM_SvldMeasurement

Get the power configuration and supply voltage level detector (SVLD) value corresponding to the SVLD comparator level. The source of the SVLD value VBAT1 in DCDC Step-Down or DCDC Off Configuration, and VCC in DCDC Step-Up or External DCDC Configuration.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2E
None	0	This command contains no parameters.	
Return Parameters			
Status	1	Standard BT error code.	
Power Mode	1	0x00 = DCDC Step-Down Configuration. 0x01 = DCDC Off Configuration. 0x02 = DCDC Step-Up Configuration. 0x03 = External DCDC Configuration. 0x04 – 0xFF reserved	
SVLD Value	1	SVLD comparator value.	

A command complete event is generated containing the SVLD value.

5.6.20 EM_SetEventMask

Enable or disable vendor specific HCI events. The bit position corresponds to the event number to enable when set to 0 and to disable when set to 1.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2F
Mask	4	Event mask.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated after the event mask is updated.

5.6.21 EM_CpuReset

Execute a CPU reset.

Parameter	Size (Bytes)	Description	Opcode: 0xFC32
None	0	This command contains no parameters.	
Return Parameters			
Status	1	Standard BT error code.	

A command complete event is generated prior to issuing the CPU reset operation.

5.6.22 EM_CalculateCrc32Ex

Calculate the 32-bit CRC for the specified continuous address range.

Parameter	Size (Bytes)	Description	Opcode: 0xFC2D
Start Address	4	Starting address.	
End Address	4	Ending address.	
Return Parameters			
Status	1	Standard BT error code.	
CRC32	4	Calculated CRC value.	

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Addresses values outside of the physical memory address space may result in unexpected behaviour of the embedded software. A command complete event is generated after the completion of this command.

5.6.23 EM_PatchQuery

Get the number of containers or patches present and specific information regarding a specific patch. This command can be issued in a loop to obtain information about all containers present in the OTP and IRAM.

Parameter	Size (Bytes)	Description	Opcode: 0xFC34
Patch Index	1	Zero-based index of patch beginning with 0 to the number of patches minus 1	
Return Parameters			
Status	1	Standard BT error code.	
Container Count	2	Number of containers present.	
Transfer Count	2	Number of containers transferred from OTP to IRAM.	
System State	4	Patch system state information (see table below).	
Container Address	4	Address where the container is located.	
Container Size	4	Size of the container	
Container CRC	4	Container CRC	
Build Number	2	Container build number.	
User Build Number	2	Container user specified ID number.	
Container Flags	1	Flags indicating how the patch was applied. 0x00 – Reserved for future use 0x01 – Container was applied 0x02 – Container could not allocate memory 0x03 – Application of container created a gap in the DRAM memory space 0x04 – 0xFF reserved	
Container Version	1	Format version of the container.	
Container Type	1	Type of container: 0x00 – Reserved for future use 0x01 – Configuration 0x02 – Write random data consisting of 32-bit address and data pairs where the 32-bit data is written to the given address 0x03 – Write random byte data consisting of 32 bit address and 8-bit data pairs where the 8-bit data is written to the given address 0x04 – Block write consisting of a single 32-bit address followed by one or more 32-bit values 0x05 – Code patch 0x06 – Unstructured 32-bit data defined by the user 0x07 – Unstructured 8-bit data defined by the user 0x08 – Block write consisting of a single 32-bit address followed by one or more 8-bit values 0x09 – OTP transfer patch that executes from OTP 0x0A – IRAM transfer patch the executes from IRAM 0x0B – 0xFF reserved	
Container ID	1	Container ID.	

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The following table shows the patching system state information:

Description	Value
OTP scan complete	0x00000001
IRAM scan complete	0x00000002
Reserved	0x00000004
Reserved	0x00000008
Container present in OTP	0x00000010
Configuration container present in OTP	0x00000020
Code patch container present in OTP	0x00000040
Container present in IRAM	0x00000080
Configuration container present in IRAM	0x00000100
Code patch container present in IRAM	0x00000200
Reserved	0x00000400
Reserved	0x00000800
Container signature found during scan	0x00001000
A CRC failure encountered during scan	0x00002000
Container present	0x00004000
A code patch in OTP allocated memory	0x00008000
A code patch in IRAM allocated memory	0x00010000
A transfer patch is present	0x00020000
Reserved	0x00040000 - 0x80000000

A command complete event is generated after the specified memory attribute has been set.

5.7 Vendor Specific Events

Table 45 lists the vendor specific events that are supported. The vendor specific events subevent codes are defined to be compatible with those defined for the EM9301 device.

Table 45 Vendor Specific Events

HCI Event	Event Code	Subevent Code
EM_ActiveStateEntered	0xFF	0x01
EM_TestModeEntered	0xFF	0x03
EM_HalNotification	0xFF	0x04

5.7.1 EM_ActiveStateEntered

Report that the active state was entered. This event is sent after one of the following conditions:

- Any hardware reset including POR after link layer is enabled
- Link layer is enabled after exiting from PTM
- Active state is entered after resuming from sleep following the successful execution of the EM_SetPowerModeEx HCI command.
- Active state is entered after the host activates the Wakeup pin

Parameter	Size (Bytes)	Description	Event Code: 0xFF
Subevent Code	1	0x01	

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5.7.2 EM_TestModeEntry

Report that PTM was entered.

Parameter	Size (Bytes)	Description	Event Code: 0xFF
Subevent Code	1	0x03	

5.7.3 EM_HalNotification

Report the HAL notification. Notifications provide information or warnings such as indicating a hardware error is pending.

Parameter	Size (Bytes)	Description	Event Code: 0xFF
Subevent Code	1	0x04	
Notification Event	1	0x00 = No event 0x01 = OTP disabled due to voltage level 0x02 = RF power reduced due to voltage level 0x03 = RF power increased due to restored voltage level 0x04 = RF disabled due to voltage level 0x05 = Power voltage level critical 0x06 = PLL lock lost 0x07 = Memory manager returned a null pointer 0xFF = Unknown error	

5.8 Hardware Error Event Codes

The hardware error event is a standard Bluetooth event where error codes are vendor defined. Table 46 defines these vendor specific hardware error codes.

Table 46 Hardware Event Codes

Parameter	Size (Bytes)	Description	Event Code: 0xFF
Error Code	1	0x00 = No error 0x01 = HCI synchronization lost 0x02 = Reserved 0x03 = Reserved 0x04 = RF system error 0x05 = CPU reset (watchdog) 0x06 = CPU reset (bus error) 0x07 = Crystal oscillator start-up error 0x08 = CRC error in OTP 0x80 = Device not programmed 0xFF = Unknown error	

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6 Changes

The following changes have been made since datasheet V4.0:

- WLCSP reference design schematic and layout updated in Figure 8.
- IOUT for Voh_high2 corrected in Table 9.
- The ENABLE pin characteristics added in Section 2.6.4 above.
- Clarification of the RF matching network requirement in the reference designs in Sections 1.8 and 1.9, and the input impedance specification in Table 18.
- The crystal oscillator frequency trimming and startup current adjustments are now recommended in Table 19.
- Table 34 commercial name changed (removed “+”)
- Added Section 4.7 regarding reflow
- Unstructured data byte and transfer patch container types added to Table 40 and Table 41.
- OCF corrections to Table 44.
- Supported baud rates updated in Section 5.6.2.
- EM_HalNotifications updated in Section 5.7.3.

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