Integrated Device Technology, Inc.

128K x 32 CMOS STATIC RAM MODULES

IDT7MP4060
IDT7MP4095

FEATURES:

- High density 4 megabit static RAM modules
- Low profile 64-pin ZIP (Zig-zag In-line vertical Package), 64-lead, 72-lead SIMMs (Single In-line Memory Modules)
- Fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible
- Gold plated fingers on the SIMM version

PIN CONFIGURATION – 7MP4095

		1	GND	PD_0 - OPEN
PD_0	2	3	PD_1	PD_1 - OPEN
I/O_0	4	5	I/O_8	
I/O_1	6	7	I/O_9	
I/O_2	8	9	I/O_{10}	
I/O_3	10	11	I/O_{11}	
V_{CC}	12	13	A_0	
A_7	14	15	A_1	
A_8	16	17	A_2	
A_9	18	19	I/O_{12}	
I/O_4	20	21	I/O_{13}	
I/O_5	22	23	I/O_{14}	
I/O_6	24	25	I/O_{15}	
I/O_7	26	27	GND	
$\overline{WE}$	28	29	A_{15}	
A_{14}	30	31	$\overline{CS}_2$	
$\overline{CS}_1$	32			
$\overline{CS}_3$		33	$\overline{CS}_4$	
A_{16}	34	35	NC	
GND	36	37	$\overline{OE}$	
I/O_{16}	38	39	I/O_{24}	
I/O_{17}	40	41	I/O_{25}	
I/O_{18}	42	43	I/O_{26}	
I/O_{19}	44	45	I/O_{27}	
A_{10}	46	47	A_3	
A_{11}	48	49	A_4	
A_{12}	50	51	A_5	
A_{13}	52	53	V_{CC}	
I/O_{20}	54	55	A_6	
I/O_{21}	56	57	I/O_{28}	
I/O_{22}	58	59	I/O_{29}	
I/O_{23}	60	61	I/O_{30}	
GND	62	63	I/O_{31}	
	64			

ZIP, SIMM
TOP VIEW

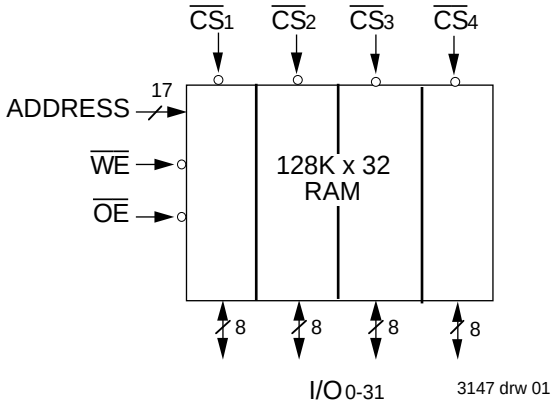
DESCRIPTION:

The IDT7MP4095/7MP4060 are 128K x 32 static RAM modules constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages. The IDT7MP4095/7MP4060 are available with access times as fast as 15ns with minimal power consumption.

The IDT7MP4095 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-lead SIMM (Single In-line Memory Module). The IDT7MP4060 is packaged in a 72-lead SIMM. The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.21 inches thick. At only 0.60 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4095/7MP4060 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

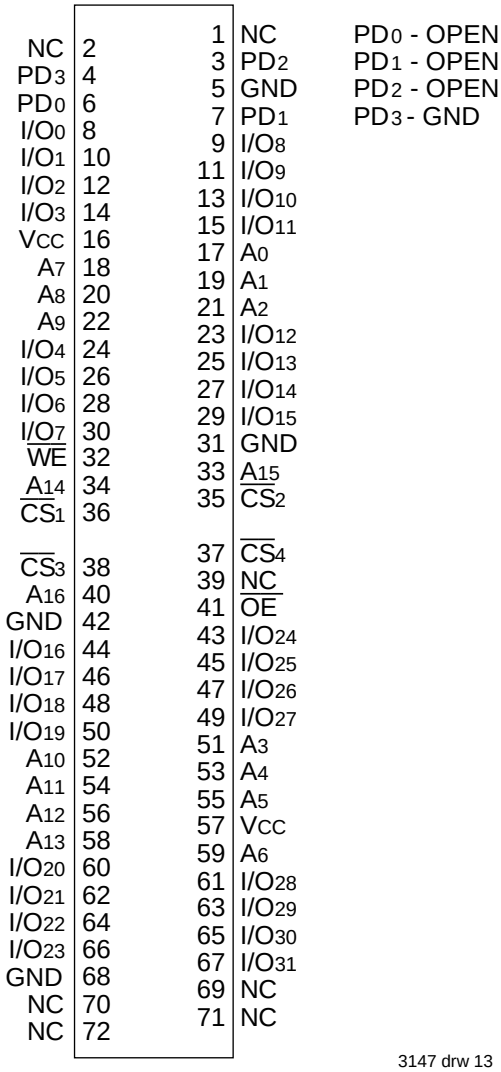
$I/O_{0–31}$	Data Inputs/Outputs
$A_{0–16}$	Addresses
$\overline{CS}_{1–4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground
NC	No Connect

3147 tbl 01

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PIN CONFIGURATION – 7MP4060



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SIMM
TOP VIEW

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data and $\overline{CS}$)	$V_{(IN)}$ = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address, $\overline{WE}$, $\overline{OE}$)	$V_{(IN)}$ = 0V	40	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE: 3147 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	5.8	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3147 tbl 05
1. V_{IL} (min) = –3.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3147 tbl 06

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

3147 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTES: 3147 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Data and $\overline{CS}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage (Address, $\overline{WE}$, and $\overline{OE}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	760	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	160	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	60	mA

3147 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3147 tbl 08

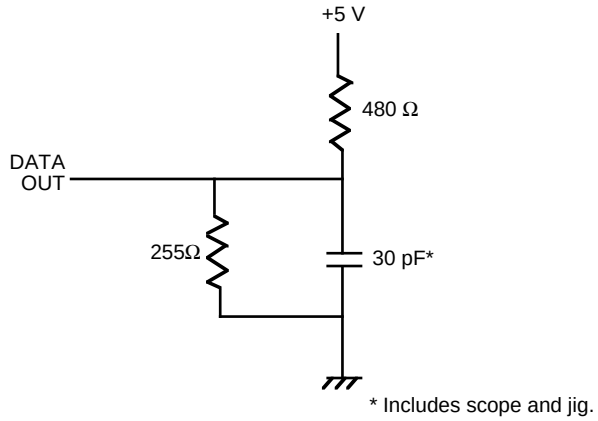


Figure 1. Output Load

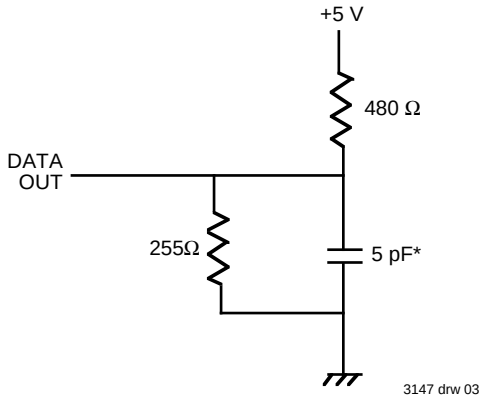


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

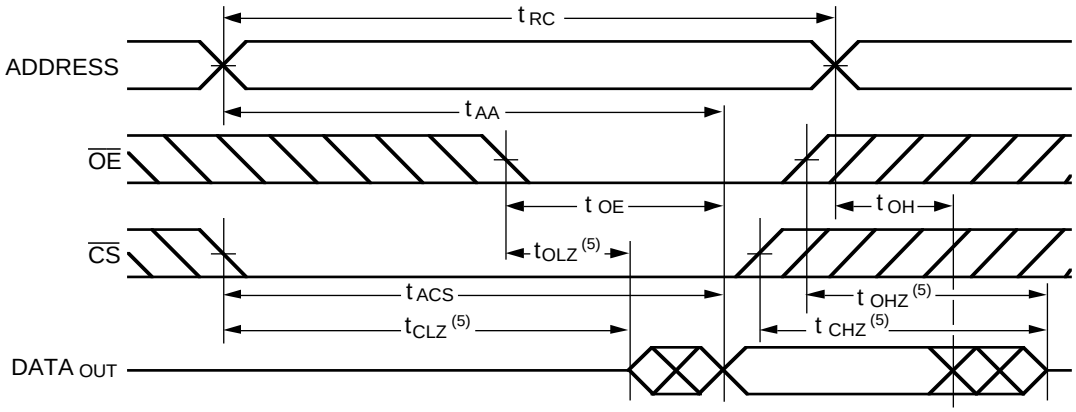
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
Read Cycle						
t_{RC}	Read Cycle Time	15	—	20	—	ns
t_{AA}	Address Access Time	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	ns
t_{CLZ}(1)	Chip Select to Output in Low Z	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	—	8	—	12	ns
t_{OHZ}(1)	Output Disable to Output in High Z	—	8	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	15	—	20	ns
Write Cycle						
t_{WC}	Write Cycle Time	15	—	20	—	ns
t_{CW}	Chip Select to End of Write	12	—	18	—	ns
t_{AW}	Address Valid to End of Write	12	—	18	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	18	—	ns
t_{WR}	Write Recovery Time	0	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High Z	—	8	—	13	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	3	—	3	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

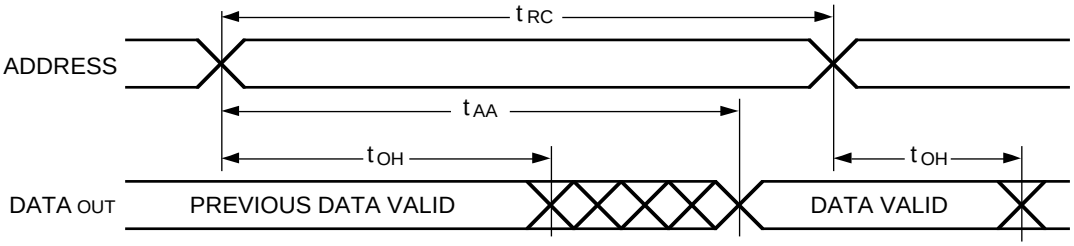
3147 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



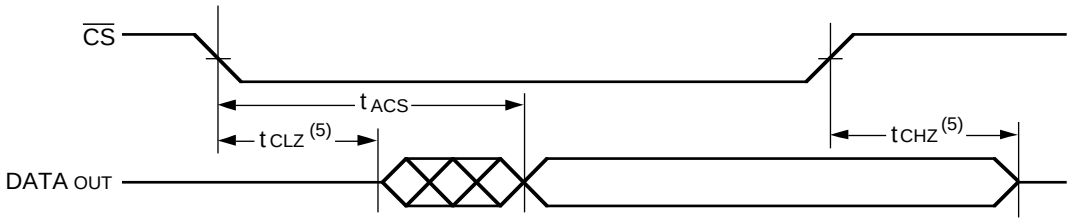
3147 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3147 drw 05

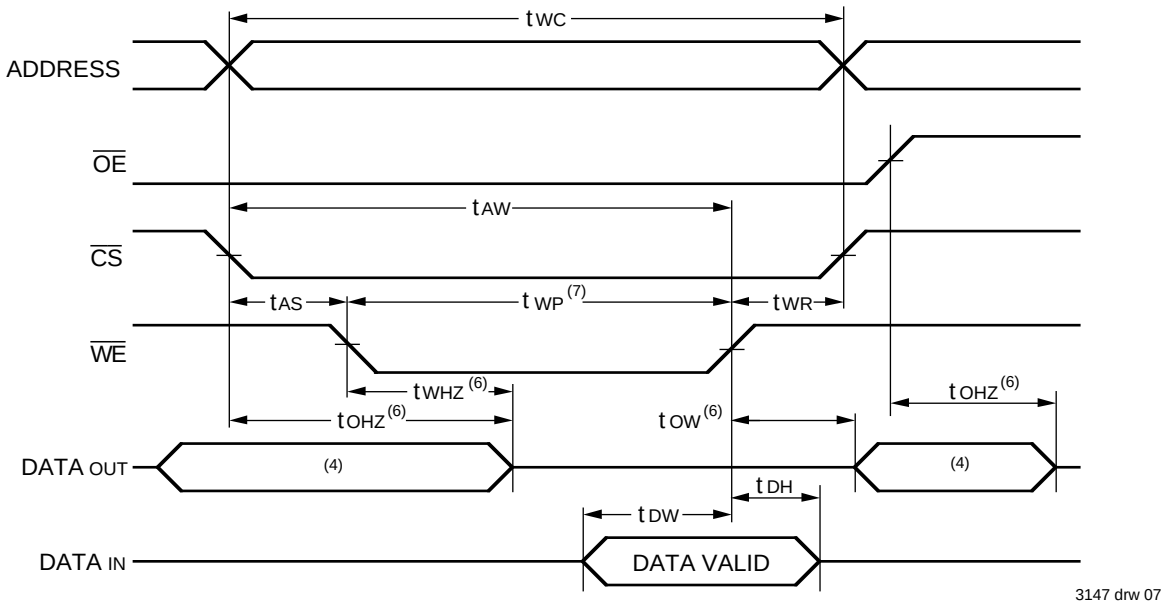
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



3147 drw 06

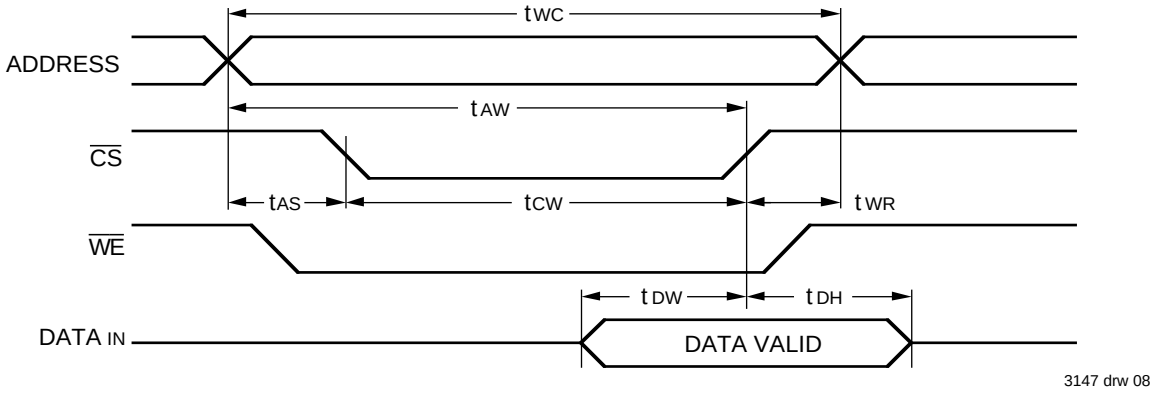
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



3147 drw 07

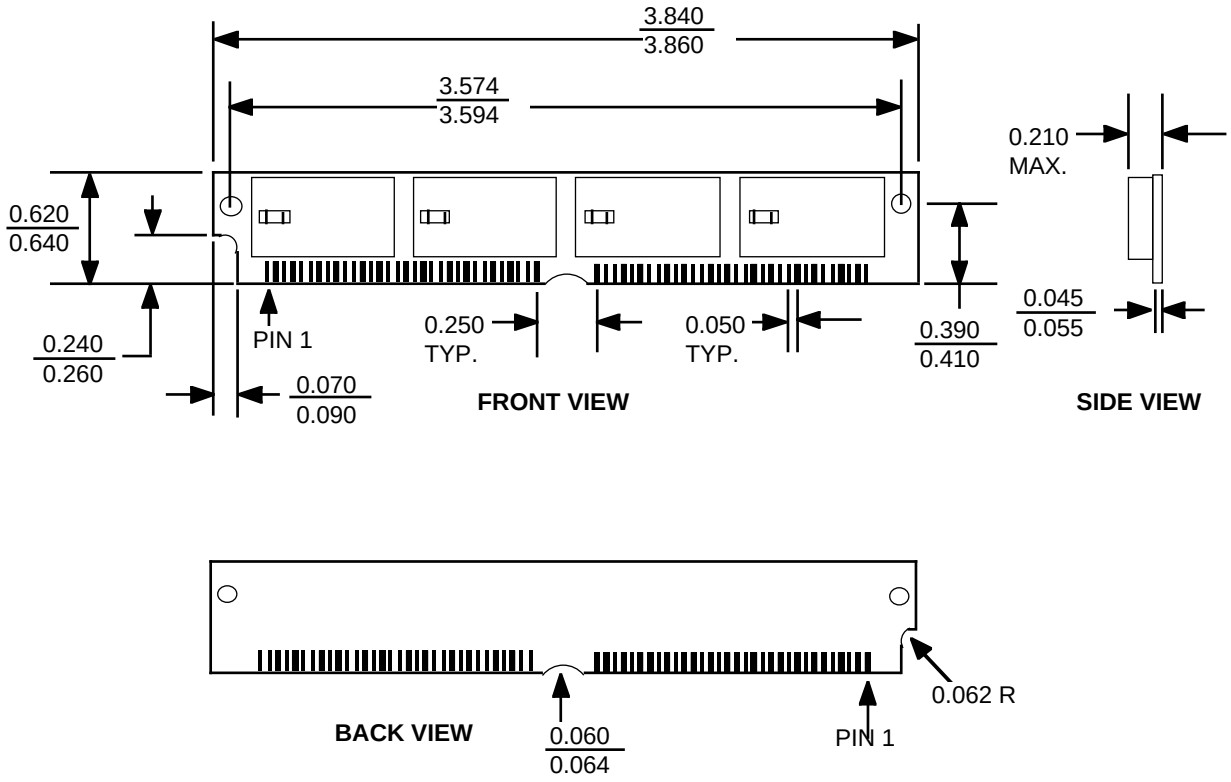
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



3147 drw 08

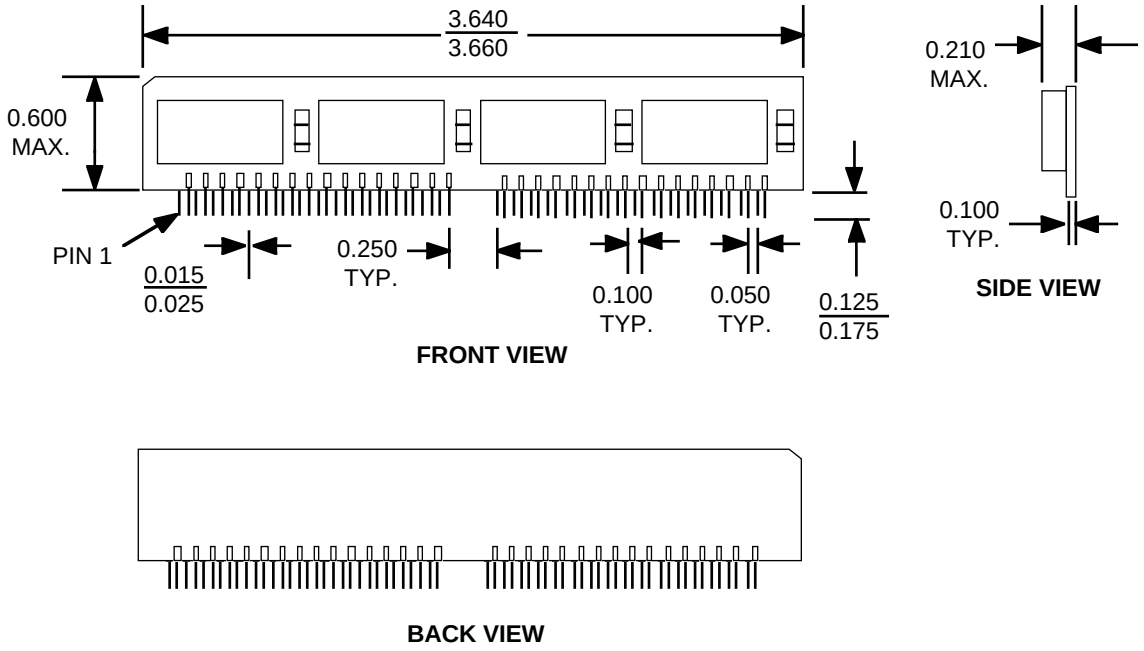
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$).

PACKAGE DIMENSIONS – IDT7MP4095
SIMM VERSION



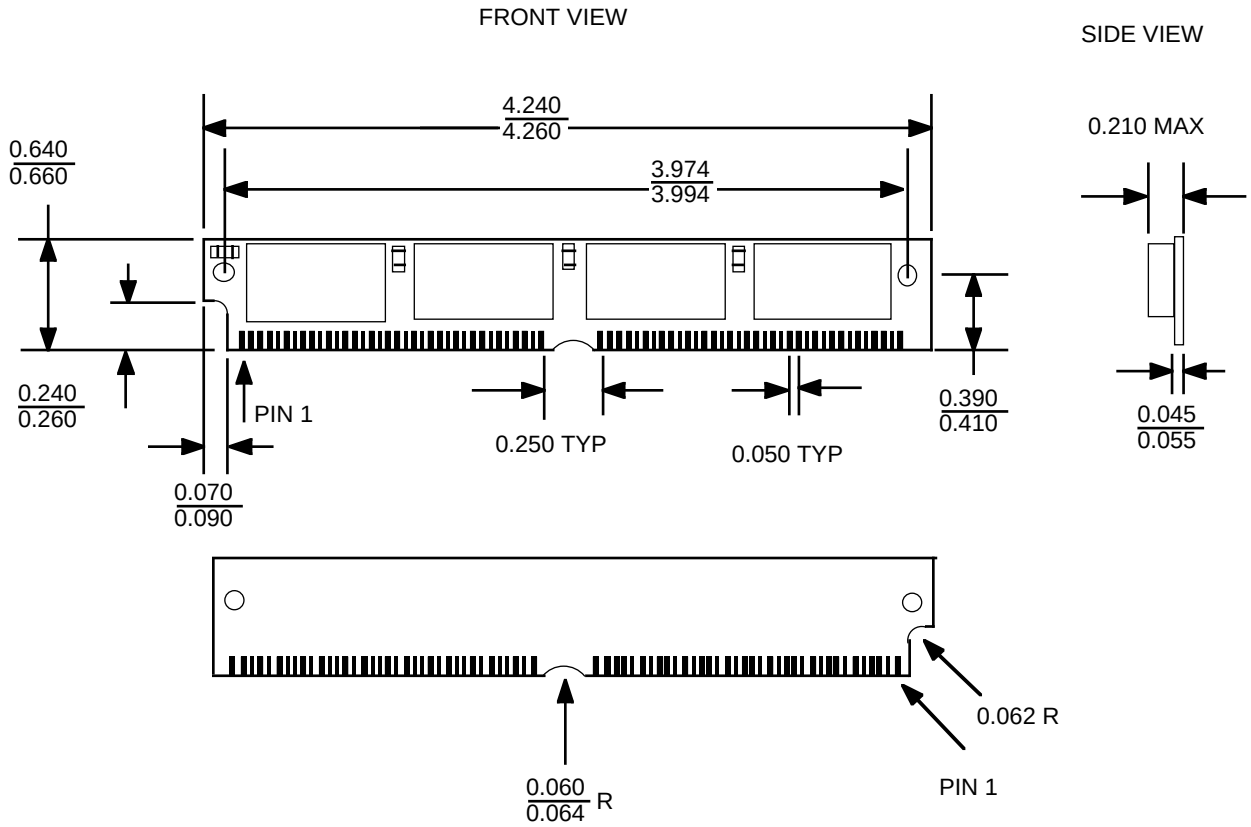
3147 drw 09

ZIP VERSION



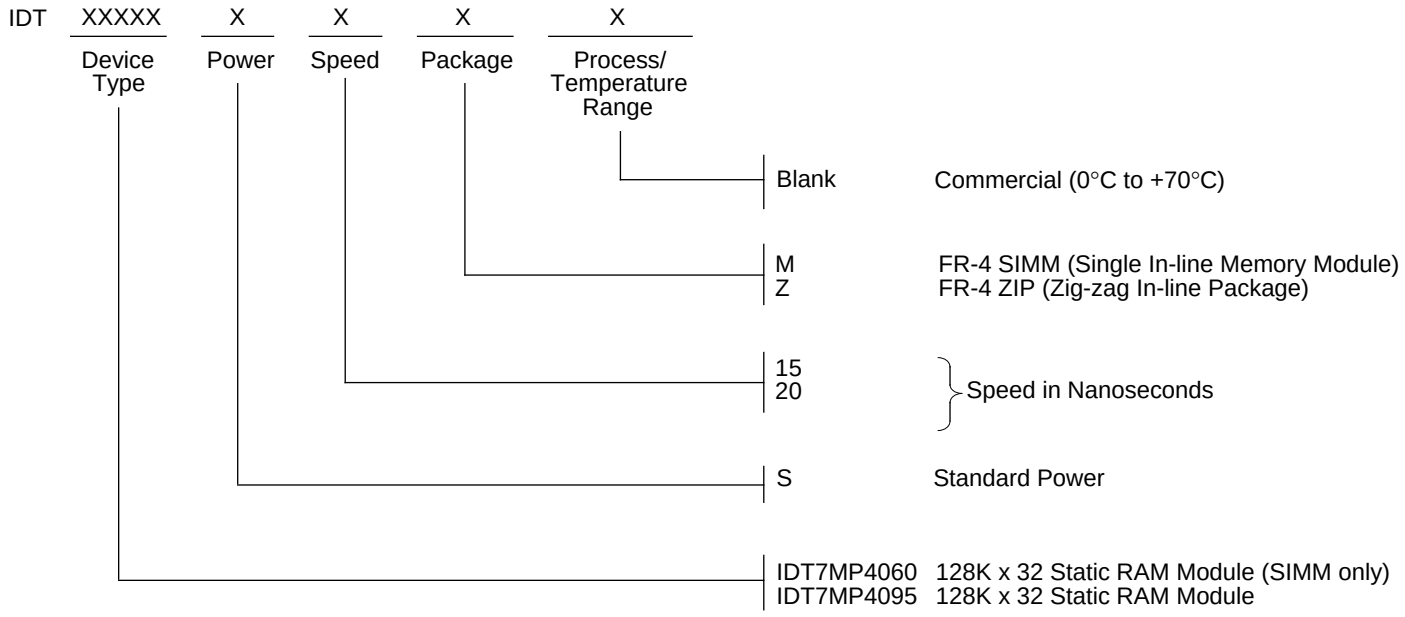
3147 drw 10

PACKAGE DIMENSIONS – IDT7MP4060



3147 drw 11

ORDERING INFORMATION



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