MAX16834

High-Power LED Driver with Integrated High-Side LED Current Sense and PWM Dimming MOSFET Driver

General Description

The MAX16834 is a current-mode high-brightness LED (HB LED) driver for boost, boost-buck, SEPIC, and high-side buck topologies. In addition to driving an n-channel power MOSFET switch controlled by the switching controller, it also drives an n-channel PWM dimming switch to achieve LED PWM dimming. The MAX16834 integrates all the building blocks necessary to implement a fixed-frequency HB LED driver with wide-range dimming control. The MAX16834 features constant-frequency peak current-mode control with programmable slope compensation to control the duty cycle of the PWM controller.

A dimming driver designed to drive an external n-channel MOSFET in series with the LED string provides wide-range dimming control up to 20kHz. In addition to PWM dimming, the MAX16834 provides analog dimming using a DC input at REFI. The programmable switching frequency (100kHz to 1MHz) allows design optimization for efficiency and board space reduction. A single resistor from RT/SYNC to ground sets the switching frequency from 100kHz to 1MHz while an external clock signal at RT/SYNC disables the internal oscillator and allows the MAX16834 to synchronize to an external clock. The MAX16834's integrated high-side current-sense amplifier eliminates the need for a separate high-side LED current-sense amplifier in boost-buck applications.

The MAX16834 operates over a wide supply range of 4.75V to 28V and includes a 3A sink/source gate driver for driving a power MOSFET in high-power LED driver applications. It can also operate at input voltages greater than 28V in boost configuration with an external voltage clamp. The MAX16834 is also suitable for DC-DC converter applications such as boost or boost-buck. Additional features include external enable/disable input, an on-chip oscillator, fault indicator output ($\overline{FLT}$) for LED open/short or overtemperature conditions, and an overvoltage protection sense input (OVP+) for true overvoltage protection.

The MAX16834 is available in a thermally enhanced 4mm x 4mm, 20-pin TQFN-EP package and in a thermally enhanced 20-pin TSSOP-EP package and is specified over the automotive -40°C to +125°C temperature range.

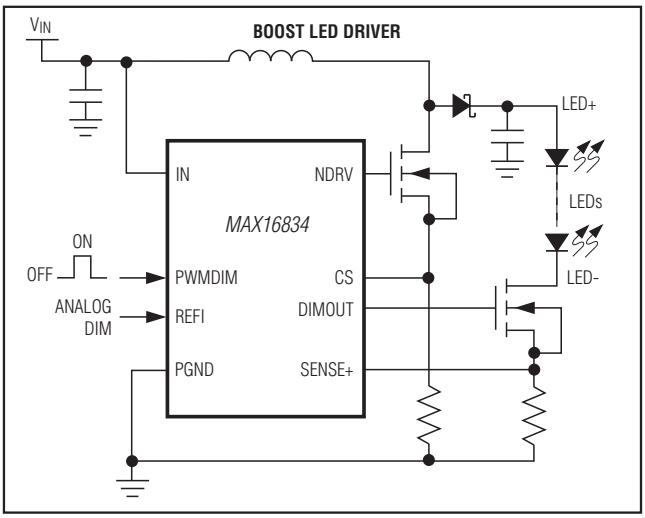
Applications

- Single-String LED LCD Backlighting
- Automotive Rear and Front Lighting
- Projection System RGB LED Light Sources
- Architectural and Decorative Lighting (MR16, M111)
- Spot and Ambient Lights
- DC-DC Boost/Boost-Buck Converters

Benefits and Features

- Integration Minimizes BOM for High-Brightness LED Driver with a Wide Dimming Range Saving Space and Cost
  - Constant-Frequency, Peak Current-Mode Control with Programmable Slope Compensation
  - Integrated PWM Dimming MOSFET Driver
  - 3000:1 PWM Dimming/Analog Dimming
  - Integrated High-Side Current-Sense Amplifier for LED Current Sense in Boost-Buck Converter
  - Internal 7V Low-Dropout Regulator
- Simple Optimization for Efficiency, Board Space and Input Operating Range
  - Supports Boost, Buck-Boost, SEPIC, and High-Side Buck Topologies
  - 100kHz to 1MHz Programmable High-Frequency Operation
  - External Clock Synchronization Input
  - Wide Input Operating Voltage Range (4.75V to 28V)
  - Works for Input Voltage > 28V with External Voltage Clamp on V_{IN} for Boost Converter
  - 20-Pin TQFN-EP and TSSOP-EP Packages
- Protection Features Increase System Reliability
  - Programmable UVLO
  - Programmable True Differential Overvoltage Protection
  - Fault Output (FLT) for Overvoltage, Overcurrent, and Thermal-Warning Faults

Simplified Application Circuit



Ordering Information and Pin Configurations appear at end of data sheet.

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Absolute Maximum Ratings

IN, HV, LV to SGND .....-0.3V to +30V
OVP+, SENSE+, DIMOUT, CLV to SGND .....-0.3V to +30V
SENSE+ to LV.....-0.3V to +0.3V
HV, IN to LV .....-0.3V to +30V
OVP+, CLV, DIMOUT to LV .....-0.3V to +6V
PGND to SGND .....-0.3V to +0.3V
V_{CC} to SGND.....-0.3V to +12V
NDRV to PGND.....-0.3V to (V_{CC} + 0.3V)
All Other Pins to SGND.....-0.3V to +6V
NDRV Continuous Current.....±50mA
DIMOUT Continuous Current.....±2mA

V_{CC} Short-Circuit Current to SGND Duration 1s
Continuous Power Dissipation (T_A = +70°C)
QFN, TQFN (derate 25.6mW/°C* above +70°C).....2051mW
TSSOP (derate 26.5mW/°C above +70°C) 2122mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**As per JEDEC51 standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA})
QFN, TQFN .....39°C/W
TSSOP .....37.7°C/W

Junction-to-Case Thermal Resistance (θ_{JC})
QFN, TQFN .....6°C/W
TSSOP .....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = V_{HV} = 12V, V_{UVEN} = 5V, V_{LV} = V_{PWMDIM} = V_{SGND}, C_{VCC} = 4.7µF, C_{LCV} = 100nF, C_{REF} = 100nF, R_{SENSE+} = 0.1Ω, R_{RT} = 10kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		4.75		28	V
Quiescent Supply Current	I_Q	Excluding I_{LED}		6	10	mA
Shutdown Supply Current	I_{SHDN}	V_{UVEN} = 0V		30	60	µA
INTERNAL LINEAR REGULATOR (V_{CC})						
Output Voltage	V_{CC}	0 ≤ I_{CC} ≤ 50mA, 9.5V ≤ V_{IN} ≤ 28V	6.3	7	7.7	V
Dropout Voltage	V_{DO}	I_{CC} = 35mA (Note 2)		0.65	1	V
Short-Circuit Current		V_{CC} = 0V, V_{IN} = 12V	80		300	mA
LINEAR REGULATOR (CLV)						
Output Voltage	(V_{CLV} - V_{LV})	0 ≤ I_{CLV} ≤ 2mA, 6V ≤ V_{HV} ≤ 28V, 6V ≤ $V_{(HV-LV)}$ ≤ 22V	4.7	5	5.3	V
Dropout Voltage	V_{DO}	I_{CLV} = 2mA, 0 ≤ V_{LV} ≤ 23.3V (Note 3)			0.5	V
Short-Circuit Current		V_{CLV} = 12V, V_{IN} = 12V, V_{HV} = 24V	2.2		10	mA
REFERENCE VOLTAGE (REF)						
Output Voltage	V_{REF}	0 ≤ I_{REF} ≤ 1mA, 4.75V ≤ V_{IN} ≤ 28V	3.625	3.70	3.775	V
REF Short-Circuit Current		V_{REF} = 0V		30		mA
UNDERVOLTAGE LOCKOUT/ENABLE INPUT (UVEN)						
UVEN On Threshold Voltage	V_{UVEN_THUP}		1.395	1.435	1.475	V
UVEN Threshold Voltage Hysteresis				200		mV
Input Leakage Current	I_{LEAK}	V_{UVEN} = 0V		1		µA
PWMDIM						
PWMDIM On Threshold Voltage	V_{PWMDIM}		1.395	1.435	1.475	V

Electrical Characteristics (continued)

(V_{IN} = V_{HV} = 12V, V_{UVEN} = 5V, V_{LV} = V_{PWMDIM} = V_{SGND}, C_{VCC} = 4.7µF, C_{LCV} = 100nF, C_{REF} = 100nF, R_{SENSE+} = 0.1Ω, R_{RT} = 10kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWMDIM Threshold Voltage Hysteresis				200		mV
Input Leakage Current		V_{PWMDIM} = 0V		1		µA
OSCILLATOR						
Oscillator Frequency	f_{OSC}	$R_{RT/SYNC}$ = 5kΩ	0.9	1	1.1	MHz
		$R_{RT/SYNC}$ = 25kΩ	180	200	220	kHz
Oscillator Frequency Range		(Note 4)	100		1000	kHz
External Sync Input Clock High Threshold		(Note 4)	2			V
External Sync Input Clock Low Threshold		(Note 4)			0.4	V
External Sync Input High Pulse Width		(Note 4)	200			ns
Maximum External Sync Period				50		µs
SLOPE COMPENSATION (SC)						
SC Pullup Current	I_{SCPU}	V_{SC} = 100mV	80	100	120	µA
SC Discharge Resistance	R_{SCD}	V_{SC} = 100mV		8		Ω
REFI						
REFI Input Bias Current		V_{REFI} = 1V		1		µA
REFI Input Common-Mode Range		(Note 4)	0		2	V
SENSE+						
SENSE+ Input Bias Current		(V_{SENSE+} - V_{LV}) = 100mV			250	µA
HIGH-SIDE LED CURRENT-SENSE AMPLIFIER (V_{SENSE+} - V_{LV})						
Input Offset Voltage		V_{LV} > 5V, (V_{SENSE+} - V_{LV}) = 5mV	-2.4	0	+2.4	mV
Voltage Gain	A_V	V_{LV} > 5V, (V_{SENSE+} - V_{LV}) = 0.2V	9.7	9.9	10.1	V/V
3dB Bandwidth		(V_{SENSE+} - V_{LV}) = 0.1V, no load		1.8		MHz
		(V_{SENSE+} - V_{LV}) = 0.02V, no load		600		kHz
LOW-SIDE LED CURRENT-SENSE AMPLIFIER						
Input Offset Voltage		V_{LV} < 1V, (V_{SENSE+} - V_{LV}) = 0V	-2	0	+2	mV
Voltage Gain	A_V	V_{LV} < 1V, (V_{SENSE+} - V_{LV}) = 0.2V	9.7	9.9	10.1	V/V
3dB Bandwidth				600		kHz
CURRENT ERROR AMPLIFIER (TRANSCONDUCTANCE AMPLIFIER)						
Transconductance	g_m	V_{COMP} = 2V, V_{PWMDIM} = 5V	400	500	600	µS
Open-Loop DC Gain	A_V			60		dB
Input Offset Voltage			-10	0	+10	mV
COMP Voltage Range	V_{COMP}	(Note 4)	0.4		2.5	V
PWM COMPARATOR						
Input Offset Voltage			0.6	0.65	0.70	V
Propagation Delay	t_{PD}	50mV overdrive		40		ns

Electrical Characteristics (continued)

(V_{IN} = V_{HV} = 12V, V_{UVEN} = 5V, V_{LV} = V_{PWMDIM} = V_{SGND}, C_{VCC} = 4.7µF, C_{LCV} = 100nF, C_{REF} = 100nF, R_{SENSE+} = 0.1Ω, R_{RT} = 10kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

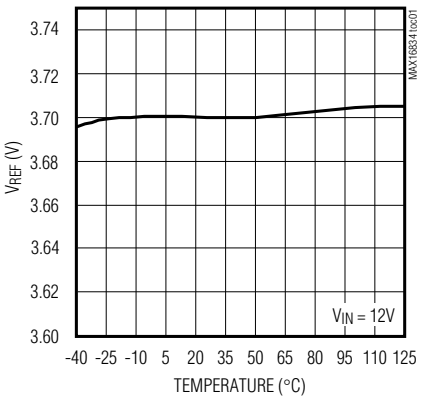
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum On-Time	$t_{ON(MIN)}$	On-time includes blanking time		100		ns
Duty Cycle		(Note 4)	90		99.5	%
CURRENT PEAK LIMIT COMPARATOR						
Trip Threshold Voltage			0.25	0.3	0.35	V
Propagation Delay		50mV overdrive with respect to NDRV		40		ns
OVERVOLTAGE PROTECTION INPUT (OVP+)						
OVP+ On Threshold Voltage	V_{OVP_ON}		1.375	1.435	1.495	V
OVP+ Hysteresis				200		mV
OVP+ Input Leakage Current		(V_{OVP} - V_{LV}) = 1.235V	-1		+1	µA
HIGH-SIDE LED SHORT COMPARATOR						
Off Threshold		V_{CLV} - V_{LV}	4.0	4.3	4.6	V
On Threshold		V_{CLV} - V_{LV}	4.1	4.4	4.7	V
Error Reject Blankout		f_{OSC} = 500kHz		256		µs
LOW-SIDE LED SHORT COMPARATOR						
Off Threshold			0.27	0.30	0.33	V
Error Reject Blankout				5		µs
HICCUP TIMER						
Hiccup Time		f_{OSC} = 500kHz		8.2		ms
GATE-DRIVER OUTPUT (NDRV)						
NDRV Peak Pullup Current		V_{CC} = 7V		3		A
NDRV Peak Pulldown Current		V_{CC} = 7V		3		A
p-Channel MOSFET R_{DSON}		(V_{CC} - V_{NDRV}) = 0.1V		1.2	1.9	Ω
n-Channel MOSFET R_{DSON}		V_{NDRV} = 0.1V		0.9	1.7	Ω
DIMOUT						
DIMOUT Peak Pullup Current		(V_{CLV} - V_{LV}) = 5V	25	50		mA
DIMOUT Peak Pulldown Current		(V_{CLV} - V_{LV}) = 5V	25	50		mA
p-Channel MOSFET R_{DSON}		(V_{CLV} - V_{DIMOUT}) = 0.1V		31		Ω
n-Channel MOSFET R_{DSON}		(V_{DIMOUT} - V_{LV}) = 0.1V		25		Ω
PWMDIM to DIMOUT Propagation Delay				200		ns
FAULT FLAG ($\overline{FLT}$)						
$\overline{FLT}$ Pulldown Current		$V_{\overline{FLT}}$ = 0.2V	2	5	10	mA
$\overline{FLT}$ Leakage Current		$V_{\overline{FLT}}$ = 1.0V		1		µA
Thermal Warning On Threshold				+140		°C
Thermal Warning Threshold Hysteresis				20		°C

Note 2: Dropout voltage is defined as V_{IN} - V_{CC}, when V_{CC} is 100mV below the value of V_{CC} for V_{IN} = 9.5V.
Note 3: Dropout is defined as V_{HV} - V_{CLV}, when V_{CLV} is 100mV below the value of V_{CLV} for V_{HV} = 8V.
Note 4: Not production tested. Guaranteed by design.

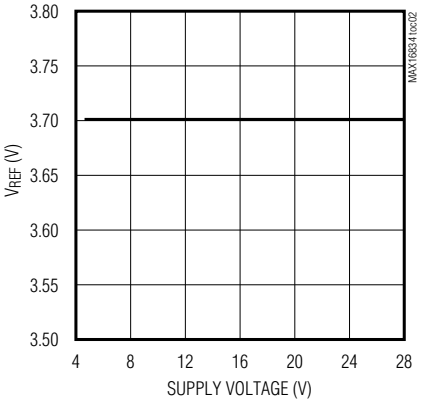
Typical Operating Characteristics

(V_{IN} = V_{HV} = 12V, V_{UVEN} = 5V, V_{LV} = V_{PWMDIM} = V_{SGND}, C_{VCC} = 4.7µF, C_{LCV} = 100nF, C_{REF} = 100nF, R_{SENSE+} = 0.1Ω, R_{RT} = 10kΩ, T_A = +25°C, unless otherwise noted.)

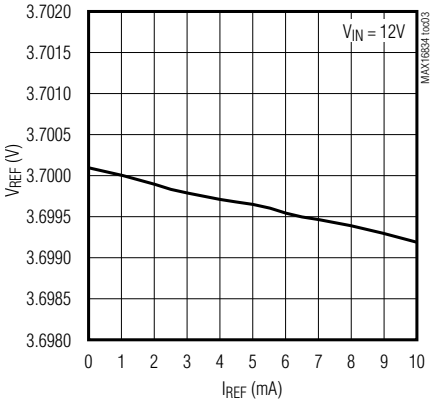
VREF vs. TEMPERATURE



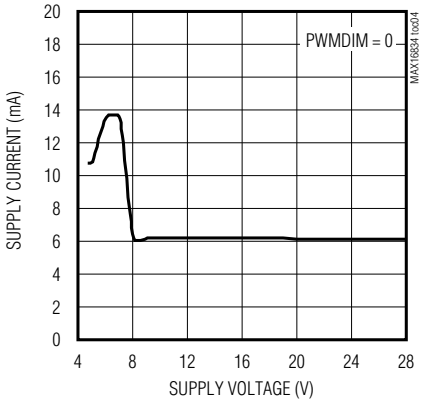
VREF vs. SUPPLY VOLTAGE



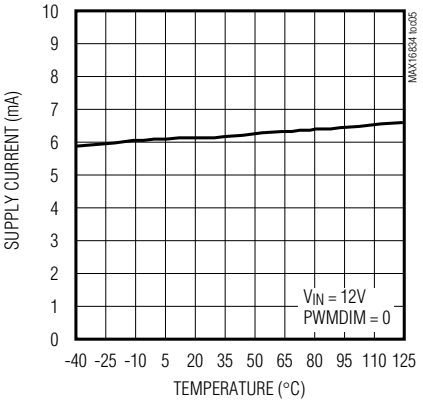
VREF vs. IREF



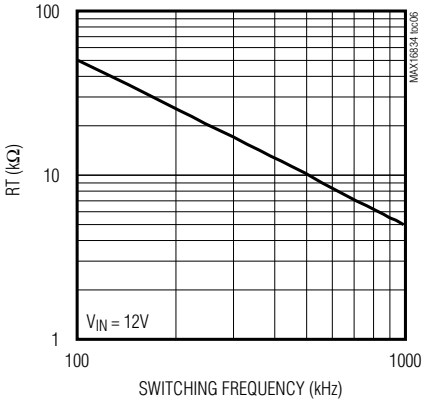
SUPPLY CURRENT vs. SUPPLY VOLTAGE



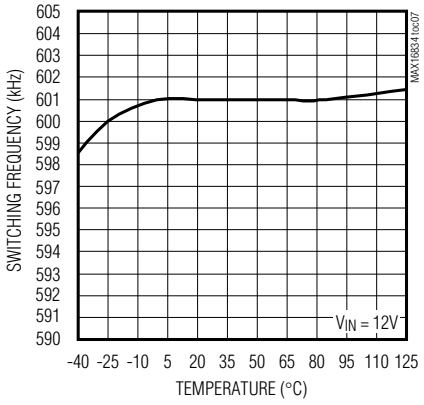
SUPPLY CURRENT vs. TEMPERATURE



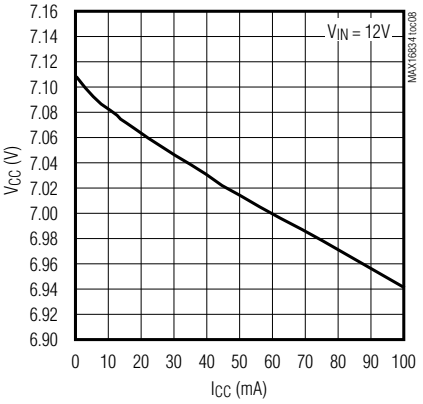
RT vs. SWITCHING FREQUENCY



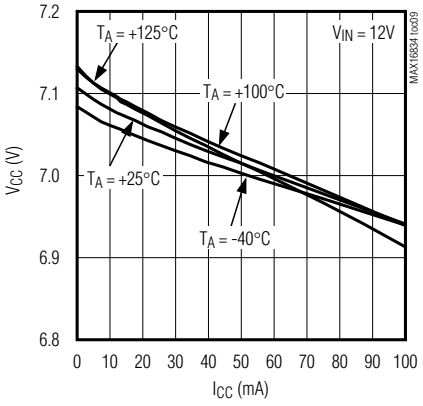
SWITCHING FREQUENCY vs. TEMPERATURE



VCC vs. ICC



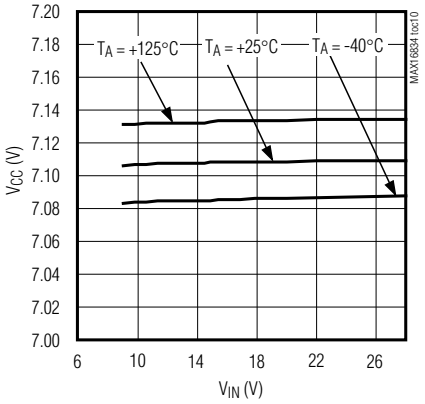
VCC vs. ICC



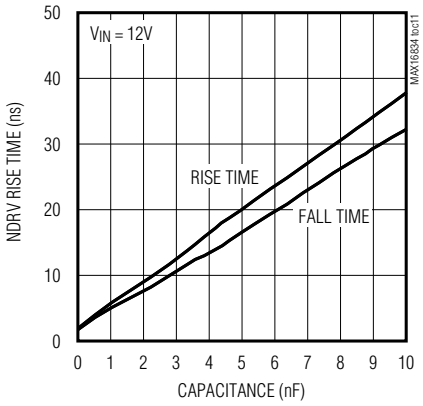
Typical Operating Characteristics (continued)

(V_{IN} = V_{HV} = 12V, V_{UVEN} = 5V, V_{LV} = V_{PWMDIM} = V_{SGND}, C_{VCC} = 4.7µF, C_{LCV} = 100nF, C_{REF} = 100nF, R_{SENSE+} = 0.1Ω, R_{RT} = 10kΩ, T_A = +25°C, unless otherwise noted.)

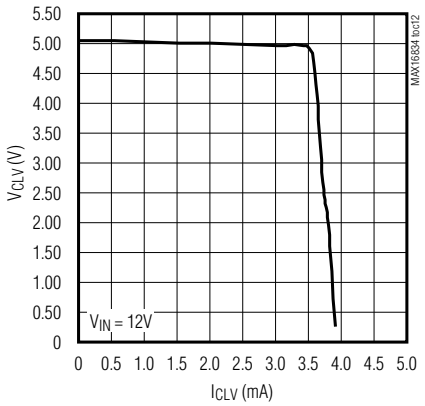
VCC vs. VIN



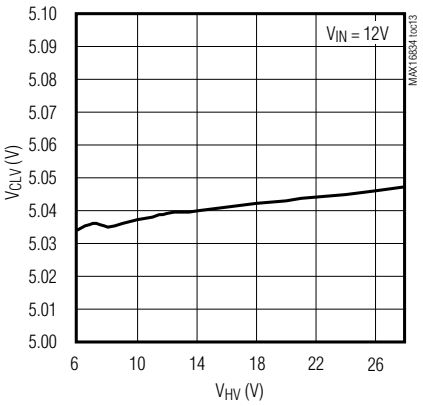
NDRV RISE/FALL TIME vs. CAPACITANCE



VCLV vs. ICLV



VCLV vs. VHV



Pin Description

PIN		NAME	FUNCTION
QFN, TQFN	TSSOP		
1	3	OVP+	LED-String Overvoltage Protection Input. Connect a resistive voltage-divider between the positive output, OVP+, and LV to set the overvoltage threshold. OVP+ has a 1.435V threshold voltage with a 200mV hysteresis.
2	4	SGND	Signal Ground
3	5	COMP	Error-Amplifier Output. Connect an RC network from COMP to SGND for stable operation. See the *Feedback Compensation* section.
4	6	REF	3.7V Reference Output Voltage. Bypass REF to SGND with a 0.1µF to 0.22µF ceramic
5	7	REFI	Current Reference Input. V_{REFI} provides a reference voltage for the current-sense amplifier to set the LED current.
6	8	SC	Current-Mode Slope Compensation Setting. Connect to an appropriate external capacitor from SC to SGND to generate a ramp signal for stable operation.

Pin Description (continued)

PIN		NAME	FUNCTION
QFN, TQFN	TSSOP		
7	9	$\overline{FLT}$	Active-Low, Open-Drain Fault Indicator Output. See the *Fault Indicator ($\overline{FLT}$)* section.
8	10	RT/SYNC	Resistor-Programmable Switching Frequency Setting/Sync Control Input. Connect a resistor from RT/SYNC to SGND to set the switching frequency. Drive RT/SYNC to synchronize the switching frequency with an external clock.
9	11	UVEN	Undervoltage-Lockout (UVLO) Threshold/Enable Input. UVEN is a dual-function adjustable UVLO threshold input with an enable feature. Connect UVEN to V_{IN} through a resistive voltage-divider to program the UVLO threshold. Observe the absolute maximum value for this pin.
10	12	PWMDIM	PWM Dimming Input. Connect to an external PWM signal for dimming operation.
11	13	CS	Current-Sense Amplifier Positive Input. Connect a resistor from CS to PGND to set the inductor peak current limit.
12	14	PGND	Power Ground
13	15	NDRV	External n-Channel Gate-Driver Output
14	16	V_{CC}	7V Low-Dropout Voltage Regulator. Bypass to PGND with at least a 1µF low-ESR ceramic capacitor. V_{CC} provides power to the n-channel gate driver (NDRV).
15	17	IN	Positive Power-Supply Input. Bypass to PGND with at least a 0.1µF ceramic capacitor.
16	18	HV	High-Side Positive Supply Input Referred to LV. HV provides power to high-side linear regulator
17	19	CLV	5V High-Side Regulator Output. CLV provides power to the dimming MOSFET driver. Connect a 0.1µF to 1µF ceramic capacitor from CLV to LV for stable operation.
18	20	DIMOUT	External Dimming MOSFET Gate Driver. DIMOUT is capable of sinking/sourcing 50mA.
19	1	LV	High-Side Reference Voltage Input. Connect to SGND for boost configuration. Connect to IN for boost-buck configuration.
20	2	SENSE+	LED Current-Sense Positive Input. Connect a bypass capacitor of at least 0.1µF between SENSE+ and LV close to the IC.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the main IC ground connection. EP must be connected to SGND.

Detailed Description

The MAX16834 is a current-mode, high-brightness LED (HB LED) driver designed to control a single-string LED current regulator with two external n-channel MOSFETs.

The MAX16834 integrates all the building blocks necessary to implement a fixed-frequency HB LED driver with wide-range dimming control. The MAX16834 allows implementation of different converter topologies such as SEPIC, boost, boost-buck, or high-side buck current regulator.

The MAX16834 features a constant-frequency, peak-current-mode control with programmable slope compensation to control the duty cycle of the PWM controller. A dimming driver offers a wide-range dimming control for the external n-channel MOSFET in series with the LED string. In addition to PWM dimming, the MAX16834 allows for analog dimming of LED current.

The MAX16834 switching frequency (100kHz to 1MHz) is adjustable using a single resistor from RT/SYNC. The MAX16834 disables the internal oscillator and synchronizes if an external clock is applied to RT/SYNC. The switching MOSFET driver sinks and sources up to 3A, making it suitable for high-power MOSFETs driving in HB LED applications, and the dimming control allows for wide PWM dimming at frequencies up to 20kHz.

The MAX16834 is suitable for boost and boost-buck LED drivers (Figures 2 and 3).

The MAX16834 alone operates over a wide 4.75V to 28V supply range. With a voltage clamp that limits the IN pin voltage to less than 28V, it can operate in boost configuration for input voltages greater than 28V. Additional features include external enable/disable input, an on-chip oscillator, fault indicator output ($\overline{FLT}$) for LED open/short or overtemperature conditions, and an overvoltage protection circuit for true differential overvoltage protection (Figure 1).

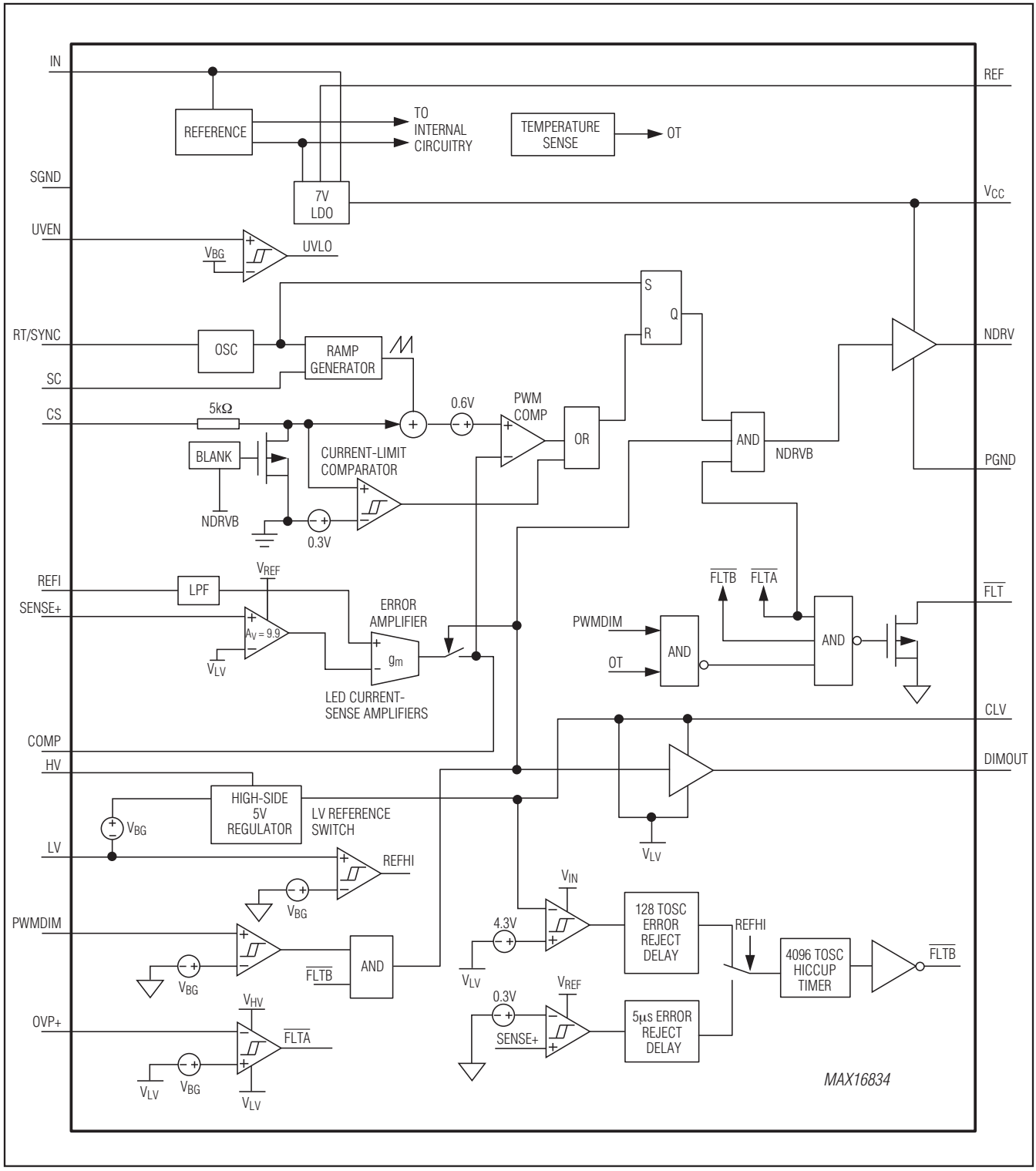


Figure 1. Internal Block Diagram

The MAX16834 is also suitable for DC-DC converter applications such as boost or boost-buck (Figures 6 and 7). Other applications include boost LED drivers with automotive load dump protection (Figure 4) and high-side buck LED drivers (Figure 5).

Undervoltage Lockout/Enable

The MAX16834 features an adjustable UVLO using the enable input (UVEN). Connect UVEN to V_{IN} through a resistive divider to set the UVLO threshold. The MAX16834 is enabled when the V_{UVEN} exceeds the 1.435V (typ) threshold. See the *Setting the UVLO Threshold* section for more information.

UVEN also functions as an enable/disable input to the device. Drive UVEN low to disable the output and high to enable the output.

Reference Voltage (REF)

The MAX16834 features a 3.7V reference output, REF. REF provides power to most of the internal circuit blocks except for the output drivers and is capable of sourcing 1mA to external circuits. Connect a 0.1µF to 0.22µF ceramic capacitor from REF to SGND. Connect REF to REFI through a resistive divider to set the LED current.

Reference Input (REFI)

The output current is proportional to the voltage at REFI. Applying an external DC voltage at REFI or using a potentiometer from REF to SGND allows analog dimming of the output current.

High-Side Reference Voltage Input (LV)

LV is a reference input. Connect LV to SGND for boost and SEPIC topologies. Connect LV to IN for boost-buck and high-side buck topologies.

Dimming Driver Regulator Input Voltage (HV)

The voltage at HV provides the input voltage for the dimming driver regulator. For boost or SEPIC topology, connect HV either to IN or to V_{CC}. For boost-buck, connect HV to a voltage higher than IN. The voltage at HV must not exceed 28V with respect to PGND. For the high-side buck, connect HV to IN.

Dimming MOSFET Driver (DIMOUT)

The MAX16834 requires an external n-channel MOSFET for PWM dimming. Connect the gate of the MOSFET to the output of the dimming driver, DIMOUT, for normal operation. The dimming driver is capable of sinking or sourcing up to 50mA of current.

n-Channel MOSFET Switch Driver (NDRV)

The MAX16834 drives an external n-channel switching MOSFET. NDRV swings between V_{CC} and PGND. NDRV is capable of sinking/sourcing 3A of peak current, allowing the MAX16834 to switch MOSFETs in high-power applications. The average current demanded from the supply to drive the external MOSFET depends on the total gate charge (Q_G) and the operating frequency of the converter, f_{SW}. Use the following equation to calculate the driver supply current I_{NDRV} required for the switching MOSFET:

$$I_{NDRV} = Q_G \times f_{SW}$$

Pulse Dimming Inputs (PWMDIM)

The MAX16834 offers a dimming input (PWMDIM) for pulse-width modulating the output current. PWM dimming can be achieved by driving PWMDIM with a pulsating voltage source. When the voltage at PWMDIM is greater than 1.435V, the PWM dimming MOSFET turns on and when the voltage on PWMDIM is below 1.235V, the PWM dimming MOSFET turns off.

High-Side Linear Regulator (V_{CLV})

The MAX16834's 5V high-side regulator (CLV) powers up the dimming MOSFET driver. V_{CLV} is measured with respect to LV and sources up to 2mA of current. Bypass CLV to LV with a 0.1µF to 1µF low-ESR ceramic capacitor. The maximum voltage on CLV with respect to PGND must not exceed 28V. This limits the input voltage for boost-buck topology.

Low-Side Linear Regulator (V_{CC})

The MAX16834's 7V low-side linear regulator (V_{CC}) powers up the switching MOSFET driver with sourcing capability of up to 50mA. Use at least a 1µF low-ESR ceramic capacitor from V_{CC} to PGND for stable operation.

LED Current-Sense Input (SENSE+)

The differential voltage from SENSE+ to LV is fed to an internal current-sense amplifier. This amplified signal is then connected to the negative input of the transconductance error amplifier. The voltage gain factor of this amplifier is 9.9 (typ).

Whenever V_{LV} is greater than 5V, the input impedance of the LED current-sense amplifier seen at the SENSE+ pin is 1kΩ ±30%. In that condition, a bias current of 20µA (±30%) is pulled from SENSE+, in addition to the current due to the 1kΩ resistor. When V_{LV} is less than 1V, the amplifier input (SENSE+ pin) is in high impedance and the bias current of 20µA (±30%) is pushed out of that pin.

Always have a bypass capacitor of at least 0.1µF value between SENSE+ and LV and close to the IC.

Internal Transconductance Error Amplifier

The MAX16834 has a built-in transconductance amplifier used to amplify the error signal inside the feedback loop. The amplified current-sense signal is connected to the negative input of the g_m amplifier with the current reference connected to REFI. The output of the op amp is controlled by the input at PWMDIM. When the signal at PWMDIM is high, the output of the op amp connects to COMP; when the signal at PWMDIM is low, the output of the op amp disconnects from COMP to preserve the charge on the compensation capacitor. When the voltage at PWMDIM goes high, the voltage on the compensation capacitor forces the converter into a steady state. COMP is connected to the negative input of the PWM comparator with CMOS inputs, which draw very little current from the compensation capacitor at COMP and thus prevent discharge of the compensation capacitor when the PWMDIM input is low.

Internal Oscillator

The internal oscillator of the MAX16834 is programmable from 100kHz to 1MHz using a single resistor at RT/SYNC. Use the following formula to calculate the switching frequency:

$$f_{OSC}\ (kHz) = \frac{5000k\Omega}{RT(k\Omega)} \times\ (kHz)$$

where RT is the resistor from RT/SYNC to SGND.

The MAX16834 synchronizes to an external clock signal at RT/SYNC. The application of an external clock disables the internal oscillator allowing the MAX16834 to use the external clock for switching operation. The internal oscillator is enabled if the external clock is absent for more than 50µs. The synchronizing pulse minimum width for proper synchronization is 200ns.

Switching MOSFET Current-Sense Input (CS)

CS is part of the current-mode control loop. The switching control uses the voltage on CS, set by R_{CS}, to terminate the on pulse width of the switching cycle, thus achieving peak current-mode control. Internal leading-edge blanking is provided to prevent premature turn-off of the switching MOSFET in each switching cycle.

Slope Compensation (SC)

The MAX16834 uses an internal-ramp generator for slope compensation. The ramp signal also resets at the beginning of each cycle and slews at the rate programmed by the external capacitor connected at SC. The current source charging the capacitor is 100µA.

Overvoltage Protection (OVP+)

OVP+ sets the overvoltage threshold limit across the LEDs. Use a resistive divider between output OVP+ and LV to set the overvoltage threshold limit. An internal overvoltage protection comparator senses the differential voltage across OVP+ and LV. If the differential voltage is greater than 1.435V, NDRV is disabled and $\overline{FLT}$ asserts. When the differential voltage drops by 200mV, NDRV is enabled and $\overline{FLT}$ deasserts. The PWM dimming MOSFET is still controlled by the PWMDIM input.

Fault Indicator ($\overline{FLT}$)

The MAX16834 features an active-low, open-drain fault indicator ($\overline{FLT}$). $\overline{FLT}$ asserts when one of the following occurs:

1) Overvoltage across the LED string
2) Short-circuit condition across the LED string, or
3) Overtemperature condition

When the output voltage drops below the overvoltage set point minus the hysteresis, $\overline{FLT}$ deasserts. Similarly during the short-circuit period, the fault signal deasserts when the dimming MOSFET is on, which happens every hiccup cycle during short circuit. During overtemperature fault, the $\overline{FLT}$ signal is the inverse of the PWM input.

Applications Information

Setting the UVLO Threshold

The UVLO threshold is set by resistors R1 and R2 (see Figure 2). The MAX16834 turns on when the voltage across R2 exceeds 1.435V, the UVLO threshold. Use the following equation to set the desired UVLO threshold:

$$V_{UVEN} = 1.435V(R1+R2)/R2$$

In a typical application, use a 10kΩ resistor for R2 and then calculate R1 based on the desired UVLO threshold.

Setting the Overvoltage Threshold

The overvoltage threshold is set by resistors R4 and R9 (see Figure 2). The overvoltage circuit in the MAX16834 is activated when the voltage on OVP+ with respect to LV exceeds 1.435V. Use the following equation to set the desired overvoltage threshold:

$$V_{OV} = 1.435V(R4+R9)/R9$$

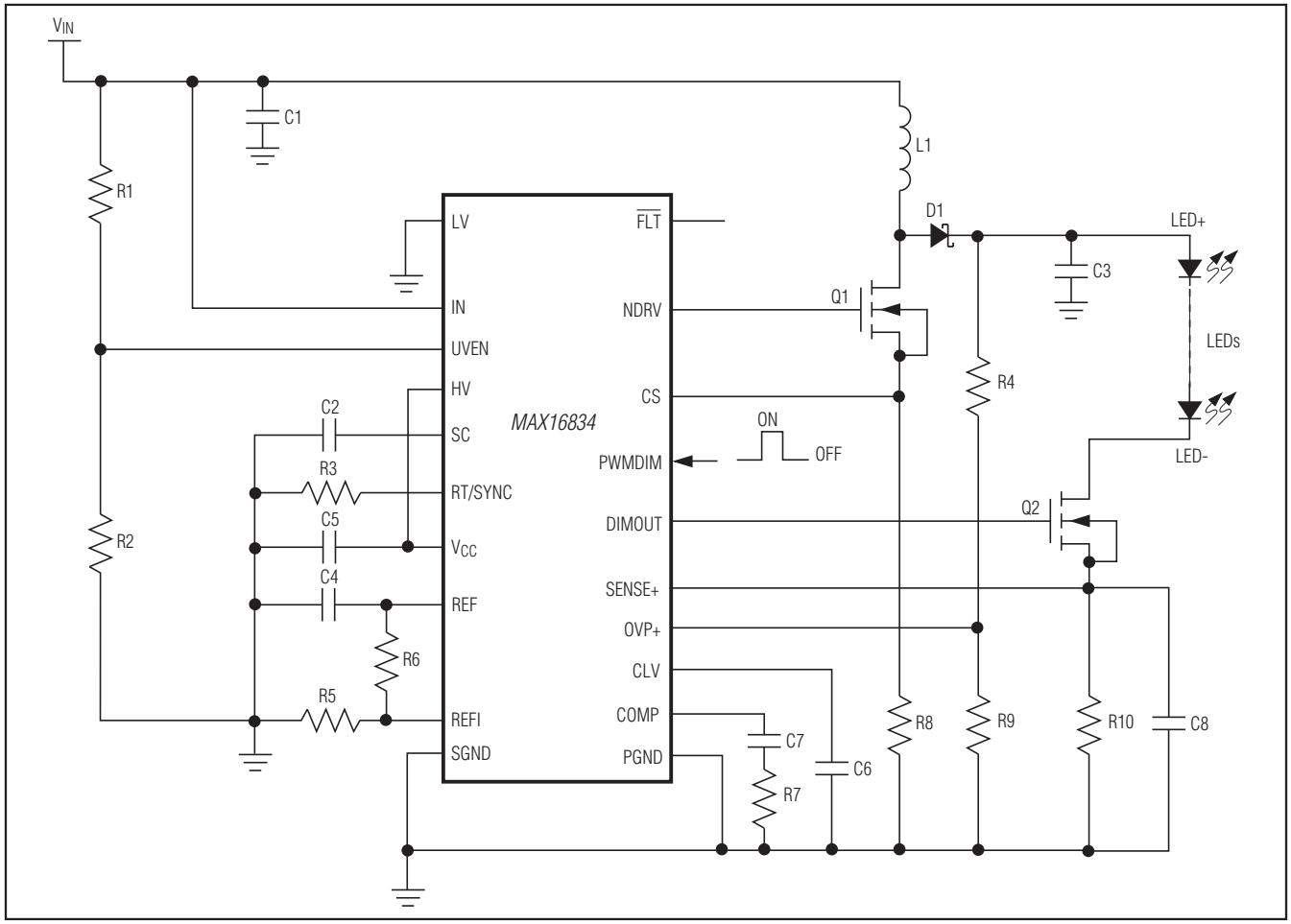


Figure 2. Boost LED Driver

Programming the LED Current

The LED current is programmed using the voltage on REFI and the LED current-sense resistor R10 (see Figure 2). The current is given by:

$$I_{LED} = \frac{V_{REF} \times R5}{R10 \times (R6 + R5) \times 9.9} (A)$$

where V_{REF} is 3.7V and the resistors R5, R6, and R10 are in ohms. The regulation voltage on the LED current-sense resistor must not exceed 0.3V to prevent activation of the LED short-circuit protection circuit.

Boost Configuration

In the boost converter (Figure 2), the average inductor current varies with the line voltage. The maximum average current occurs at the lowest line voltage. For the boost converter, the average inductor current is equal to the input current.

Calculate maximum duty cycle using the below equation.

$$D_{MAX} = \frac{V_{LED} + V_D - V_{INMIN}}{V_{LED} + V_D - V_{FET}}$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of the rectifier diode D1 in volts (approximately 0.6V), V_{INMIN} is the minimum input supply voltage in volts, and V_{FET} is the average drain to source voltage of the MOSFET Q1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of the maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the following equations to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔI_L, and the peak inductor current IL_P in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple (ΔI_L) to be ±30% of the average inductor current:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

and

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

The inductance value (L) of the inductor L1 in henries (H) is calculated as:

$$L = \frac{(V_{INMIN} - V_{FET}) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔI_L is in amperes.

Choose an inductor that has a minimum inductance greater than the calculated value. The current rating of the inductor should be higher than IL_P at the operating temperature.

Boost-Buck Configuration

In the boost-buck LED driver (Figure 3), the average inductor current is equal to the input current plus the LED current.

Calculate maximum duty cycle using the following equation:

$$D_{MAX} = \frac{V_{LED} + V_D}{V_{LED} + V_D + V_{INMIN} - V_{FET}}$$

where V_{LED} is the forward voltage of the LED string in volts, V_D is the forward drop of the rectifier diode D1 (approximately 0.6V) in volts, V_{INMIN} is the minimum input supply voltage in volts, and V_{FET} is the average drain to source voltage of the MOSFET Q1 in volts when it is on. Use an approximate value of 0.2V initially to calculate D_{MAX}. A more accurate value of maximum duty cycle can be calculated once the power MOSFET is selected based on the maximum inductor current.

Use the below equations to calculate the maximum average inductor current IL_{AVG}, peak-to-peak inductor current ripple ΔI_L, and the peak inductor current IL_P in amperes:

$$IL_{AVG} = \frac{I_{LED}}{1 - D_{MAX}}$$

Allowing the peak-to-peak inductor ripple ΔI_L to be ±30% of the average inductor current:

$$\Delta I_L = IL_{AVG} \times 0.3 \times 2$$

$$IL_P = IL_{AVG} + \frac{\Delta I_L}{2}$$

The inductance value (L) of the inductor L1 in henries is calculated as:

$$L = \frac{(V_{INMIN} - V_{FET}) \times D_{MAX}}{f_{SW} \times \Delta I_L}$$

where f_{SW} is the switching frequency in hertz, V_{INMIN} and V_{FET} are in volts, and ΔI_L is in amperes. Choose an inductor that has a minimum inductance greater than the calculated value.

Peak Current-Sense Resistor (R8)

The value of the switch current-sense resistor R8 for the boost and boost-buck configurations is calculated as follows:

$$R8 = \frac{0.25}{(IL_P \times 1.25)} \Omega$$

where 0.25V is the minimum peak current-sense threshold, IL_P is the peak inductor current in amperes, and the factor 1.25 provides a 25% margin to account for tolerances. The worst cycle-by-cycle current limiter triggers at 350mV (max). The I_{SAT} of the inductor should be higher than 0.35V/R8.

Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL and ESR effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance. To minimize audible noise generated by the ceramic capacitors during PWM dimming, it may be necessary to minimize the number of ceramic capacitors on the output. In these cases an additional electrolytic or tantalum capacitor provides most of the bulk capacitance.

Boost and boost-buck configurations: The calculation of the output capacitance is the same for both boost and boost-buck configurations. The output ripple is caused by the ESR and the bulk capacitance of the output capacitor if the ESL effect is considered negligible. For simplicity, assume that the contributions from

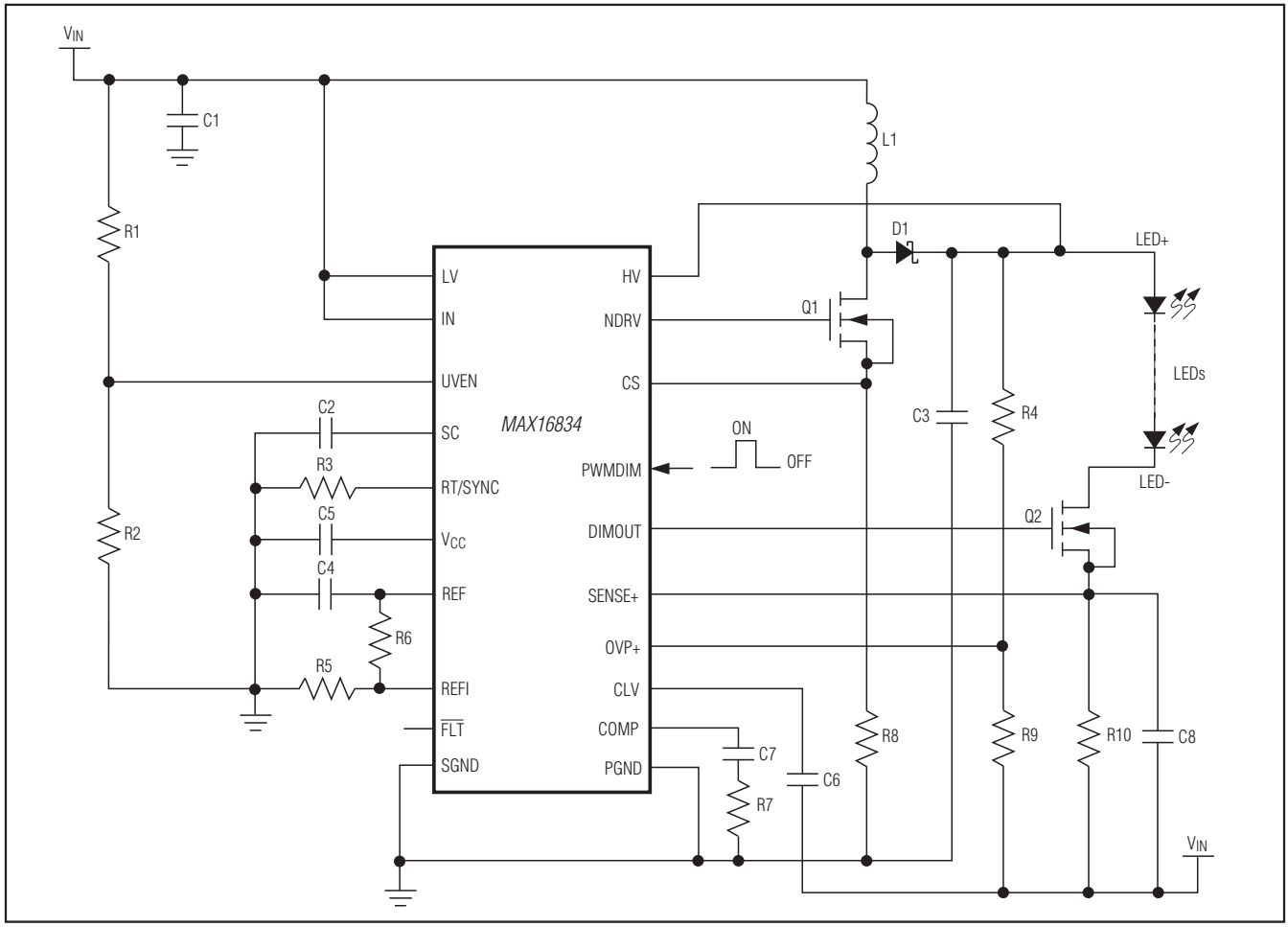


Figure 3. Boost-Buck LED Driver (V_{LED+} < 28V)

ESR and the bulk capacitance are equal, allowing 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{OUT} \geq \frac{I_{LED} \times 2 \times D_{MAX}}{\Delta V_{OUTRIPPLE} \times f_{SW}}$$

where I_{LED} is in amperes, C_{OUT} is in farads, f_{SW} is in hertz, and $\Delta V_{OUTRIPPLE}$ is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor. Based on this, the ESR of the output capacitor is given by:

$$ESR_{COUT} < \frac{\Delta V_{OUTRIPPLE}(\Omega)}{(IL_P \times 2)}$$

where IL_P is the peak inductor current in amperes.

Use the below equation to calculate the RMS current rating of the output capacitor:

$$I_{COUT(RMS)} = \sqrt{(IL_{AVG} \times (1 - D_{MAX}))^2 \times D_{MAX} + (IL_{AVG} \times D_{MAX})^2 \times (1 - D_{MAX})}$$

Input Capacitor

The input filter capacitor bypasses the ripple current drawn by the converter and reduces the amplitude of high-frequency current conducted to the input supply. The ESR, ESL, and the bulk capacitance of the input capacitor contribute to the input ripple. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current from the converter.

For the boost configuration, the input current is the same as the inductor current. For boost-buck

configuration, the input current is the inductor current minus the LED current. But for both configurations, the ripple current that the input filter capacitor has to supply is the same as the inductor ripple current with the condition that the output filter capacitor should be connected to ground for boost-buck configuration. This reduces the size of the input capacitor, as the inductor current is continuous with maximum ±30% ripple. Neglecting the effect of LED current ripple, the calculation of the input capacitor for boost as well as boost-buck configurations is the same.

Neglecting the effect of the ESL, the ESR, and the bulk capacitance at the input contributes to the input voltage ripple. For simplicity, assume that the contribution from the ESR and the bulk capacitance is equal. This allows 50% of the ripple for the bulk capacitance. The capacitance is given by:

$$C_{IN} \geq \frac{\Delta I_L}{4 \times \Delta V_{IN} \times f_{SW}}$$

where ΔI_L is in amperes, C_{IN} is in farads, f_{SW} is in hertz, and ΔV_{IN} is in volts. The remaining 50% of allowable ripple is for the ESR of the output capacitor. Based on this, the ESR of the input capacitor is given by:

$$ESR_{CIN} < \frac{\Delta V_{IN}}{\Delta I_L \times 2}$$

where ΔI_L is in amperes, ESR_{CIN} is in ohms, and ΔV_{IN} is in volts.

Use the below equation to calculate the RMS current rating of the input capacitor:

$$I_{CIN(RMS)} = \frac{\Delta I_L}{2\sqrt{3}}$$

Slope Compensation

Slope compensation should be added to converters with peak current-mode control operating in continuous conduction mode with more than 50% duty cycle to avoid current loop instability and subharmonic oscillations. The minimum amount of slope added to the peak inductor current to stabilize the current control loop is half of the falling slope of the inductor.

In the MAX16834, the slope compensating ramp is added to the current-sense signal before it is fed to the PWM comparator. Connect a capacitor (C2 in the application circuit) from SC to ground for slope compensation. This capacitor is charged with a 100µA current source and discharged at the beginning of each switching cycle to generate the slope compensation ramp.

The value of the slope compensation capacitor C2 is calculated as shown below:

Boost configuration:

$$C2 = \frac{3 \times L \times 100 \times 10^{-6}}{(V_{LED} - V_{INMIN}) \times R8 \times 2}$$

where C2 is in farads, L is the inductance of the inductor L1 in henries, 100µA is the pullup current from SC, V_{LED} and V_{INMIN} are in volts, and R8 is the switch current-sense resistor in ohms.

Boost-buck configuration:

$$C2 = \frac{3 \times L \times 100 \times 10^{-6}}{(V_{LED}) \times R8 \times 2}$$

where C2 is in farads, L is the inductance of the inductor L1 in henries, 100µA is the pullup current from SC, V_{LED} is in volts, and R8 is the switch current-sense resistor in ohms.

Selection of Power Semiconductors

Switching MOSFET

The switching MOSFET (Q1) should have a voltage rating sufficient to withstand the maximum output voltage together with the diode drop of the rectifier diode D1 and any possible overshoot due to ringing caused by parasitic inductances and capacitances. Use a MOSFET with a drain-to-source voltage rating higher than that calculated by the following equations:

Boost configuration:

$$V_{DS} = (V_{LED} + V_D) \times 1.2$$

where V_{DS} is the drain-to-source voltage in volts and V_D is the forward drop of the rectifier diode D1. The factor of 1.2 provides a 20% safety margin.

Boost-buck configuration:

$$V_{DS} = (V_{LED} + V_{INMAX} + V_D) \times 1.2$$

where V_{DS} is the drain-to-source voltage in volts and V_D is the forward drop of the rectifier diode D1. The factor of 1.2 provides a 20% safety margin.

The continuous drain current rating of the selected MOSFET, when the case temperature is at +70°C, should be greater than the value calculated by the fol-

lowing equation. The MOSFET must be mounted on a board as per manufacturer specifications to dissipate the heat.

The RMS current rating of the switching MOSFET Q1 is calculated as follows for boost and boost-buck configurations:

$$ID_{RMS} = \left(\sqrt{(IL_{AVG})^2 \times D_{MAX}} \right) \times 1.3$$

where ID_{RMS} is the MOSFET Q1's drain RMS current in amperes.

The MOSFET Q1 will dissipate power due to both switching losses as well as conduction losses. The conduction losses in the MOSFET is calculated as follows:

$$P_{COND} = (IL_{AVG})^2 \times D_{MAX} \times R_{DSON}$$

where R_{DSON} is the on-resistance of Q1 in ohms with an assumed junction temperature of +100°C, P_{COND} is in watts, and IL_{AVG} is in amperes.

Use the following equations to calculate the switching losses in the MOSFET:

Boost configuration:

$$P_{SW} = \left(\frac{IL_{AVG} \times V_{LED}^2 \times C_{GD} \times f_{SW}}{2} \right) \times \left(\frac{1}{IG_{ON}} + \frac{1}{IG_{OFF}} \right)$$

Boost-buck configuration:

$$P_{SW} = \left(\frac{IL_{AVG} \times (V_{LED} + V_{INMAX})^2 \times C_{GD} \times f_{SW}}{2} \right) \times \left(\frac{1}{IG_{ON}} + \frac{1}{IG_{OFF}} \right)$$

where IG_{ON} and IG_{OFF} are the gate currents of the MOSFET Q1 in amperes when it is turned on and turned off, respectively, V_{LED} and V_{INMAX} are in volts, IL_{AVG} is in amperes, f_{SW} is in hertz, and C_{GD} is the gate-to-drain MOSFET capacitance in farads.

Choose a MOSFET that has a higher power rating than that calculated by the following equation when the MOSFET case temperature is at +70°C:

$$P_{TOT}(W) = P_{COND}(W) + P_{SW}(W)$$

Rectifier Diode

Use a Schottky diode as the rectifier (D1) for fast switching and to reduce power dissipation. The selected Schottky diode must have a voltage rating 20% above the maximum converter output voltage. The maximum converter output voltage is V_{LED} in boost configuration and V_{LED} + V_{INMAX} in boost-buck configuration.

The current rating of the diode should be greater than I_D in the following equation:

$$I_D = IL_{AVG} \times (1 - D_{MAX}) \times 1.5$$

Dimming MOSFET

Select a dimming MOSFET (Q2) with continuous current rating at +70°C, higher than the LED current by 30%. The drain-to-source voltage rating of the dimming MOSFET must be higher than V_{LED} by 20%.

Feedback Compensation

The LED current control loop comprising of the switching converter, the LED current amplifier, and the error amplifier should be compensated for stable control of the LED current. The switching converter small-signal transfer function has a right half-plane (RHP) zero for both boost and boost-buck configurations as the inductor current is in continuous conduction mode. The RHP zero adds a 20dB/decade gain together with a 90° phase lag, which is difficult to compensate. The easiest way to avoid this zero is to roll off the loop gain to 0dB at a frequency less than one-fifth of the RHP zero frequency with a -20dB/decade slope.

The worst-case RHP zero frequency (f_{ZRHP}) is calculated as follows:

Boost configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED}}$$

Boost-buck configuration:

$$f_{ZRHP} = \frac{V_{LED} \times (1 - D_{MAX})^2}{2\pi \times L \times I_{LED} \times D_{MAX}}$$

where f_{ZRHP} is in hertz, V_{LED} is in volts, L is the inductance value of L1 in henries (H), and I_{LED} is in amperes.

The switching converter small-signal transfer function also has an output pole for both boost and boost-buck configurations. The effective output impedance that determines the output pole frequency together with the output filter capacitance is calculated as:

Boost configuration:

$$R_{OUT} = \frac{(R_{LED} + R10) \times V_{LED}}{(R_{LED} + R10) \times I_{LED} + V_{LED}}$$

Boost-buck configuration:

$$R_{OUT} = \frac{(R_{LED} + R10) \times V_{LED}}{(R_{LED} + R10) \times I_{LED} \times D_{MAX} + V_{LED}}$$

where R_{LED} is the dynamic impedance (rate of change of voltage with current) of the LED string at the operating current, R10 is the LED current-sense resistor in ohms, V_{LED} is in volts, and I_{LED} is in amperes.

The output pole frequency for both boost and boost-buck configurations is calculated as follows:

$$f_{P2} = \frac{1}{2\pi \times C_{OUT} \times R_{OUT}}$$

where f_{P2} is in hertz, C_{OUT} is the output filter capacitance in farads, R_{OUT} is the effective output impedance in ohms calculated above.

Compensation components R7 and C7 perform two functions. C7 introduces a low-frequency pole that introduces a -20dB/decade slope into the loop gain. R7 flattens the gain of the error amplifier for frequencies above the zero formed by R7 and C7. For compensation, this zero is placed at the output pole frequency f_{P2} such that it provides a -20dB/decade slope for frequencies above f_{P2} for the complete loop gain.

The value of R7 needed to fix the total loop gain at f_{P2} such that the total loop gain crosses 0dB at -20dB/decade at one-fifth of the RHP zero can be calculated as follows:

$$R7 = \frac{f_{ZRHP} \times R8}{5 \times f_{P2} \times (1 - D_{MAX}) \times R10 \times 9.9 \times GM_{COMP}}$$

where R7 is the compensation resistor in ohms, f_{ZRHP} and f_{P2} are in hertz, R8 is the switch current-sense resistor in ohms, R10 is the LED current-sense resistor in ohms, factor 9.9 is the gain of the LED current amplifier, and GM_{COMP} is the transconductance of the error amplifier in Siemens.

The value of C7 can be calculated as:

$$C7 = \frac{1}{2\pi \times R7 \times f_{P2}}$$

where C7 is in farads, f_{P2} is in hertz, and R7 is in ohms.

To minimize switching frequency noise, an additional capacitor can be added in parallel with the series combination of R7 and C7. The pole from this capacitor and R7 must be a decade higher than the loop crossover frequency.

Short-Circuit Protection

Boost Configuration

In the boost configuration (Figure 2), if the LED string is shorted then the excess current flowing in the LED current-sense resistor will cause NDRV to stop switching. The input voltage will appear on the output capacitor, and this causes very high peak currents to flow in the LED current-sense resistor R10 because the dimming MOSFET (Q2) is on. Once the voltage across the LED current-sense resistor exceeds 300mV for more than 5µs, then the dimming MOSFET Q2 turns off and stays off for 4096 switching clock cycles. At the same time, NDRV is also off. The MAX16834 goes into the hiccup mode and recovers from hiccup once the short has been removed. The power dissipation in the dimming MOSFET (Q2) is minimized during a short across the LED string. During the same period, $\overline{FLT}$ only goes high when the dimming MOSFET is on.

Boost-Buck Configuration

In the case of the boost-buck configuration (Figure 3), once an LED string short occurs then the behavior is different. A short across the LED string causes a high current spike due to the external capacitors at the output. The regulation loop will cause NDRV to stop switching. This causes the voltage on HV to drop if its voltage is derived from LED+. The voltage on CLV will drop, and this drop is detected after 128 clock cycles. The dimming MOSFET and the switching MOSFET will stop switching. It stays off for 4096 clock cycles, and the cycle repeats itself. The short across the LED string will cause the MAX16834 to go into a hiccup mode. At the same time the $\overline{FLT}$ signal asserts itself for 4096 clock cycles every hiccup cycle. In the case where the HV voltage is derived from a source different than LED+, then the LED current will stay in regulation even during a short across the LED string. In this case, $\overline{FLT}$ does not assert itself during the short.

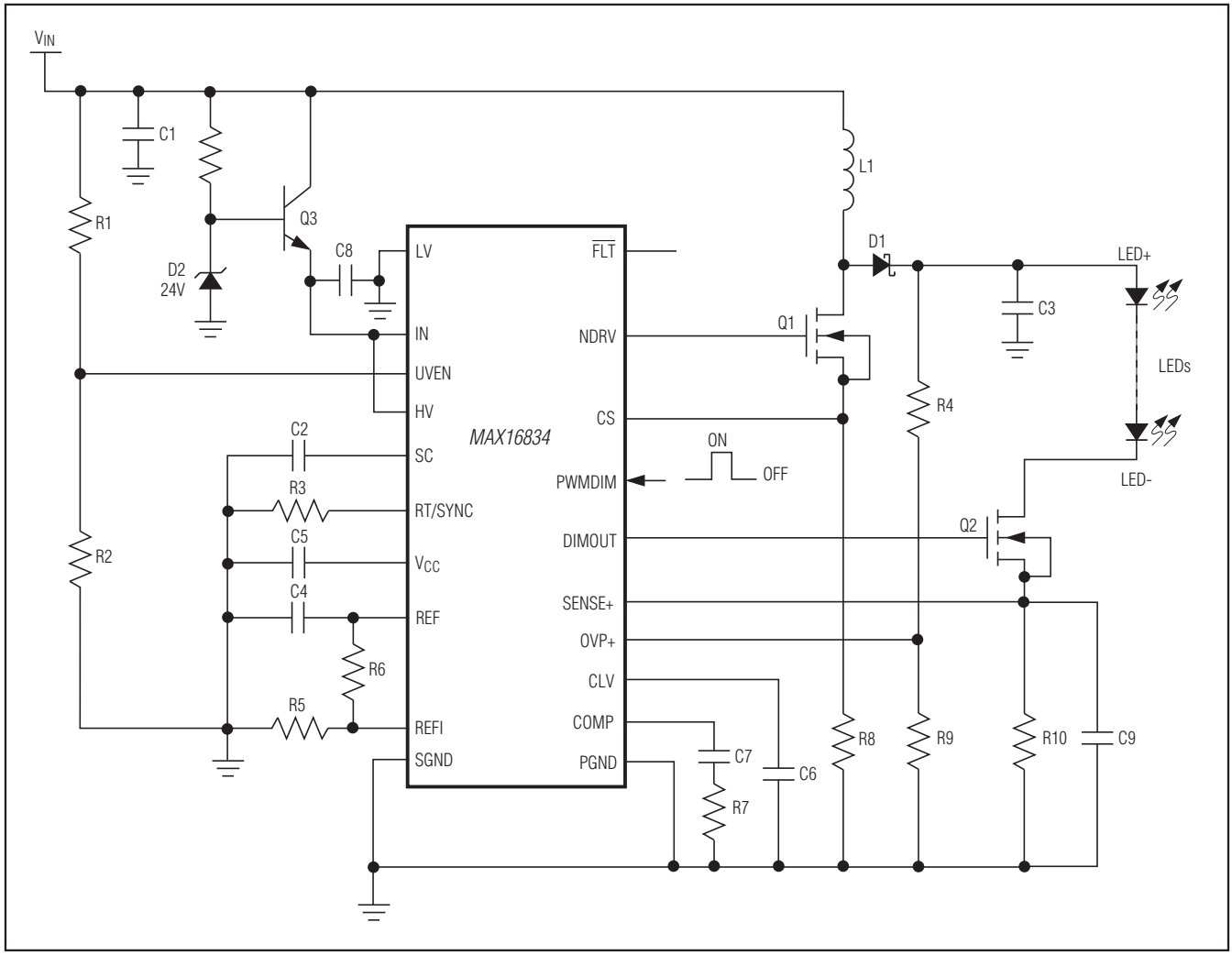


Figure 4. Boost LED Driver with Automotive Load Dump Protection

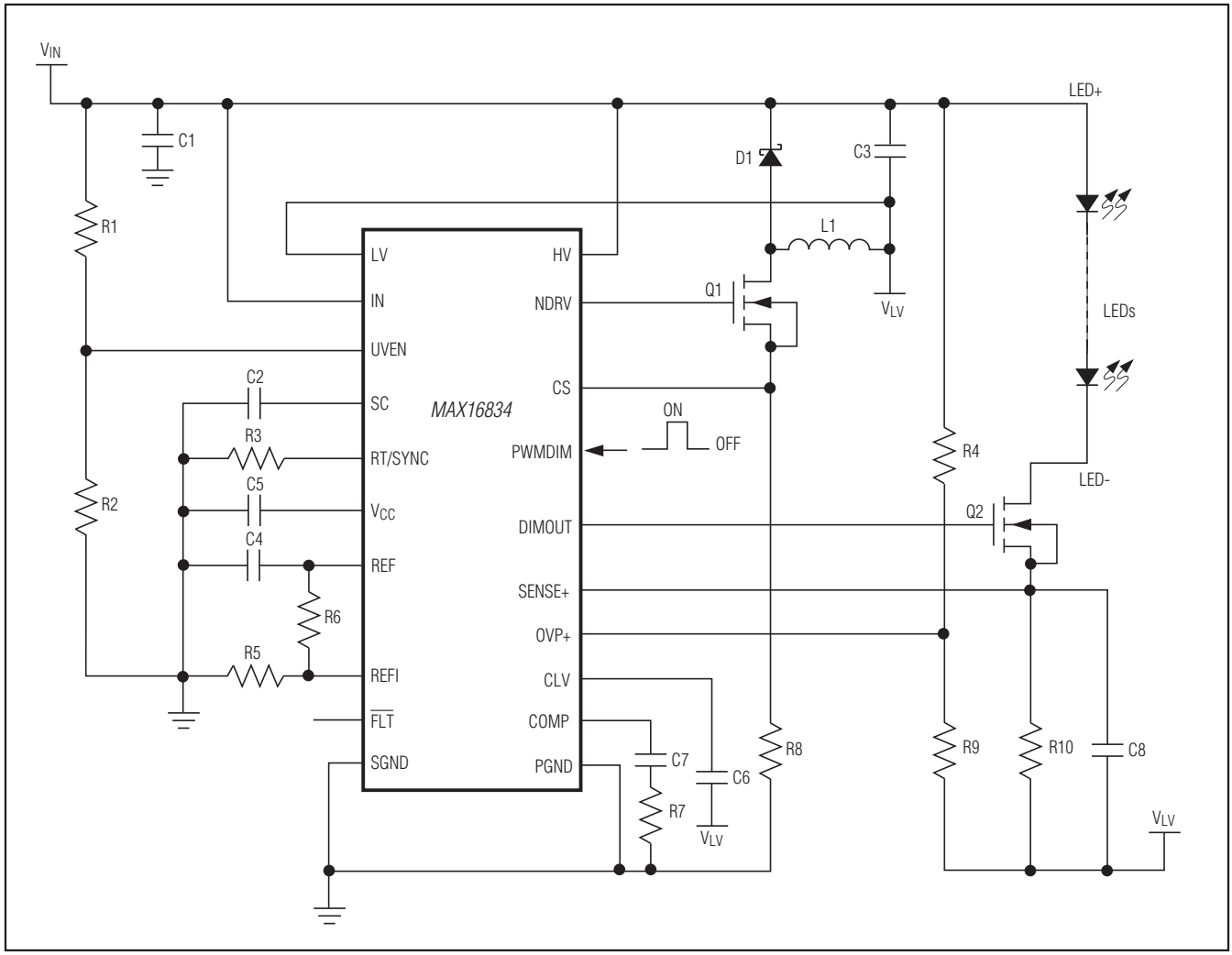


Figure 5. High-Side Buck LED Driver

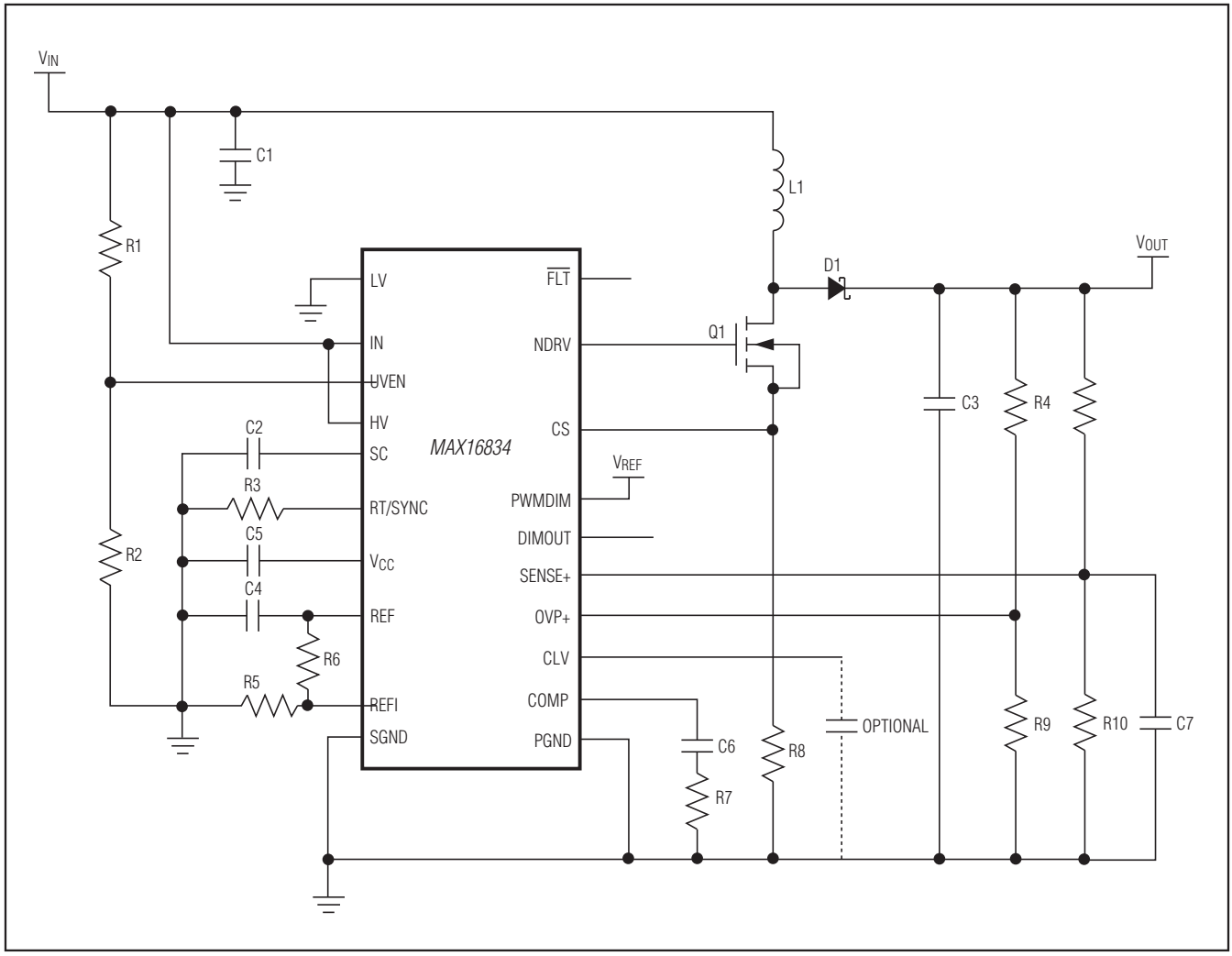


Figure 6. Boost DC-DC Converter

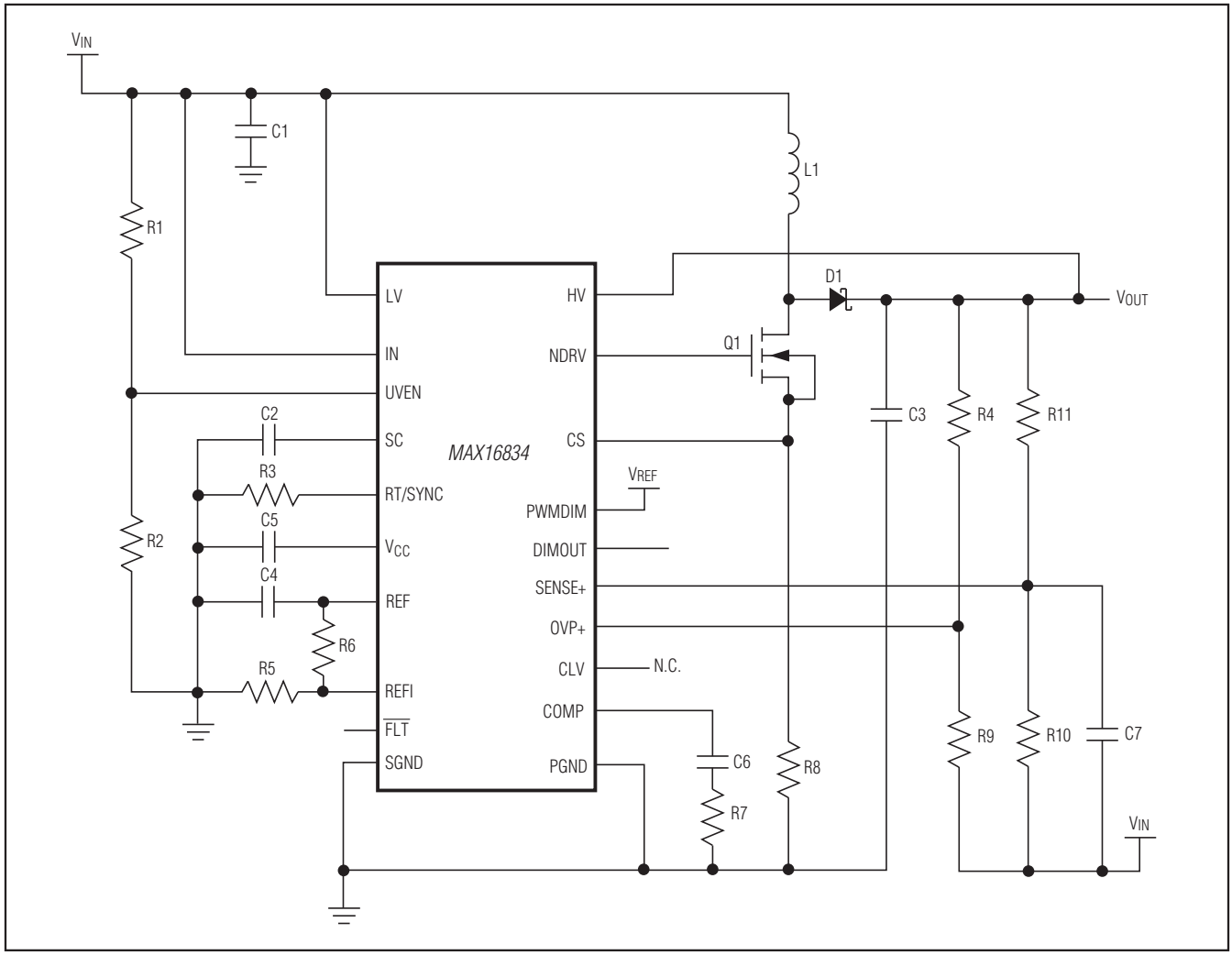


Figure 7. Boost-Buck DC-DC Converter

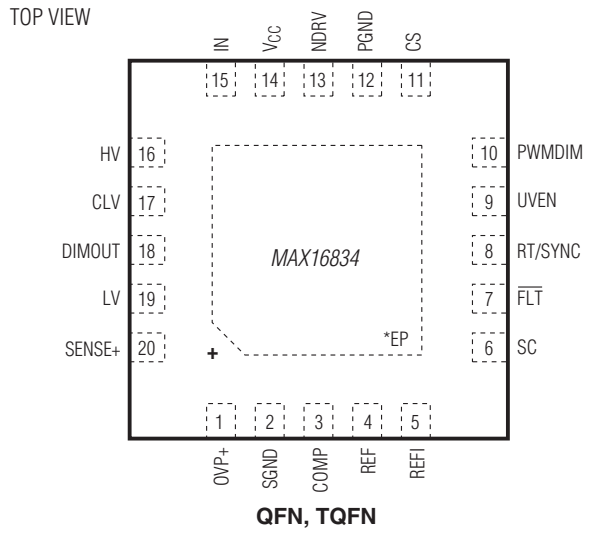
Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a dv/dt source; therefore, minimize the surface area of the heatsink as much as is compatible with the MOSFET power dissipation or shield it. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

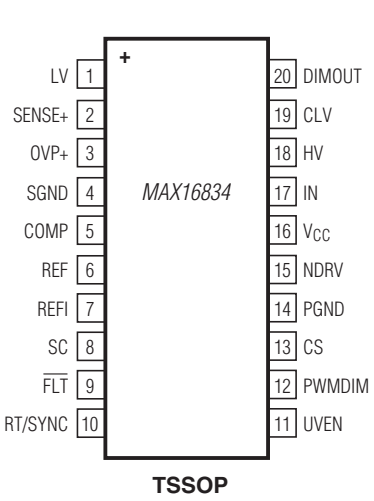
Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the MAX16834 package. Ensure that all heat-dissipating components have adequate cooling.
2) Isolate the power components and high-current path from the sensitive analog circuitry.
3) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short such that:
   a) The anode of D1 must be connected very close to the drain of the MOSFET Q1.
   b) The cathode of D1 must be connected very close to C_{OUT}.
   c) C_{OUT} and the current-sense resistor R8 must be connected directly to the ground plane.
4) Connect PGND and SGND to a star-point configuration.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
6) Route high-speed switching nodes away from the sensitive analog areas. Use an internal PCB layer for the PGND and SGND plane as an EMI shield to keep radiated noise away from the device, feedback dividers, and analog bypass capacitors.
7) To prevent discharge of the compensation capacitors during the off-time of the dimming cycle, ensure that the PCB area close to these components has extremely low leakage. Discharge of these capacitors due to leakage results in reduced performance of the dimming circuitry.

Pin Configurations



QFN, TQFN



TSSOP

*EP = EXPOSED PAD.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16834ATP+	-40°C to +125°C	20 TQFN-EP*
MAX16834ATP/V+	-40°C to +125°C	20 TQFN-EP*
MAX16834AUP+	-40°C to +125°C	20 TSSOP-EP*
MAX16834AUP/V+	-40°C to +125°C	20 TSSOP-EP*
MAX16834AGP/VY+	-40°C to +125°C	20 QFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
/V denotes an automotive qualified part.
/VY denotes an automotive qualified part in a "side wettable flank" package.

Chip Information

PROCESS: BiCMOS–DMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2044-3	21-0139	90-0037
20 TSSOP	U20E+1	21-0108	90-0114
20 QFN	G2044Y+1	21-0576	90-0360

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/08	Initial release	—
1	2/09	Added TSSOP package and automotive version. Also updated *Electrical Characteristics*, *Pin Description*, *Detailed Description*, and *LED Current-Sense Input (SENSE+)* section, *Pin Configuration* and *Package Information*	1, 2, 6, 7, 8, 9, 22
2	5/09	Added automotive version of TQFN package	1
3	1/10	Added requirement for a capacitor on the SENSE+ pin	2, 3, 4, 7, 9, 11, 13, 17–20
4	8/11	Added side wettable flank package	1, 6, 7, 22
5	1/15	Updated *Benefits and Features* section	1

