Ordering number:ENN*4144

CMOS IC

LC573104A, 573102A

4-bit Single Chip Microcontroller

Preliminary

Overview

LC573104A and LC573102A are CMOS 4-bit microcontrollers featuring low-voltage operation and low power dissipation.

Both LC573104A and LC573102A incorporate a 4-bit parallel processing ALU, 4K bytes/2K bytes ROM, a 64×4-bit RAM, a 16-bit timer, and an infrared remote control transmission carrier output circuit.

Applications

- Remote controller.
- Control of small measuring instruments.

Features

- ROM : 4096×8 bits (LC573104A)
  2048×8 bits (LC573102A)
- RAM : 64×4 bits
- Cycle time

Cycle time	System clock generator	Oscillation frequency	Supply voltage
17.6µs	Ceramic oscillation circuit	455kHz	2.3 to 6.0V

- Current Drain

a. At normal operation

Current drain	System clock generator	Oscillation frequency	Supply voltage
150µA typ	CR oscillation	455kHz	3.0V
400µA typ	CR oscillation	455kHz	5.0V

b. HALT mode

Current drain	System clock generator	Oscillation frequency	Supply voltage
80µA typ	CR oscillation	455kHz	3.0V
300µA typ	CR oscillation	455kHz	5.0V

c. HOLD mode

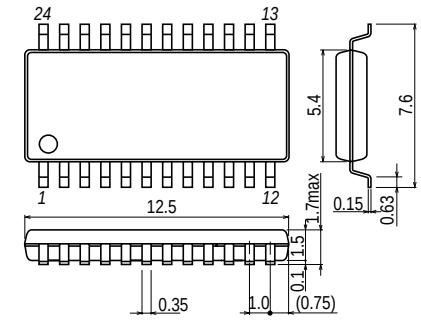
Leakage current	Condition	Oscillation frequency	Supply voltage
0.1µA typ	When CR oscillation is at STOP mode	455kHz	5.0V

Package Dimensions

unit:mm

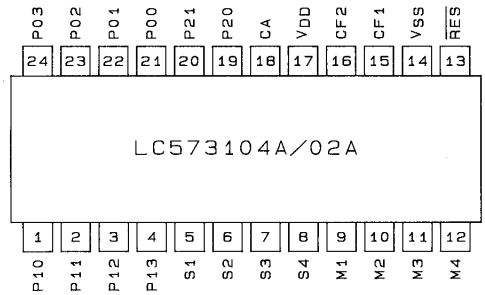
3112A-MFP24S

[LC573104A, 573102A]



SANYO : MFP24S

Pin Assignment



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■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges,or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

• Port
  · Input port (S port, M port) : 2-port (8 pins) [Key scan input port]
  · Input/Ouput port : 3-port (10 pins)
    P0 port, P1 port 2-port (8 pins) [Key scan output port]
    P2 port 1-port (2 pins) [Key scan expansion port]
    [LED direct drivable port]
• Infrared remote control carrier generation circuit.
  · Software-controllable remote control carrier output ON/OFF.
  · Software-controllable carrier frequency and duty ratio.
    <38kHz-1/3 duty, 38kHz-1/2 duty, 57kHz-1/2 duty>
    (When fixed carrier signal is output, it is specified by mask option)
  · 1kHz to 200kHz infrared remote control transmission carrier frequency.
    (When carrier output is selected by timer at mask option, and when 455kHz CR oscillator is used)
  · Infrared carrier output-dedicated terminal built-in (CA terminal).
  · 108ms HALT-mode cancel signal output.
• Timer
  · 16-bit software-controllable Timer
    Timer input clock : Ceramic (CR) oscillation frequency (455kHz).
  · 108ms HALT release request signal generation timer (Free running timer).
  · Watchdog timer (changed over between USED/UNUSED by mask option)
• Sub-routine stack level
  · 2 levels
• Oscillation circuit
  · Ceramic (CR) oscillation circuit : 455kHz (for System clock generation), Feedback resistor built-in.
• Standby function
  · HALT mode
    HALT mode used to reduce current drain.
    HALT mode suspends program execution.
    Following shows how to release the HALT mode.
    (A) System reset
    (B) HALT mode release request signal.
  · HOLD mode
    HOLD mode stops ceramic resonator (CR). The HOLD mold can be released in two ways.
    (A) System reset
    (B) Apply H level input to S port pin or M port pin. (However, it is necessary to set S port or M port HOLD mode release permission flag beforehand.)
• From of shipment
  · MFP-24S (1.0mm pitch) and chip.

NOTE : When dipping in solder to mount the MFP package on board, contact SANYO for instructions.

The Application Development System for the LC573100 Series.

(1) Manual
  (A) Users Manual : LC573100 Series Users Manual.
  (B) Development Tool Manual : LC573100 Series Development Tool Manual.

(2) Development Tools
- Tools for application development of the LC573100 Series.
  (A) Personal computer (MS-DOS based).
  (B) Cross assembler (LC573100.EXE).
  (C) Mask option generator (SU573100.EXE).
- Tools to evaluate application development of the LC573100 Series.
  (A) EVA chip (LC5797).

NOTE 1) As RAM capacity differs between EVA chip (LC5797) and the LC573100 Series, always check before programming and debugging.
  LC573100 : 64×4 bits
  LC5797 : 256×4 bits

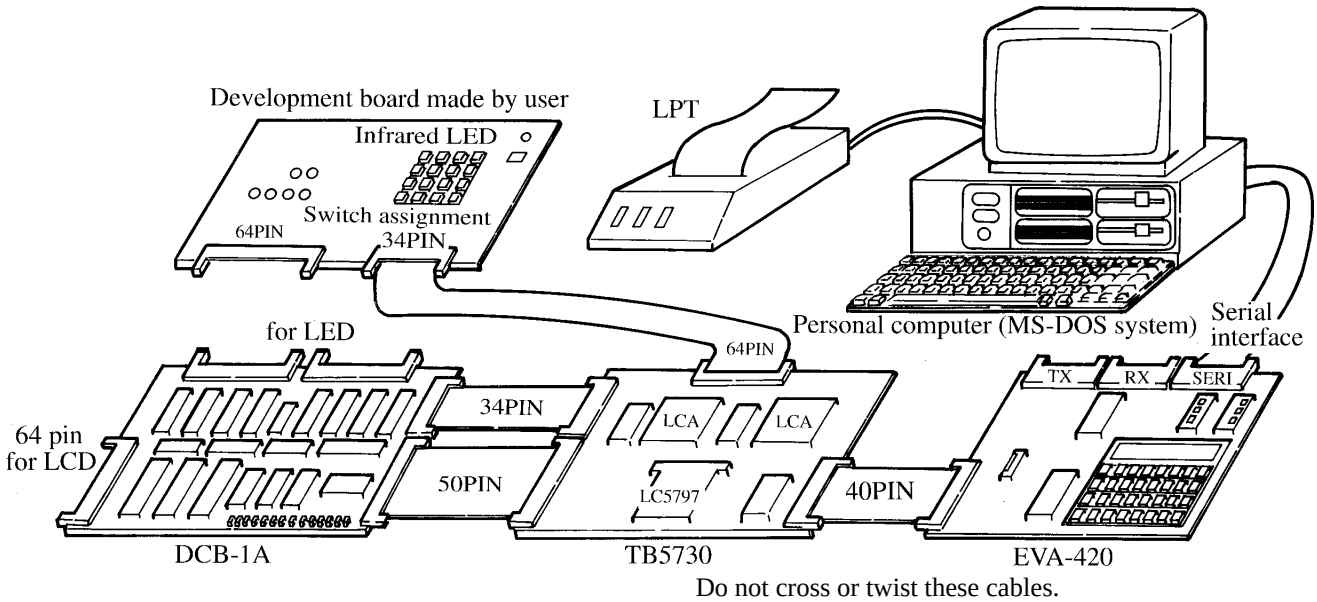
NOTE 2) Always keep the DPH value in mind when programming. Only DPH '0' to '3' may be used as the RAM address.
  If DPH other than '0' to '3' is used as RAM address when programming, SANYO will not be liable for any trouble caused.

  (B) EVA chip board (TB5730).

NOTE) The application evaluation board is the evaluation board made by the user.

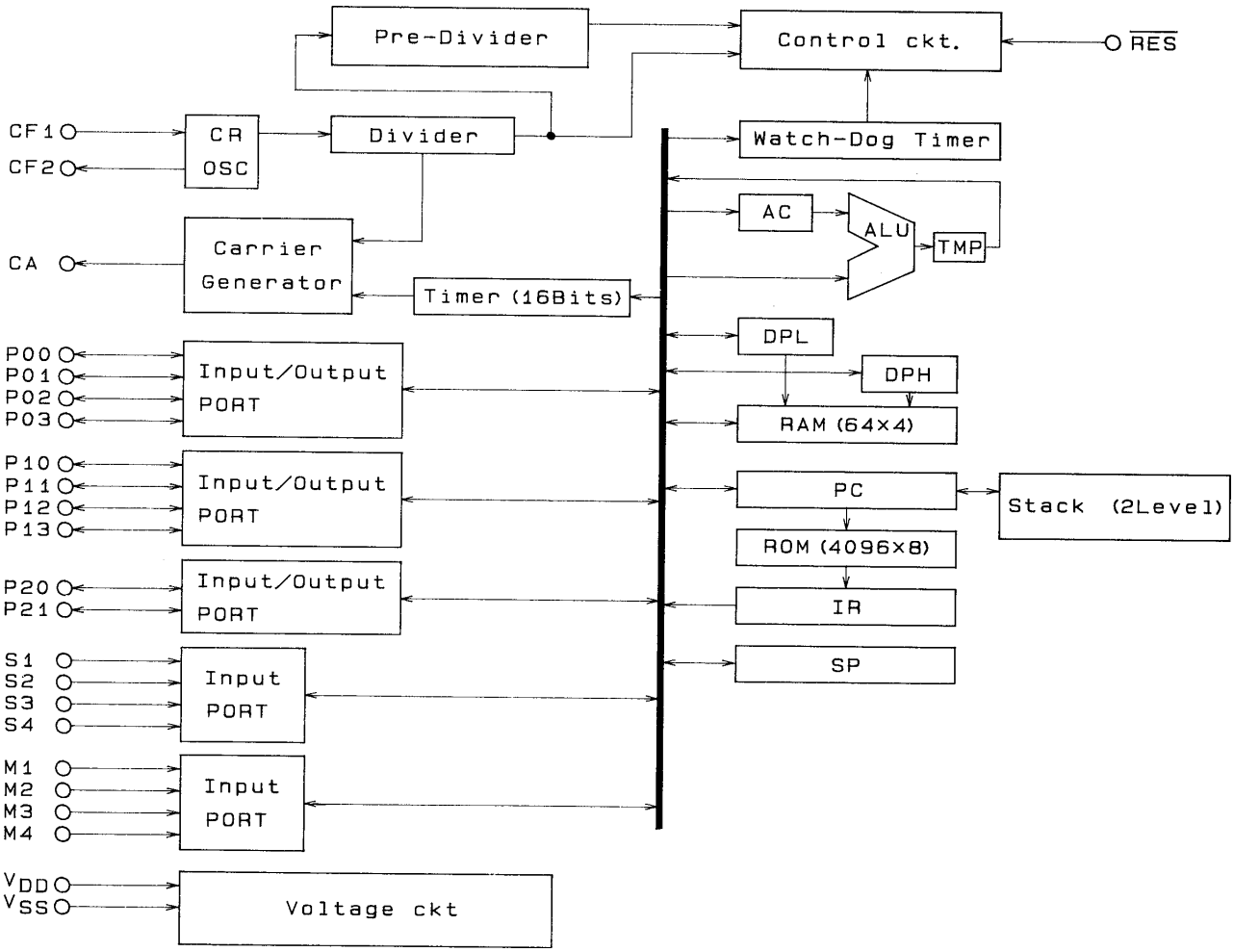
  (C) Evaluation board [EVA420 (Monitor ROM : ER-573000)]
  (D) Display and mask option data control board [DCB-1A (REV3.6)]

Development Support System Outline



(A) Block Diagram

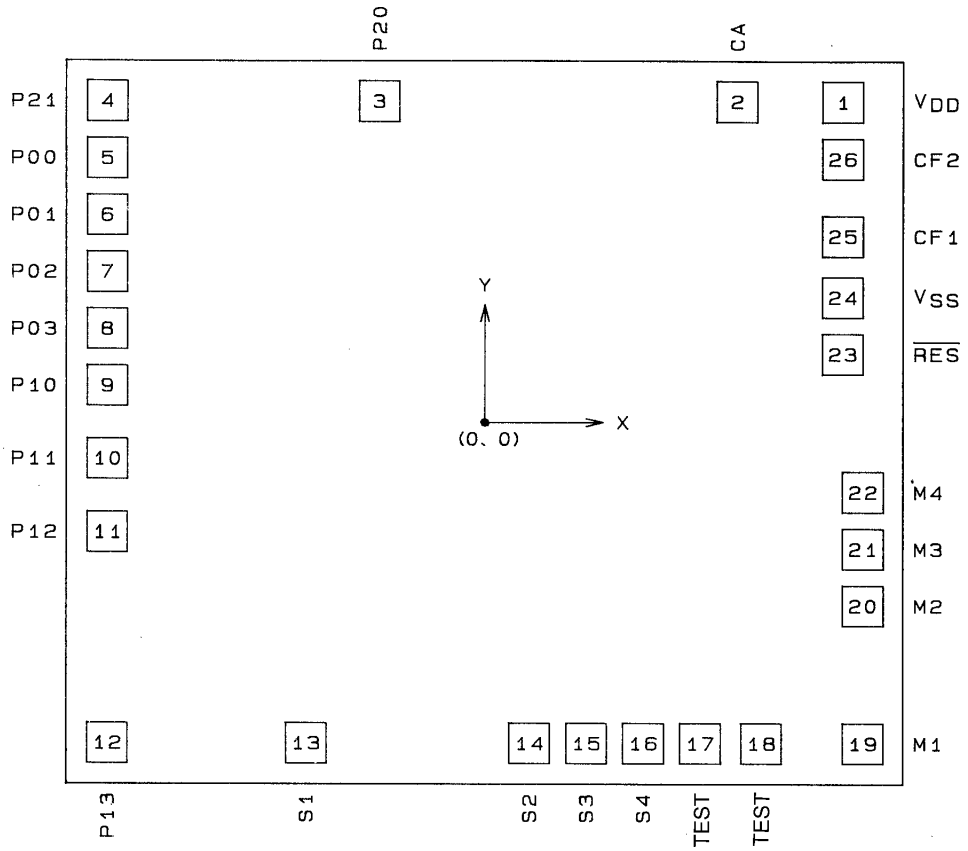
(LC573104A)



Die Specifications

Chip size : 3.51mm×3.19mm
Chip thickness : 480μm
Pad size : 120μm×120μm

Pad Layout



Pad coordinates

MFP24S pin assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)
17	1	V_{DD}	1465	1365
18	2	CA	1155	1365
19	3	P20	– 305	1365
20	4	P21	–1485	1365
21	5	P00	–1485	1110
22	6	P01	–1485	870
23	7	P02	–1485	565
24	8	P03	–1485	325
1	9	P10	–1485	20
2	10	P11	–1485	– 220
3	11	P12	–1485	– 480
4	12	P13	–1485	–1395
5	13	S1	– 410	–1395

MFP24S pin assignment				
	Pad No.	Pin Name	X (μm)	Y (μm)
6	14	S2	360	–1395
7	15	S3	560	–1395
8	16	S4	760	–1395
–	17	TEST	960	–1395
–	18	TEST	1140	–1395
9	19	M1	1560	–1395
10	20	M2	1560	– 905
11	21	M3	1560	– 685
12	22	M4	1560	– 445
13	23	$\overline{RES}$	1465	330
14	24	V_{SS}	1465	570
15	25	CF1	1465	755
16	26	CF2	1465	1155

- The chip center is the origin of the above pad coordinates.
  The X, Y values represent the coordinate of the pad center.
- When dipping the MFP24S package in solder to mount on boards, contact SANYO for instructions, etc.
- Chip substrate should be connected to V_{SS} or left open.

Pin Function

MFP24S Pin No.	Pin name	Input/ Output	Function description	Option	Reset status
17	V_{DD}	–	Supply voltage. See Fig 1.		
14	V_{SS}	–	Ground. See Fig 1.		
15	CF1	Input	User for system clock oscillation. • 455kHz ceramic resonator is connected between CF1 and CF2 for oscillation. • Stops oscillation when receiving CR oscillation stop command.		
16	CF2	Output			
5 6 7 8	S1 S2 S3 S4	Input	Input port S. • LSI system is reset by charging VDD to S1 to S4 simultaneously (Mask option). • Data is loaded in accumulator.	(1) 'L' level HOLD Tr YES/NO (2) Reset by S1 to S4.	• Pull-down resistor ON. • Reset signal ENABLE.
9 10 11 12	M1 M2 M3 M4	Input	Input port M. Data loaded in accumulator.	'L' level HOLD Tr YES/NO	• Pull-down resistor ON.
21 22 23 24	P00 P01 P02 P03	Input/ Output	Input/output port. • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch Open Drain Output)		
1 2 3 4	P10 P11 P12 P13	Input/ Output	Input/output port. • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch Open Drain Output)		
19 20	P20 P21	Input/ Output	Input/output port. • Data loaded in accumulator. • Output pin to output data from accumulator. (P-ch Open Drain Output) • LED direct drivable pin.		
18	CA	Output	Remote control carrier output.	Fixed carrier output/ Carrier output by timer	• At reset 'L' level. • At fixed carrier output 38kHz-1/3 duty.
13	$\overline{RES}$	Input	Reset input. Internal pull-up resistor.		

Supply connections

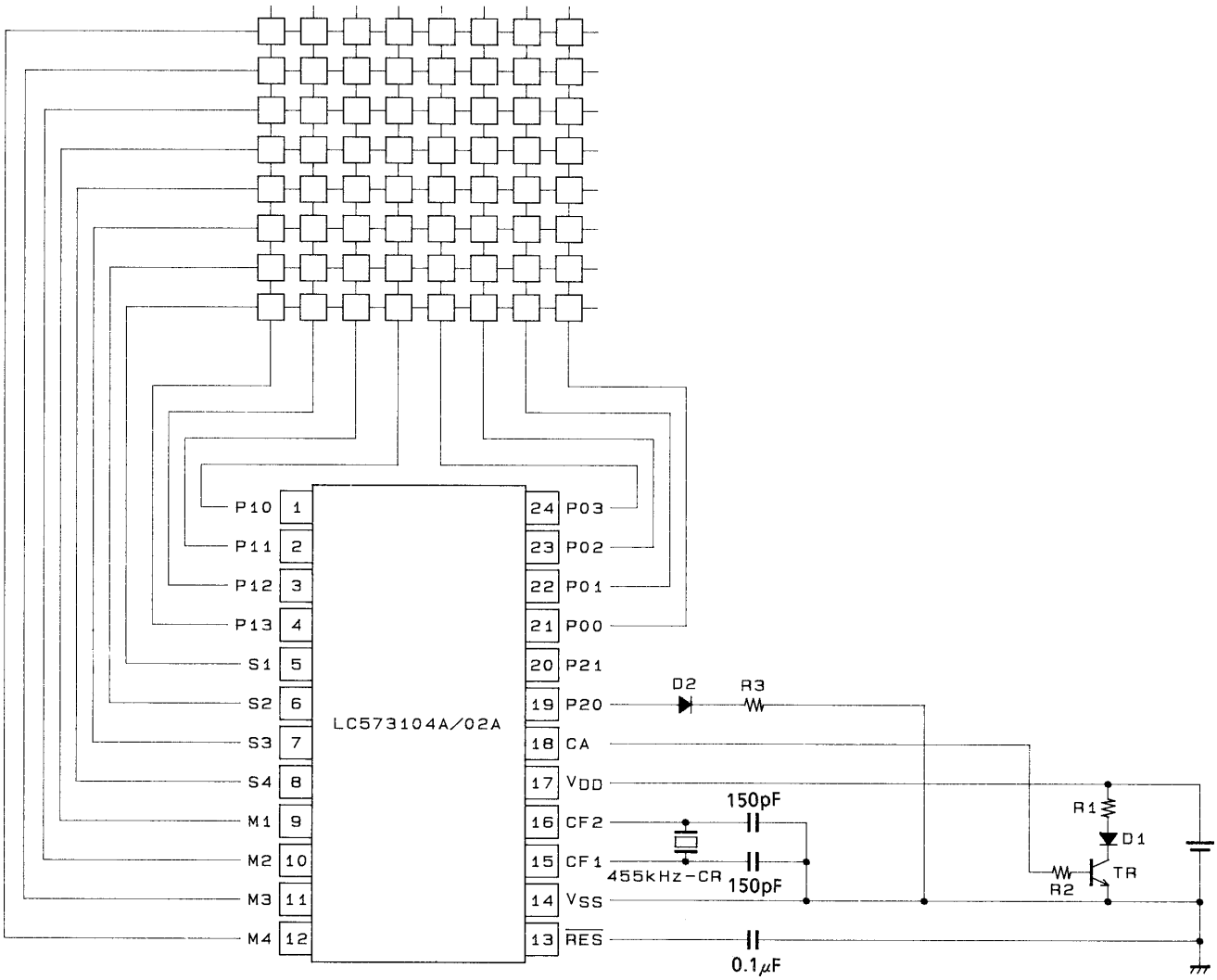
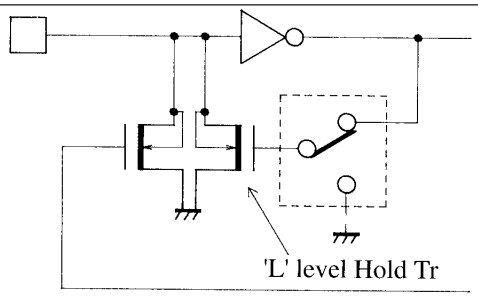


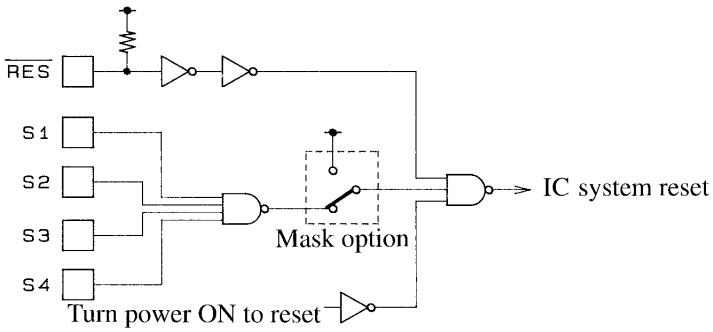
Fig. 1 Supply connections

Mask Option

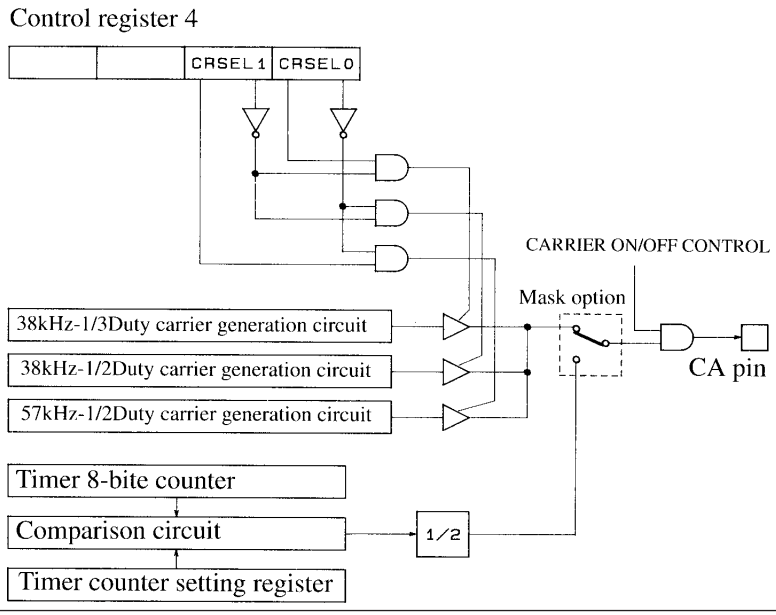
(1) Input port option

Option	Circuit	Remarks
'L' level Hold Tr selection		Next port switches over in sequence. • S1 to S4, M1 to M4 Input signal level Hold Tr selection • 'L' level Hold Tr used. • 'L' level Hold Tr not used.

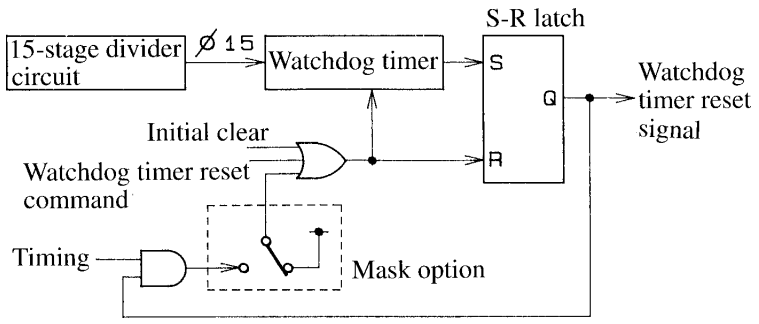
(2) Reset signal option by S port

Option	Circuit	Remarks
Resetting IC by S port		Selects signal for resetting IC system by simultaneously charging 'H' level to S1 to S4. • Allow • Prohibit

(3) Carrier standard clock generation circuit option for remote control

Option	Circuit	Remarks
38/57kHz		Software-controllable carrier frequency and duty. • Following carrier frequency and duty may be selected by setting control register 4. (1) 38kHz-1/3 Duty (2) 38kHz-1/2 Duty (3) 57kHz-1/2 Duty
Timer 8 bit overflow		Timer 8-bit overflow signal generates carrier signal for infrared remote control.

(4) Watchdog timer circuit option

Option	Circuit	Remarks
Watchdog timer selection		Watchdog timer used/unused selection

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
	V_{DD1}		–0.3 to V_{DD}	V
	V_{DD2}		–0.3 to V_{DD}	V
Input voltage	V_{IN}	S1 to S4, M1 to M4, $\overline{RES}$, P00 to P03, P10 to P13, P20, P21, CF1 (P00 to P03, P10 to P13, P20, P21 are input mode)	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	CA, P00 to P03, P10 to P13, P20, P21, CF2 (P00 to P03, P10 to P13, P20, P21 are output mode)	–0.3 to V_{DD}+0.3	V
Output current (Per 1 pin)	I_{OUT1}	CA (per 1 pin)	25	mA
	I_{OUT2}	P00 to P03, P10 to P13 (per 1 pin)	500	µA
	I_{OUT3}	P20, P21 (Per 1 pin)	10	mA
	I_{OUT4}	Output pins other than listed above (per 1 pin)	500	µA
Total output current of all pins except CA	I_{ALL}	All pins totaled (except for CA pin)	25	mA
Operating temperature	Topr		–30 to +70	˚C
Storage temperature	Tstg		–40 to +125	˚C

Recommended Operating Ranges at Ta =–30 to +70˚C, V_{SS}=0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		2.3		6.0	V
Input high-level voltage	V_{IH1}	S1 to S4, M1 to M4, P00 to P03, P10 to P13, P20, P21 (P0, P1, P2 ports are input mode)	$0.7V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL1}		0		$0.3V_{DD}$	V
Input high-level voltage	V_{IH2}	$\overline{RES}$	$0.75V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL2}		0		$0.25V_{DD}$	V
Operation frequency	f_{OPG}	At CR oscillation, Fig. 2	380	455	500	kHz

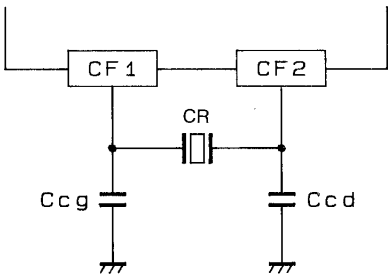


Fig. 2 CR Oscillation Circuit

Electrical Characteristics at Ta =–30 to +70˚C, V_{SS}=0V

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Input impedance	$R_{IN}1A$	V_{DD}=2.9V, V_{IL}=0.4V, S1 to S4, M1 to M4, 'L' level Hold Tr, Fig. 3		150	300	1000	kΩ
	$R_{IN}1B$	V_{DD}=2.9V, V_{IL}=0.4V, S1 to S4, M1 to M4, 'L' level pull-down Tr, Fig. 3		30	50	100	kΩ
	$R_{IN}2$	V_{DD}=2.9V, $\overline{RES}$		10		300	kΩ
Output high-level voltage	$V_{OH}1$	V_{DD}=2.9V, I_{OH}=–450µA, P00 to P03, P10 to P13		V_{DD}–0.45			V
Output off-leak current	$\|I_{OFF}\|$	V_{DD}=2.9V, P00 to P03, P10 to P13	$V_{IN}=V_{SS}$			1.0	µA
	$\|I_{OFF}\|$		$V_{IN}=V_{DD}$	–1.0			µA
Output high-level voltage	$V_{OH}2$	V_{DD}=2.9V, I_{OH}=–10mA, P20, P21		V_{DD}–0.5			V
Output off-leak current	$\|I_{OFF}\|$	V_{DD}=2.9V, P20, P21	$V_{IN}=V_{SS}$			1.0	µA
	$\|I_{OFF}\|$		$V_{IN}=V_{DD}$	–1.0			µA
Output current (H)	$I_{OH}1$	V_{DD}=3.0V, $V_{OH}=V_{DD}$–1.5V, CA		6	12		mA
Output current (L)	$I_{OL}1$	V_{DD}=3.0V, V_{OH}=0.9V, CA		2	5		mA
HALT-mode supply current	$I_{DD}1$	V_{DD}=3.0V, 455kHz CR oscillation, Ccd=Ccg=150pF, Ta≤50°C, Fig.5			80	300	µA
Operating current	$I_{DD}2$	V_{DD}=3.0V, 455=kHz CR oscillation, Ccd=Ccg=150pF, Ta≤50°C, Fig.5			150	500	µA
Supply leak current 1	$I_{LEAK}1$	V_{DD}=3.0V	Ta=25°C		0.2	1	µA
Supply leak current 2	$I_{LEAK}2$		Ta=50°C		1	5	µA
Oscillator start-up voltage	V_{ST}	Ccd=Ccg=150pF, 455kHz CR oscillation, Fig. 4				2.3	V
Oscillator sustaining voltage	V_{SUS}			2.0			V
Oscillator start-up time	t_{ST}	V_{DD}=2.3V, Ccd=Ccg=150pF, 455kHz CR oscillation, Fig. 4				30	ms

Recommended Oscillators.

Oscillator	Manufacturer	Part number	Ccg	Ccd
455kHz ceramic oscillator	Kyocera	KBR-455BK/Y	150pF	150pF
	Murata	CSB455E	150pF	150pF
	Fuji Ceramics	POE-455	150pF	150pF

Electrical Characteristics at Ta =–30 to +70˚C, V_{SS}=0V

Parameter	Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Input impedance	$R_{IN}1A$	V_{DD}=5.0V, V_{IL}=0.4V, S1 to S4, M1 to M4, 'L' level Hold Tr, Fig. 3		70	200	600	kΩ
	$R_{IN}1B$	V_{DD}=5.0V, S1 to S4, M1 to M4, 'L' level pull-down Tr, Fig. 3		30	50	100	kΩ
	$R_{IN}2$	V_{DD}=5.0V, $\overline{RES}$		10		300	kΩ
Output high-level voltage	$V_{OH}1$	V_{DD}=5.0V, I_{OH}=–750µA, P00 to P03, P10 to P13		V_{DD}–0.75			V
Output off-leak current	$\|I_{OFF}\|$	V_{DD}=5.0V, P00 to P03, P10 to P13	$V_{IN}=V_{SS}$			1.0	µA
	$\|I_{OFF}\|$		$V_{IN}=V_{DD}$	–1.0			µA
Output high-level voltage	$V_{OH}2$	V_{DD}=5.0V, I_{OH}=–10mA, P20, P21		V_{DD}–0.5			V
Output off-leak current	$\|I_{OFF}\|$	V_{DD}=5.0V, P20, P21	$V_{IN}=V_{SS}$			1.0	µA
	$\|I_{OFF}\|$		$V_{IN}=V_{DD}$	–1.0			µA
Output current (H)	$I_{OH}1$	V_{DD}=5.0V, $V_{OH}=V_{DD}$–2.5V, CA		10	20		mA
Output current (L)	$I_{OL}1$	V_{DD}=5.0V, V_{OL}=0.9V, CA		2	5		mA
HALT-mode supply current	$I_{DD}1$	V_{DD}=5.0V, 455kHz CR oscillation, Ccd=Ccg=150pF, Ta≤50°C, Fig.5			300	400	µA
Operating current	$I_{DD}2$	V_{DD}=5.0V, 455kHz CR oscillation, Ccd=Ccg=150pF, Ta≤50°C, Fig.5			400	500	µA
Supply leak current 1	$I_{LEAK}1$	V_{DD}=5.0V	Ta=25°C		0.2	1	µA
Supply leak current 2	$I_{LEAK}2$		Ta=50°C		1	5	µA
Oscillator start-up voltage	V_{ST}	Ccd=Ccg=150pF, 455kHz CR oscillation, Fig. 4				2.3	V
Oscillator sustaining voltage	V_{SUS}			2.0			V
Oscillator start-up time	t_{ST}	V_{DD}=2.3V, Ccd=Ccg=150pF, 455kHz CR oscillation, Fig. 4				30	ms

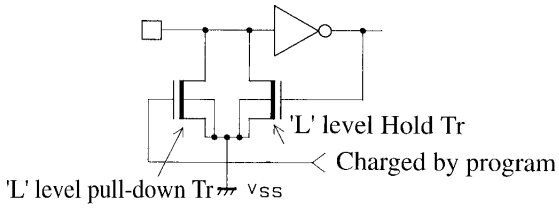


Fig. 3 : S1 to S4, M1 to M4 input structure

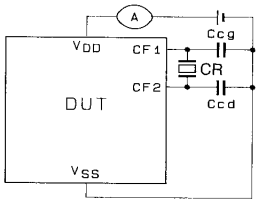


Fig. 5 : Supply current measuring circuit

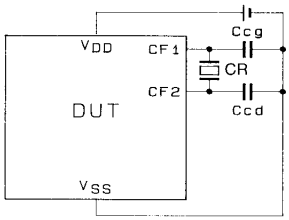


Fig. 4 : Oscillator start-up voltage, Oscillator sustaining voltage, and Oscillator start-up time measuring circuit.

Note : CR is 455kHz, S-PORT : M-PORT : Input lead Tr is ON.
$\overline{\text{RES}}$ terminal has resistor built-in and is OPEN.
I/O-PORT is set at Output Mode and data is 'H'.

LC573100 Series Instruction Set

The instruction set uses the following abbreviations and symbols.

AC	: Accumulator	M	: Memory
ACn	: Accumulator bit n	M (DP)	: Memory addressed by DP
CF	: Carry flag	[M (DP)]	: Contents of memory addressed by DP
DP	: Data pointer	PC	: Program counter
DPL	: Data pointer low nibble	PCn	: Program counter bit n
DPH	: Data pointer high nibble	PAGE	: Page latch
EDP	: Data pointer save register	STSn	: Status register n
EDPL	: Data pointer save register low nibble	(STSm)	: Status register n content
EDPH	: Data pointer save register high nibble	[P ( )]	: Contents of port ( )
SP	: Strobe pointer	X	: Immediate data
TREG	: Temporary register	Xn	: Immediate data bit n
SCFn	: Start conditioning flag n	PDF	: Input port pull-down flag
CTLn	: Control register n	SFR	: Special function register
HEFn	: Hold enable flag n	(SFR)	: Contents of special function register
ROM	: ROM data	CSTF	: Chrono start flag
CFCF	: Ceramic resonator oscillator control flag	SPC	: Strobe pointer control bit
( )	: Contents	$\overline{\text{CCF}}$	: Carrier output control flag
[ ]	: Contents	$\overline{( )}$	: Complement of contents
$\vee$	: Logical OR	$\overline{[ ]}$	: Complement of contents
$\veebar$	: Logical exclusive-OR	ϕ n	: Output from stage n of 15-stage divider
$\wedge$	: Logical AND	WDT	: Watchdog timer
$\leftarrow$	: Transfer direction, result		

• The special function registers are abbreviated as follows.

TCON	: Timer control register
TLOW	: Timer/counter register low byte
THIGH	: Timer/counter register high byte
CTL4	: Control register 4
P0	: Port P0
P1	: Port P1
P2	: Port P2

LC573100 Series Instructions

Instruction	Mnemonic	Instruction code	Function	Bytes	Cycles	Function description	Status flag affected
Accumulator	TAAT	0 0 0 0 0 0 0 1	AC, TRGE ← ROM	1	2	Contents of ROM on current page, addressed by PC whose low-orderd 8 bits are replaced with contents of AC and M (DP), are loaded to AC and TREG	
	MTR	0 0 0 1 0 0 1 0	M (DP) ← TREG	1	1	Stores the conternts of TREG memory location pointed to by DP.	
	ASR0	0 0 0 1 1 0 0 0	$AC_n \leftarrow AC_{n+1}$, $AC_3 \leftarrow 0$	1	1	Shifts the contents of the AC right and enter 0 into the MSB.	
	ASR1	0 0 0 1 1 0 0 1	$AC_n \leftarrow AC_{n+1}$, $AC_3 \leftarrow 1$	1	1	Shifts the contents of the AC right and enter 1 into the MSB.	
	ASL0	0 0 0 1 1 0 1 0	$AC_n \leftarrow AC_{n-1}$, $AC_0 \leftarrow 0$	1	1	Shifts the contents of the AC left and enter 0 into the LSB.	
	ASL1	0 0 0 1 1 0 1 1	$AC_n \leftarrow AC_{n-1}$, $AC_0 \leftarrow 1$	1	1	Shifts the contents of the AC left and enter 1 into the LSB.	
	INC	1 0 0 1 1 0 0 0	AC, M (DP) ← M (DP)+1	1	1	Memory M (DP) contents incremented +1, and loaded to AC and M (DP).	
	DEC	1 0 0 1 1 0 0 1	AC, M (DP) ← M (DP)–1	1	1	Memory M (DP) contents decremented –1, and loaded to AC and M (DP).	
Arithmetic	ADC	1 0 0 0 0 0 0 0	AC ← (AC)+[M (DP)]+CF	1	1	AC, memory M (DP) and CF contents are binary-added and the result loaded to AC.	CF
	ADC*	1 0 0 0 1 0 0 0	AC, M (DP) ← (AC)+[M (DP)]+CF	1	1	AC, memory M (DP) and CF contents are binary-added and the result loaded to AC, M (DP).	CF
	ADCI X	1 0 0 1 0 0 0 0 – – – – $X_3X_2X_1X_0$	AC ← (AC)+X+CF	2	2	AC, immediate data and CF contents are binary-added, and the result loaded to AC.	CF
	SBC	1 0 0 0 0 0 0 1	AC ← (AC)+$\overline{[M\ (DP)]}$+CF	1	1	AC, memory M (DP) and CF contents are binary-subtracted, and the result loaded to AC.	CF
	SBC*	1 0 0 0 1 0 0 1	AC, M (DP) ← (AC)+$\overline{[M\ (DP)]}$+CF	1	1	AC, memory M (DP) and CF contents are binary-subtracted, and the result loaded to AC and M (DP).	CF
	SBCI X	1 0 0 1 0 0 0 1 – – – – $X_3X_2X_1X_0$	AC ← (AC)+$\overline{X}$+CF	2	2	AC, immediate data and CF contents are binary-subtracted and the result loaded to AC.	CF
	ADD	1 0 0 0 0 0 1 0	AC ← (AC)+[M (DP)]	1	1	AC and memory M (DP) contents are binary-added and the result loaded to AC.	CF
	ADD*	1 0 0 0 1 0 1 0	AC, M (DP) ← (AC)+[M (DP)]	1	1	AC and memory M (DP) contents are binary-added and the result loaded to AC and M (DP).	CF
	ADDI X	1 0 0 1 0 0 1 0 – – – – $X_3X_2X_1X_0$	AC ← (AC)+X	2	2	AC and immediate data contents are binary-added and the result loaded to AC.	CF
	SUB	1 0 0 0 0 0 1 1	AC ← (AC)+$\overline{[M\ (DP)]}$+1	1	1	AC and memory M (DP) contents are binary-subtracted and the result loaded to AC.	CF
	SUB*	1 0 0 0 1 0 1 1	AC, M (DP) ← (AC)+$\overline{[M\ (DP)]}$+1	1	1	AC and memory M (DP) contents are binary-subtracted and the result loaded to AC and M (DP).	CF
	SUBI X	1 0 0 1 0 0 1 1 – – – – $X_3X_2X_1X_0$	AC ← (AC)+$\overline{X}$+1	2	2	AC and immediate data contents are binary-subtracted and the result loaded in AC.	CF
	ADN	1 0 0 0 0 1 0 0	AC ← (AC)+[M (DP)]	1	1	AC and memory M (DP) contents are binary-added and the result loaded to AC.	
	ADN*	1 0 0 0 1 1 0 0	AC, M (DP) ← (AC)+[M (DP)]	1	1	AC and memory M (DP) contents are binary-added and the result loaded to AC and M (DP).	
	ADNI X	1 0 0 1 0 1 0 0 – – – – $X_3X_2X_1X_0$	AC ← (AC)+X	2	2	AC and immediate data contents are binary-added and the result loaded in AC.	
Logical	AND	1 0 0 0 0 1 0 1	AC ← (AC)∧[M (DP)]	1	1	AC and memory M (DP) contents are ANDed and the result loaded to AC.	
	AND*	1 0 0 0 1 1 0 1	AC, M (DP) ← (AC)∧[M (DP)]	1	1	AC and memory M (DP) contents are ANDed and the result loaded to AC and M (DP).	
	ANDI X	1 0 0 1 0 1 0 1 – – – – $X_3X_2X_1X_0$	AC ← (AC)∧X	2	2	AC and immediate data contents are ANDed and the result loaded to AC.	
	EOR	1 0 0 0 0 1 1 0	AC ← (AC) ⩛ [M (DP)]	1	1	AC and memory M (DP) are exclusive ORed and the result loaded to AC.	
	EOR*	1 0 0 0 1 1 1 0	AC, M (DP) ← (AC) ⩛ [M (DP)]	1	1	AC and memory M (DP) are exclusive ORed, and the result loaded to AC and M (DP).	
	EORI X	1 0 0 1 0 1 1 0 – – – – $X_3X_2X_1X_0$	AC ← (AC) ⩛ X	2	2	AC and immediate data are exclusive ORed and the result loaded to AC.	
	OR	1 0 0 0 0 1 1 1	AC ← (AC) ∨ [M (DP)]	1	1	AC and memory M (DP) are ORed and the result loaded to AC.	
	OR*	1 0 0 0 1 1 1 1	AC, M (DP) ← (AC) ∨ [M (DP)]	1	1	AC and memory M (DP) are ORed and the result loaded to AC and M (DP).	
	ORI X	1 0 0 1 0 1 1 1 – – – – $X_3X_2X_1X_0$	AC ← (AC) ∨ X	2	2	AC and immediate data are ORed and the result loaded to AC.	

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Instruction	Mnemonic	Instruction code	Function	Bytes	Cycles	Function description	Status flag affected
Data Pointer	SDPL	0 0 0 1 1 1 0 0	DPL ← (AC)	1	1	AC contents loaded to DPL.	
	SDPH	0 0 0 1 1 1 0 1	DPH ← (AC)	1	1	AC contents loaded to DPH.	
	LDPL	1 1 1 1 1 1 0 1	AC ← (DPL)	1	1	DPL contents loaded to AC.	
	LDPH	1 1 1 1 1 1 1 0	AC ← (DPH)	1	1	DPH contents loaded to AC.	
	MDPL X	1 0 1 1 $X_3X_2X_1X_0$	DPL ← X	1	1	Immediate data X loaded to DPL.	
	MDPH X	1 1 0 0 $X_3X_2X_1X_0$	DPH ← X	1	1	Immediate data X loaded to DPH.	
	EDPL	0 0 0 1 1 1 1 0	(DPL) ↔ (EDPL)	1	1	DPL and EDPL contents exchanged.	
	EDPH	0 0 0 1 1 1 1 1	(DPH) ↔ (EDPH)	1	1	DPH and EDPH contents exchanged.	
	IDPL	1 0 0 1 1 0 1 0	DPL ← (DPL)+1	1	1	DPL contents incremented +1.	
	IDPH	1 0 0 1 1 1 0 0	DPH ← (DPH)+1	1	1	DPH contents incremented +1.	
	DDPL	1 0 0 1 1 0 1 1	DPL ← (DPL)–1	1	1	DPL contents decremented –1.	
	DDPH	1 0 0 1 1 1 0 1	DPH ← (DPH)–1	1	1	DPH contents decremented –1.	
SP	SSP	1 0 1 0 1 1 1 0	SP ← (AC)	1	1	AC contents loaded to SP.	
	LSP	1 0 1 0 1 0 1 0	AC ← (SP)	1	1	SP contents loaded to AC.	
	MSP X	1 1 1 0 $X_3X_2X_1X_0$	SP ← X	1	1	Immediate data X loaded to SP.	
	ISP	1 0 0 1 1 1 1 0	SP ← (SP)+1	1	1	SP contents incremented +1.	
	DSP	1 0 0 1 1 1 1 1	SP ← (SP)–1	1	1	SP contents decremented –1.	
Flag	LHLT	1 0 1 0 1 0 1 1	AC ← (STS2), STS2 ← 0	1	1	STS2 contents loaded to AC and STS2 is reset.	SCF1 to SCF4
	L500	1 0 1 0 1 1 0 0	AC ← (STS1), SCF0 ← 0	1	1	STS1 contents loaded to AC and SCF0 is reset.	SCF0
	CSP	0 0 0 0 0 1 0 0	CSTF ← 0	1	1	CSTF reset.	CSTF
	CST	0 0 0 0 0 1 0 1	CSTF ← 1	1	1	CSTF set.	CSTF
	RC5	0 0 0 0 0 1 1 0	HEF0 ← 0	1	1	HEF0 reset to inhibit Halt mode release by overflow from the divider circuit.	HEF0
	SC5	0 0 0 0 0 1 1 1	HEF0 ← 1	1	1	HEF0 set enabling overflow from the divider circuit to release the Halt mode.	HEF0
	RCF	1 1 1 1 0 0 0 0	CF ← 0	1	1	CF reset.	CF
	SCF	1 1 1 1 0 0 0 1	CF ← 1	1	1	CF set.	CF
Data transfer	LDA	1 0 1 0 1 0 0 1	AC ← [M (DP)]	1	1	Memory M (DP) contents transferred to AC.	
	STA	1 0 1 0 1 1 0 1	M (DP) ← (AC)	1	1	AC contents stored in memory M (DP).	
	LDI X	0 0 1 1 $X_3X_2X_1X_0$	AC ← X	1	1	Immediate data X loaded to AC.	
	MVI X	0 0 1 0 $X_3X_2X_1X_0$	M (DP) ← X	1	1	Immediate data X loaded to memory M (DP).	

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Instruction	Mnemonic	Instruction code	Function	Bytes	Cycles	Function description	Status flag affected
CPU control	HALT	0 0 0 0 0 0 0 0	CPU operation halts	1	1	• Halts CPU operation. HALT mode is released under the following conditions. • HALT mode is cancelled by the interaction of SIC X and SC5 commands.	
	SCI X	1 1 0 1 $X_3X_2X_1X_0$	CTL2 ← X	1	1	X_0 to X_3: Operation. X_0: HFE1 is set to enable release of HALT mode by overflow signal from divider circuit following CF oscillation circuit. X_1: HFE2 is set enabling signal rise at input port S to release HALT mode. X_2: HFE3 is set enabling signal rise at input port M to release HALT mode. X_3: HFE4 is set enabling 1/10 second pulse to release HALT.	HEF1 to HEF4
	NOP	1 1 1 1 1 1 1 1	No operation	1	1	No operation.	
Input/Output	IPS	1 0 1 0 1 1 1 1	AC ← [P (S)]	1	1	Input data at input port S loaded to AC.	
	IPM	1 0 1 0 1 0 0 0	AC ← [P (M)]	1	1	Input data at input port M loaded to AC.	
	SPDR X	1 1 1 1 0 1 X_1X_0	PDF ← X	1	1	Pull-down resister MOS-Tr at corresponding input port turned ON/OFF. Bit content / Operation X_0=0: S-Terminal Pull down Tr OFF. X_0=1: S-Terminal Pull down Tr ON. X_1=0: M-Terminal Pull down Tr OFF. X_1=1: M-Terminal Pull down Tr ON.	PDF
	OUT	1 1 1 1 1 1 0 0	(1) Cannot be used when SPC =0&SP=0H to CH, EH, FH.	1	1	Cannnot be used. (Causes error when OUT is executed at SPC=0&SP=0H to CH, EH, FH.)	
			(2) When SP=0&SP=D CTL3 ← (AC)			AC contents transferred to CTL3.	CFCF CCF
			(3) When SPC=1 SFR ← (AC)			AC contents transferred to special function register SFR.	
	TWRT	0 0 0 0 0 0 1 0	(1) Cannot be used when SPC =0&SP=0H to CH, EH, FH.	1	1	Cannnot be used. (Causes error when TWRT is executed at SPC=0&SP=0H to CH, EH, FH.)	
			(2) When SPC=0&SP=D CTL3 ← ROM			High-order 4 bits data of ROM, on current page, addressed by PC whose low-order 8 bits are replaced by AC and M (DP) contents, is transferred to CTL3.	CFCF CCF
			(3) When SPC=1 SFR ← ROM			High-order 4 bits or 8 bits data of ROM, on the current page, addressed by PC whose low-order 8 bits are replaced by AC and M (DP) contents is transferred to special function register SFR	
	IN	0 0 0 1 0 1 1 1	(1) Cannot be used at SPC =0&SP=0H to CH, EH, FH.	1	1	Cannnot be used. (Causes error when IN is executed at SPC=0&SP=0H to CH, EH, FH.)	
			(2) When SPC=0&SP=D AC ← (STS3)			STS3 contents transferred to AC.	
			(3) When SPC=1 AC ← (SFR)			Special function register SFR contents transferred to AC.	

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Instruction	Mnemonic	Instruction code	Function	Bytes	Cycles	Function description	Status flag affected
Branching/subroutine	JMP X	0 0 0 0 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	(PC_{10} to PC_0) ← X_{10} to X_0	2	2	Loads data specified by X_{10} to X_0 to PC and jumps unconditionally.	
	BAB0 X	0 1 0 0 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC_0=1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC bit 0 is '1', data specified by X_{10} to X_0 is loaded to PC and jumps. At '0', PC is incremented +2.	
	BAB1 X	0 1 0 1 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC_1=1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC bit 1 is '1', data specified by X_{10} to X_0 is loaded to PC and jumps. At '0', PC is incremented +2.	
	BAB2 X	0 1 1 0 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC_2=1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC bit 2 is '1', data specified by X_{10} to X_0 is loaded to PC and jumps. At '0', PC is incremented +2.	
	BAB3 X	0 1 1 1 1 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC_3=1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC bit 3 is '1', data specified by X_{10} to X_0 is loaded to PC and jumps. At '0', PC is incremented +2.	
	BAZ X	0 1 0 0 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC=0 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC is '0', data specified by X_{10} to X_0 is loaded to PC and jumps. When AC is not '0', PC is incremented +2.	
	BANZ X	0 1 0 1 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If AC≠0 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When AC is not '0', data specified by X_{10} to X_0 is loaded to PC and jumps. When AC is '0', PC is incremented +2.	
	BCNH X	0 1 1 0 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If CF≠1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When CF is '0', data specified by X_{10} to X_0 is loaded to PC and jumps. When CF is '1', PC is incremented +2.	
	BCH X	0 1 1 1 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	If CF=1 then (PC_{10} to PC_0) ← X_{10} to X_0	2	2	When CF is '1', data specified by X_{10} to X_0 is loaded to PC and jumps. When CF is '0', PC is incremented +2.	
	PAGE	0 0 0 1 0 0 0 1	PAGE ← [M (DP)]	1	1	Memory M (DP) contents loaded to PAGE latch.	
	JMP*	0 0 0 1 0 0 0 0	PC_{10} to PC_{08} ← (PAGE) PC_{07} to PC_{04} ← (AC) PC_{03} to PC_{00} ← [M (DP)]	1	1	Unconditionally jumps to page specified by PAGE and address whose low-order 8 bits are specified by contents of AC and memory M (DP).	
	ROM0	1 1 0 0 1 0 0 0 0 0 1 0 0 0 0 0	PC_{11} ← 0	2	2	Select ROM bank 0.	
	ROM1	1 1 0 0 1 0 0 0 0 0 1 0 0 0 0 1	PC_{11} ← 1	2	2	Select ROM bank 1.	
	JSR X	1 0 1 0 0 $X_{10}X_9X_8$ $X_7X_6X_5X_4$ $X_3X_2X_1X_0$	STACK ← (PC)+2 (PC_{10} to PC_0) ← X_{10} to X_0	2	2	Current PC+2 contents are saved in STACK, data specified by X_{10} to X_0 is loaded to PC and sub-routine is called.	
	RST	0 0 0 1 0 0 1 1	PC ← (STACK)	1	1	Returns PC contents saved in STACK to PC and returns from sub-routine.	
Miscellaneous	SPC0	1 1 0 0 1 0 0 1 0 0 1 0 0 0 0 0	SPC ← 0	2	2	Resets strobe pointer control bit (SPC) to '0'.	SPC
	SPC1	1 1 0 0 1 0 0 1 0 0 1 0 0 0 0 1	SPC ← 1	2	2	Sets strobe pointer control bit (SPC) to '1'.	SPC
	CSEC	1 1 1 1 1 0 1 1	ϕ11 to ϕ15 ← 0	1	1	Resets high-order 4 bits of divider circuit.	SCF0 SCF4
	RWDT	1 1 1 1 1 0 0 1	(WDT) ← 0	1	1	Resets Watchdog Timer counter.	

LC573100 Series Instructions Map

Uppwer \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	HALT	**TAAT**	**TWRT**	–	CSP	CST	RC5	SC5	JMP X							
1	JMP*	PAGE	MTR	RTS	–	–	–	IN	ASR0	ASR1	ASL0	ASL1	SDPL	SDPH	EDPL	EDPH
2	MVI X															
3	LDI X															
4	BAZ X								BAB0 X							
5	BCNH X								BAB1 X							
6	BCNH X								BAB2 X							
7	BCH X								BAB3 X							
8	ADC	SBC	ADD	SUB	ADN	AND	EOR	OR	ADC*	SBC*	ADD*	SUB*	ADN*	AND*	EOR*	OR*
9	ADCI	SBCI	ADDI	SUBI	ADNI	ANDI	EORI	ORI	INC	DEC	IDPL	DDPL	IDPH	DDPH	ISP	DSP
A	JSR X								IPM	LDA	LSP	LHLT	L500	STA	SSP	IPS
B	MDPL X															
C	MDPH X				–				ROMX	SPCX	–					
D	SIC X															
E	MSP X															
F	RCF	SCF	NOP	NOP	SPDR X				–	RWDT	–	CSEC	OUT	LDPL	LDPH	NOP

XXX : 1 Byte-1 Cycle instruction

XXX : 2 Byte-2 Cycle instruction

XXX : 1 Byte-2 Cycle instruction

ROMX : ROM0 instruction (C820H),
ROM1 instruction (C821H)

SPCX : SPC0 instruction (C920H),
SPC1 instruction (C921H)

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