MAX17548

42V, Dual-Output, Synchronous Step-Down Controller

General Description

The MAX17548 is a dual-output, synchronous step-down controller that drives nMOSFETs.

The device features a peak-current-mode, constant-frequency architecture, allowing it to operate up to 2.2MHz. The device can be configured as two single-phase, independent 10A power supplies or as a dual-phase, single-output 20A power supply. The device also provides the ability to run two controllers 180° out-of-phase to reduce the power loss and noise due to the input-capacitor ESR.

The IC supports current sensing using either an external current-sense resistor for accuracy or an inductor DCR for improved system efficiency. Current foldback limits MOSFET power dissipation under short-circuit conditions.

The IC provides independent adjustable soft-start for each output and can start up monotonically into a prebiased output. The IC can be configured in either PWM or DCM modes of operation, depending on whether constant-frequency operation or light-load efficiency is desired.

The IC operates over the -40°C to +125°C temperature range and is available in a lead(Pb)-free, 32-pin TQFN, 5mm x 5mm package with an exposed pad.

Applications

- Industrial Power Supplies
- Distributed DC Power Systems
- Motion Control
- Programmable Logic Controllers
- Computerized Numerical Control

Benefits and Features

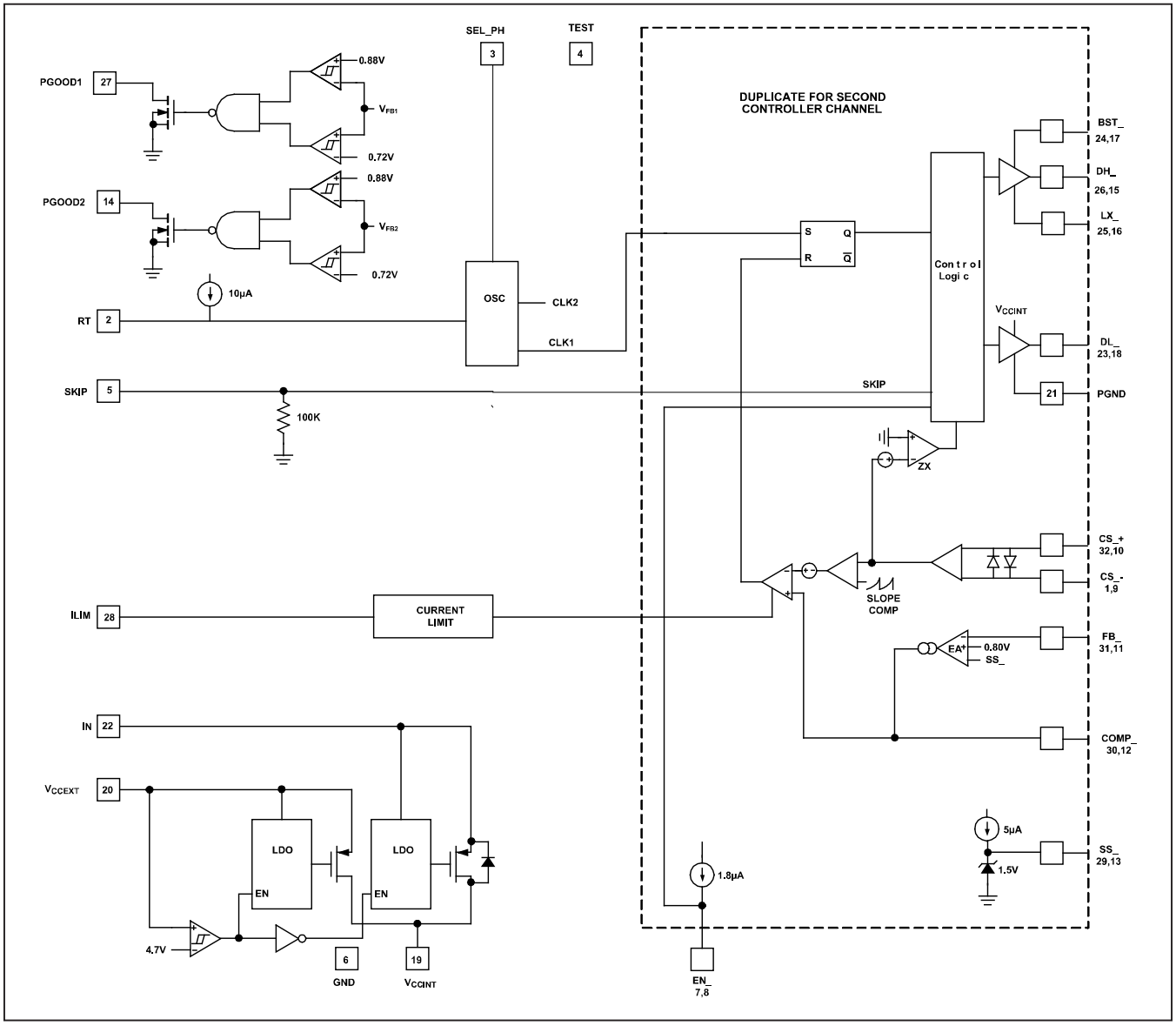
- Wide Range of Operation
  - Wide 4.5V to 42V Input Voltage Range
  - Wide 0.8V to 24V Output Voltage Range
  - R_{SENSE} or Inductor DCR Current Sensing
  - Selectable In-Phase or 180° Out-of-Phase Operation
  - Adjustable 100kHz to 2.2MHz Switching Frequency
  - Independent Enable and PGOOD
  - Available in a Lead(Pb)-Free 32-Pin, 5mm x 5mm TQFN-EP Package
- Enhances Power Efficiency
  - Low-Impedance Gate Drives for High Efficiency
  - DCM Operation at Light Loads
  - Auxiliary Bootstrap LDO
- Operates Reliably in Adverse Industrial Environments
  - Independent Adjustable Soft-Start or Tracking
  - Current Foldback Limits MOSFET Heat Dissipation During a Short-Circuit Condition
  - Operates Over the -40°C to +125°C Temperature Range
  - Output Overvoltage and Overtemperature Protections

***Ordering Information* appears at end of data sheet.**

19-8778; Rev 0; 2/17

maxim integrated™

Block Diagram



Absolute Maximum Ratings

IN to GND ..... -0.3V to +48V
CS_+ to GND ..... -0.3V to +40V
CS_+ to CS_- ..... -0.3V to +0.3V
LX_, BST_ to PGND ..... -0.3V to +48V
BST_ to LX_ ..... -0.3V to +6V
BST_ to V_{CCINT} ..... -0.3V to +48V
DH_ to LX_ ..... -0.3V to ($V_{BST_}$ + 0.3)V
DL_ to PGND ..... -0.3V to (V_{CCINT} + 0.3)V
EN_ to GND ..... -0.3V to +6V
V_{CCINT} to GND ..... -0.3V to +6V
V_{CCEXT} to GND ..... -0.3V to +26V
PGND to GND ..... -0.3V to +0.3V
PGOOD_ to GND ..... -0.3V to +6V
FB_, COMP_, SS_, RT, SKIP, SEL_PH, I_{LIM} ..... -0.3V to (V_{CCINT} + 0.3)V
GND to EP ..... -0.3V to +0.3V
Continuous Power Dissipation at +70°C (multilayer board) 2758.6mW
Power Deration (multilayer board) ..... 34.5 mW/°C
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 29°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 24V, RT = open, C_{VCCINT} = 4.7µF, EN_ = open, DH_, DL_ = open, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}		4.5		42	V
		V_{CCINT} = V_{IN}	4.5		5.5	
Operating Supply Current (Note 3)	I_{IN}	SKIP = open, LX_ = PGND, BST_ = 5V EN1 = open, EN2 = GND, V_{FB1} = 0.84V or EN2 = open, EN1 = GND, V_{FB2} = 0.84V	0.5	1.5	2.0	mA
		SKIP = open, LX_ = PGND, BST_ = 5V EN1 = EN2 = open, V_{FB1} = V_{FB1} = 0.84V	1	2.5	3.5	
		SKIP = V_{CCINT}, LX_ = PGND, BST_ = 5V EN1 = open, EN2 = GND, V_{FB1} = 0.76V or EN2 = open, EN1 = GND, V_{FB2} = 0.76V	1	1.8	3.5	mA
		SKIP = V_{CCINT}, LX_ = PGND,BST_=5V EN1 = EN2 = open, V_{FB1} = V_{FB1} = 0.76V	1.5	3.2	5	
Shutdown Supply Current		EN1 = EN2 = GND		10	20	µA

Electrical Characteristics (continued)

(V_{IN} = 24V, RT = open, C_{VCCINT} = 4.7µF, EN_ = open, DH_, DL_ = open, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CCINT} REGULATOR						
V_{CCINT} Output Voltage	V_{CCINT}	6V < V_{IN} < 42V, I_{VCCINT} = 1mA	4.95	5.1	5.25	V
		6V < V_{CCEXT} < 24V, I_{VCCINT} = 1mA (V_{CCINT} supplied from V_{CCEXT})	4.95	5.1	5.25	
V_{CCINT} Load Regulation		V_{IN} = 12V, I = 0mA to 100mA, VCCEXT = 0V (V_{CCINT} supplied from V_{IN})	5	25	50	mV
		V_{VCCEXT} = 12V, I_{VCCINT} = 0mA to 100mA (V_{CCINT} supplied from V_{CCEXT})	5	25	50	
V_{CCINT} Short-Circuit Output Current		V_{IN} = 8.5V, V_{CCEXT} = 0V, V_{CCINT} = 4V	120	250	340	mA
		V_{CCEXT} = 8.5V, V_{CCINT} = 4V (V_{CCINT} supplied from V_{CCEXT})	120	250	340	
V_{CCINT} Dropout Voltage		V_{IN} = 4.5V, load = 75mA, V_{CCEXT} = 0	50	150	420	mV
		V_{CCINT} supplied from V_{CCEXT}, V_{IN} = 24V, V_{CCEXT} = 4.7V, load = 75mA	50	150	420	
V_{CCEXT} Switch Overvoltage		V_{CCEXT} rising	4.55	4.7	4.85	V
V_{CCEXT} Switch Overvoltage Hysteresis			0.2	0.25	0.3	V
V_{CCINT} UVLO		V_{CCINT} rising	4	4.2	4.4	V
		V_{CCINT} falling	3.5	3.7	3.9	
OSCILLATOR						
Switching Frequency	f_{SW}	RT = 62kΩ	405	440	475	kHz
		RT = V_{CCINT}	480	535	590	
		RT = GND	325	350	375	
RT Pullup Current		V_{RT} = 0.5V	9.5	10	10.5	µA
Switching Frequency Adjustable Range	f_{SW}	26.5kΩ < RT < 280kΩ	100		2200	kHz
SKIP						
DCM Mode Setting Range			1.25		V_{CCINT} -1.6	V
PWM Mode Setting Range			V_{CCINT} - 1.5		V_{CCINT}	V
SKIP Pulldown Resistance			70	100	130	kΩ

Electrical Characteristics (continued)

(V_{IN} = 24V, RT = open, C_{VCCINT} = 4.7µF, EN_ = open, DH_, DL_ = open, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER						
DH_ to BST_ On-Resistance		Sourcing 100mA	0.7	1.3	2.5	Ω
DH_ to LX_ On-Resistance		Sinking 100mA	0.25	0.5	0.9	Ω
DL_ to V_{CCINT} On-Resistance		Sourcing 100mA	0.7	1.3	2.5	Ω
DL_ to PGND_ On-Resistance		Sinking 100mA	0.35	0.75	1.25	Ω
DH_ Minimum Controlled On-Time	t_{ON_MIN}			120	155	ns
DL_ Minimum Controlled Off-Time	t_{OFF_MIN}	PWM mode, $V_{FB_}$ = 0.84V	80	120	160	ns
Dead Time	t_{DT}	DH_ falling to DL_ rising, C_{LOAD} = 6nF		30		ns
		DL_ falling to DH_ rising, C_{LOAD} = 6nF		30		
DH_ Transition Time		DH_ rising, C_{LOAD} = 6nF		25		ns
		DH_ falling, C_{LOAD} = 6nF		15		
DL_ Transition Time		DL_ rising, C_{LOAD} = 6nF		25		ns
		DL_ falling, C_{LOAD} = 6nF		15		
SOFT-START						
Soft-Start Current	I_{SS}	V_{SS} = 0.5V	3.5	5	6.5	µA
ENABLE						
EN_ Logic-High Threshold		EN_ rising	1.2	1.25	1.3	V
EN_ Hysteresis				90		mV
EN_ Bias Pullup Bias Current		$V_{EN_}$ = 0.5V	0.9	1.8	2.7	µA
CURRENT-SENSE AMPLIFIER						
CS_+ , CS_- Common-Mode Voltage Range			0		24	V
CS_+ to CS_- Input Operating Voltage Range	V_{CS_+} - V_{CS_-}	0 < V_{CS_-} < 24V	-100		+100	mV
Current-Sense Amplifier Gain		ILIM = GND	30	33.3	36.6	V/V
		ILIM = open	18	20	22	
		V_{ILIM} = V_{CCINT}	12	13.3	14.5	
CS_+ Input Bias Current		0 < V_{CS_-} < 24V, T_A = T_J = +25°C		0.01	1	µA
CS_- Input Bias Current		V_{CS_+} = V_{CS_-} = 1.2V or 24V	5		600	µA

Electrical Characteristics (continued)

(V_{IN} = 24V, RT = open, C_{VCCINT} = 4.7µF, EN_ = open, DH_, DL_ = open, T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMIT						
Cycle-by-Cycle Peak Positive Current-Limit Threshold	V_{CS}	ILIM = open, V_{IN} = 12V, V_{OUT} = 1.25V	42.5	50	55	mV
		ILIM = GND, V_{IN} = 12V, V_{OUT} = 1.25V	23	30	37	
		V_{ILIM} = V_{CCINT}, V_{IN} = 12V, V_{OUT} = 1.25V	65	75	85	
ERROR AMPLIFIER						
Feedback Regulation Voltage	$V_{FB_}$		788	800	812	mV
FB _ Input Leakage Current		$V_{FB_}$ = 0.8V, T_A = T_J = +25°C	-100	0	+100	nA
Transconductance	$g_{M_}$		1.7	2	2.3	mA/V
POWER-GOOD OUTPUTS						
PGOOD_ Threshold	$V_{FB_}$ rising		103	110	113	% of FB_
	$V_{FB_}$ falling		87	90	93	
PGOOD_ Output Low Level		$I_{PGOOD_}$ = 10mA	0.05	0.15	0.25	V
PGOOD_ Leakage Current		$V_{PGOOD_}$= 5V , T_A = T_J = +25°C	-100		+100	nA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold				160		°C
Thermal-Shutdown Hysteresis				20		°C

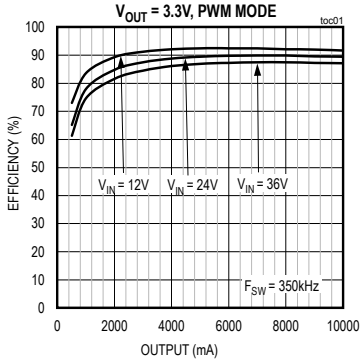
Note 2: Limits are 100% tested at T_A = +25°C. Limits over the temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: This supply current excludes the switching current due to the external MOSFETs' gate charge.

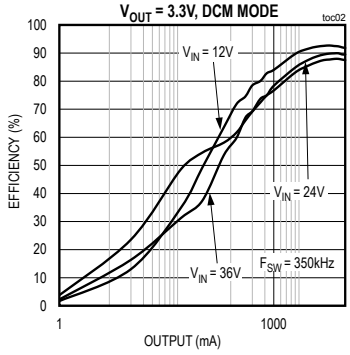
Typical Operating Characteristics

(V_{IN} = 24V, unless otherwise noted. See Figure 8.)

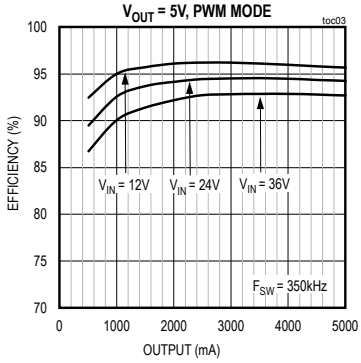
EFFICIENCY vs. OUTPUT CURRENT
V_{OUT} = 3.3V, PWM MODE



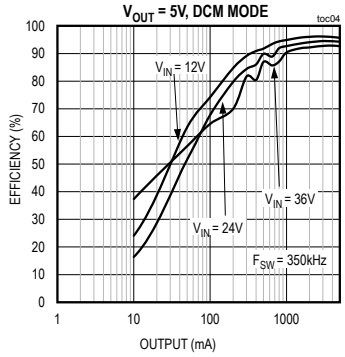
EFFICIENCY vs. OUTPUT CURRENT
V_{OUT} = 3.3V, DCM MODE



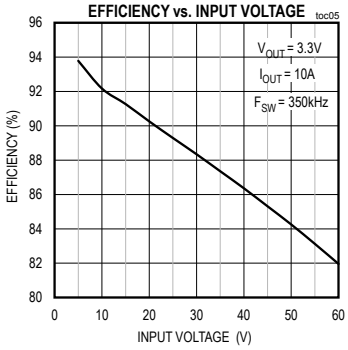
EFFICIENCY vs. OUTPUT CURRENT
V_{OUT} = 5V, PWM MODE



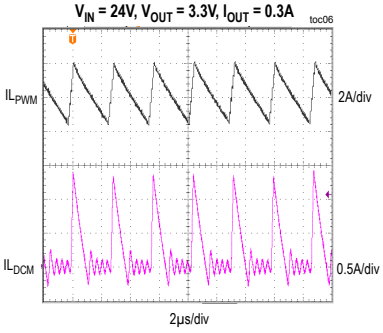
EFFICIENCY vs. OUTPUT CURRENT
V_{OUT} = 5V, DCM MODE



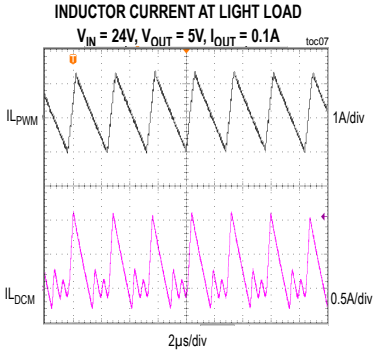
EFFICIENCY vs. INPUT VOLTAGE



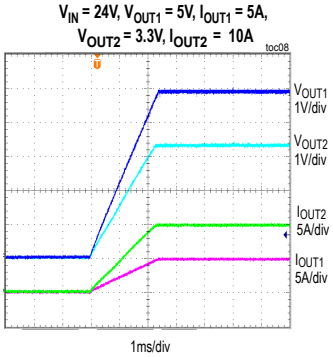
INDUCTOR CURRENT AT LIGHT LOAD
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 0.3A



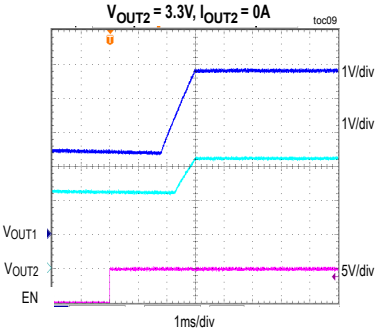
INDUCTOR CURRENT AT LIGHT LOAD
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.1A



STARTUP FROM ENABLE
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 5A,
V_{OUT2} = 3.3V, I_{OUT2} = 10A



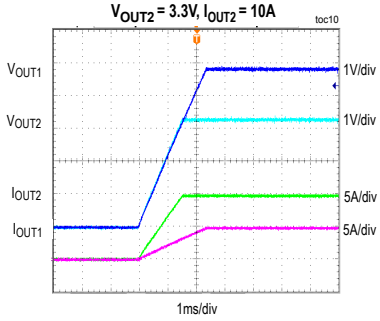
STARTUP INTO PREBIASED OUTPUT
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 0A,
V_{OUT2} = 3.3V, I_{OUT2} = 0A



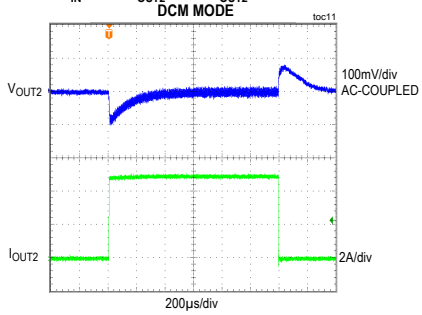
Typical Operating Characteristics (continued)

(V_{IN} = 24V, unless otherwise noted. See Figure 8.)

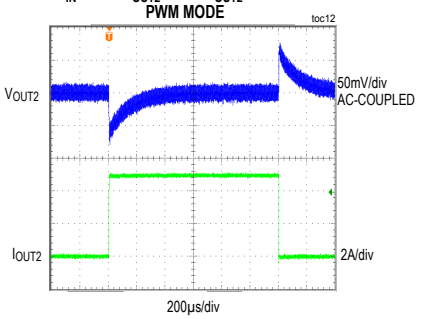
COINCIDENT TRACKING AT STARTUP
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 5A,
V_{OUT2} = 3.3V, I_{OUT2} = 10A



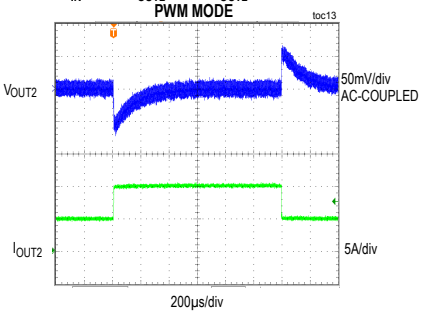
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT2} = 3.3V, I_{OUT2} = 0.1A to 5A
DCM MODE



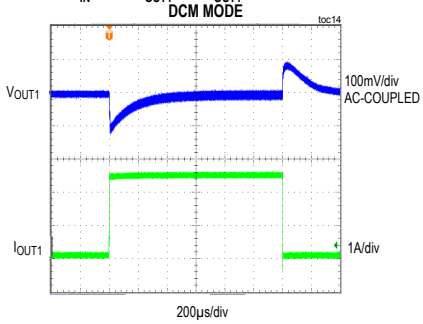
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT2} = 3.3V, I_{OUT2} = 0A to 5A
PWM MODE



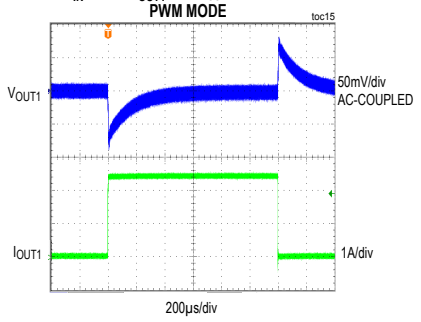
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT2} = 3.3V, I_{OUT2} = 5A to 10A
PWM MODE



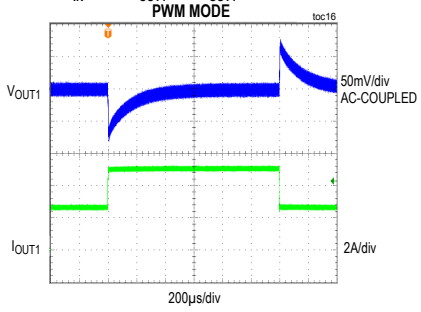
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 0.05A to 2.5A
DCM MODE



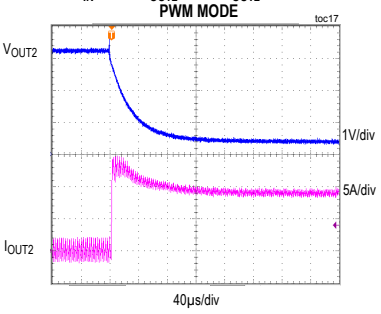
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 0A to 2.5A
PWM MODE



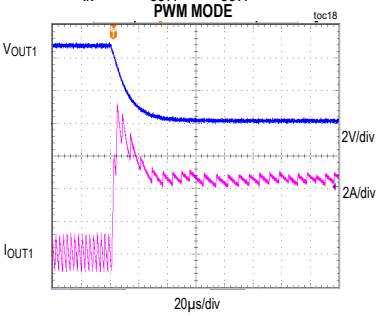
LOAD TRANSIENT RESPONSE
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = 2.5A to 5A
PWM MODE



OVERCURRENT PROTECTION
V_{IN} = 24V, V_{OUT2} = 3.3V, I_{OUT2} = SHORT
PWM MODE



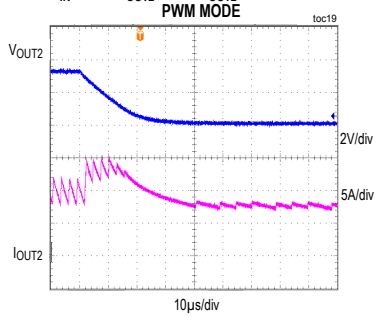
OVER CURRENT PROTECTION
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT1} = SHORT
PWM MODE



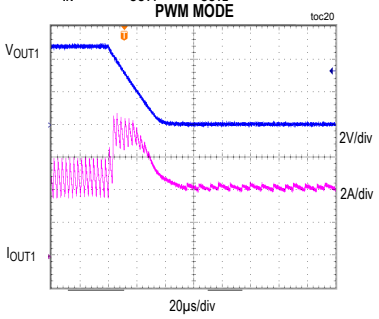
Typical Operating Characteristics (continued)

(V_{IN} = 24V, unless otherwise noted. See Figure 8.)

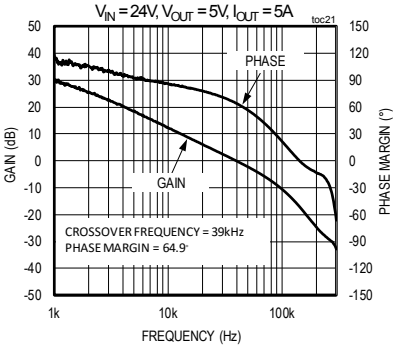
SHORT-CIRCUIT UNDER STEADY-STATE
V_{IN} = 24V, V_{OUT2} = 3.3V, I_{OUT2} = 10A TO SHORT
PWM MODE



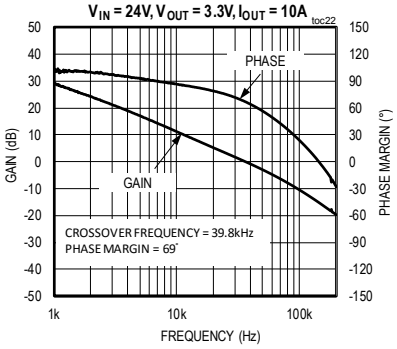
SHORT-CIRCUIT UNDER STEADY-STATE
V_{IN} = 24V, V_{OUT1} = 5V, I_{OUT2} = 5A TO SHORT
PWM MODE



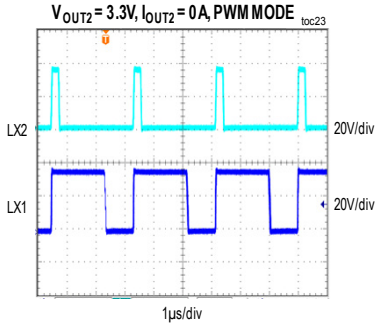
CLOSED-LOOP BODE PLOT
V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 5A



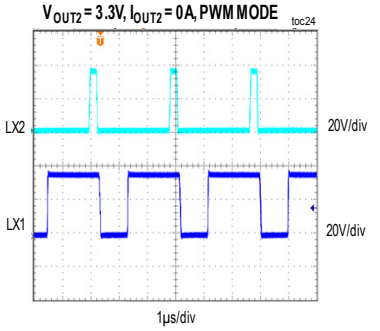
CLOSED-LOOP BODE PLOT
V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 10A



0° IN-PHASE OPERATION
V_{IN} = 36V, V_{OUT1} = 24V, I_{OUT2} = 0A
V_{OUT2} = 3.3V, I_{OUT2} = 0A, PWM MODE

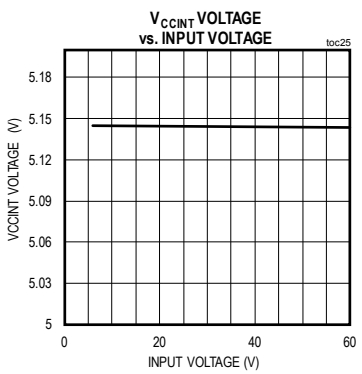


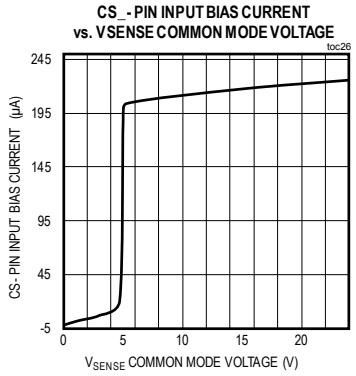
180° OUT-OF-PHASE OPERATION
V_{IN} = 36V, V_{OUT1} = 24V, I_{OUT2} = 0A
V_{OUT2} = 3.3V, I_{OUT2} = 0A, PWM MODE

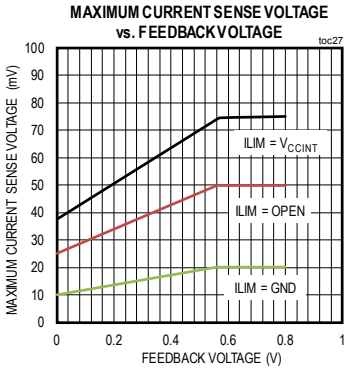


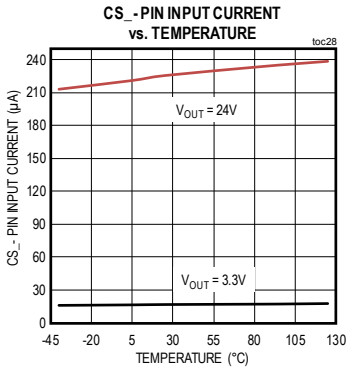
Typical Operating Characteristics (continued)

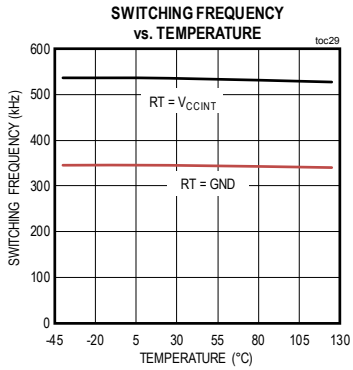
(V_{IN} = 24V, unless otherwise noted. See Figure 8.)

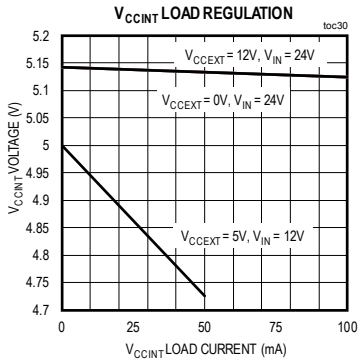




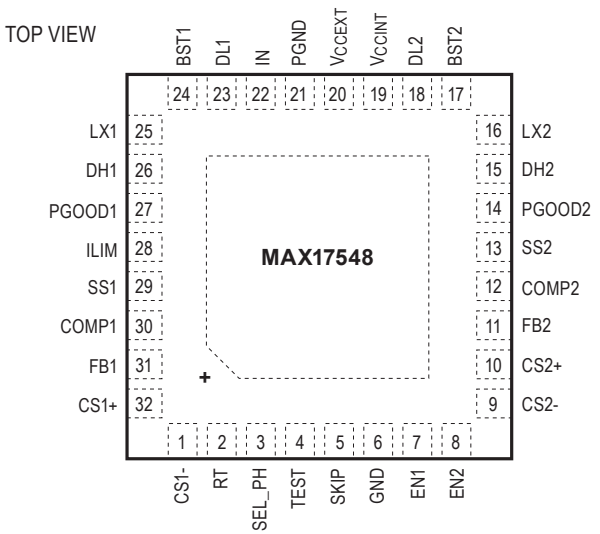








Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	FUNCTION
1, 9	CS1-, CS2-	Current-Sense Amplifier Negative Input of Controller 1 and Controller 2, Respectively. Connect to negative terminal of current-sense signal. See Figure 5 and Figure 6.
2	RT	Switching-Frequency Programming Resistor Connection. Connect a resistor between RT and GND to set the switching frequency. See Figure 3. Connect to V_{CCINT} to program switching frequency of 535kHz. Connect to GND to program switching frequency of 350kHz.
3	SEL_PH	Phase-Selection Input. The SEL_PH pin programs the phase shift between the two controllers of the device.
4	TEST	Connect to GND
5	SKIP	Connect SKIP to V_{CCINT} to select PWM mode of operation. Pull up SKIP with 100kΩ to V_{CCINT} or connect to a voltage between 1.25V and V_{CCINT} - 1.5V to program DCM mode of operation. SKIP is internally pulled down to GND by 100kΩ.
6	GND	Signal Ground Connection. GND should connect to the PGND plane at a single point. Refer to the MAX17558 evaluation kit data sheet PCB layout for an example grounding scheme.
7, 8	EN1, EN2	Enable Input for Controller 1 and Controller 2. Either leave unconnected or connect to a voltage between 1.25V and 5.5V to enable corresponding controller. Connect to GND to disable corresponding controller.

Pin Description (continued)

PIN	NAME	FUNCTION
10, 32	CS2+, CS1+	Current-Sense Amplifier Positive Input of Controller 2 and Controller 1. Connect to positive terminal of current-sense signal. See Figure 5 and Figure 6.
11, 31	FB2, FB1	Feedback Voltage Input of Controller 2 and Controller 1. Connect the FB_ pins to the midpoint of a resistor-divider from output to GND. See the circuit of Figure 4 for details.
12, 30	COMP2, COMP1	Error-Amplifier Output and Compensation Network-Connection Node for Controller 2 and Controller 1. Connect the COMP_ pins to the compensation network as shown in the circuit of Figure 7.
13, 29	SS2, SS1	Output-Voltage Soft-Start Time Programming Pins. Connect a capacitor from SS_ to GND to program output-voltage soft-start time. Alternatively, a resistor-divider on another voltage supply connected to this pin allows the device output to track the other supply during startup. See the *Shutdown and Startup (EN_ and SS_)* and *Soft-Start Capacitor* sections for more details.
14, 27	PGOOD2, PGOOD1	Open-Drain Power-Good Pins of Controller 2 and Controller 1. Pull up with external resistor to a maximum of 5.5V.
15, 26	DH2, DH1	High-Side MOSFET Gate-Driver Output of Controller 2 and Controller 1. Connect to gate of respective high-side MOSFET.
16, 25	LX2, LX1	Switching Node Connection Input of Controller 2 and Controller 1. Connect to respective output-filter inductors.
17, 24	BST2, BST1	Bootstrap Capacitor Connection Input of Controller 2 and Controller 1. Connect a capacitor between BST_ and corresponding LX_. See the *Bootstrap Capacitor Selection* section for more details.
18, 23	DL2, DL1	Low-Side MOSFET Gate-Driver Output of Controller 2 and Controller 1. Connect to gate of respective low-side MOSFET.
19	V_{CCINT}	Internal LDO Output. Connect a minimum 4.7µF low-ESR ceramic capacitor between V_{CCINT} and PGND.
20	V_{CCEXT}	External Power-Supply Input for Internal LDO. Apply a voltage between 4.85V and 24V to disconnect the LDO that operates from IN, and power internal circuitry with the LDO connected to V_{CCEXT}. A minimum of 0.1µF local decoupling for the V_{CCEXT} pin is recommended.
21	PGND	Power Ground. Connect to the source terminal of the external low-side MOSFETs and V_{CCINT} bypass capacitor return terminal. Refer to the MAX17558 evaluation kit data sheet PCB layout for an example.
22	IN	Supply Input. Bypass with minimum 1µF low-ESR ceramic capacitor to PGND.
28	ILIM	Current-Limit Selection Input for Both Controllers. See the *Peak Current-Limit Programming (ILIM)* section for a more detailed description.
—	EP	Exposed Pad. Connect to GND pin of the IC. Connect to a large copper plane with multiple vias to improve thermal performance. Refer to the MAX17558 evaluation kit data sheet PCB layout for an example grounding scheme and thermal via arrangement.

Detailed Description

The MAX17548 is a dual-output synchronous step-down controller that operates from a 4.5V to 42V wide input supply range with programmable output voltage ranging from 0.8V to 24V. The IC uses constant-frequency, peak current-mode control for the control loop. The frequency of the device can be adjusted from 100kHz to 2.2MHz using a resistor at the RT pin. Input capacitor size can be minimized by running the two outputs 180° out-of-phase.

The phase shift between the two controllers of the IC can be selected using the SEL_PH pin. The device provides independent adjustable soft-start and can start up monotonically with a prebiased output voltage. It also features selectable DCM/PWM mode of operation. Other features include independent open-drain PGOOD_ outputs and independent enable (EN_) inputs.

Internal LDO (V_{CCINT})

The IC has two internal 100mA low-dropout (LDO) linear regulators that power V_{CCINT}. One regulator is powered from IN, while the other is powered from V_{CCEXT}. At any time, one of the two regulators is in operation depending on the voltage levels at V_{CCEXT}. If V_{CCEXT} voltage is greater than 4.7V (typ) then V_{CCINT} is powered from the V_{CCEXT} regulator. If V_{CCEXT} is lower than 4.55V (typ), then V_{CCINT} is powered from the IN regulator. Powering V_{CCINT} from V_{CCEXT} increases efficiency at higher input voltages. V_{CCEXT} can be connected to one of the switching regulator outputs if that output voltage is greater than 4.7V (typ). The maximum voltage limit on V_{CCEXT} is 24V.

V_{CCINT} output voltage powers the gate drivers and internal control circuitry. V_{CCINT} should be decoupled to PGND with at least a 4.7µF low-ESR ceramic capacitor. The IC employs an undervoltage-lockout (UVLO) circuit that forces both the regulators off when V_{CCINT} falls below 3.8V (typ). The regulators are enabled again when V_{CCINT} > 4.2V (typ).

Low-Side Gate Driver (DL_)

Low-side external MOSFET gate drivers are powered from V_{CCINT}. Under normal operating conditions, the low-side gate-driver output (DL_) is always the complement of the high-side gate-driver output (DH_). On each controller, dedicated circuitry monitors the DH_ and DL_ outputs and prevents either gate-drive signal from turning on until the other gate-drive signal is fully off. Thus, the circuit allows DH_ to turn on only when DL_ has been turned off. Similarly, it prevents DL_ from turning on until DH_ has been turned off.

There must be a low-impedance path from the DL_ and DH_ pins to the external MOSFET gates to ensure that the gate driver's circuitry works properly. To minimize impedance, very short, wide traces should be used in the PCB layout. The internal pulldown transistor that drives the DL_ low is robust with a 0.75Ω (typ) on-resistance. This low on-resistance helps prevent DL_ from being pulled up during the fast rising of the LX_ node, due to capacitive coupling from the drain to the gate of the low-side synchronous rectifier MOSFET.

High-Side Gate Driver (DH_)

High-side gate drivers are powered from the bootstrap capacitors connected between BST_ and LX_. The bootstrap capacitor normally gets charged to V_{CCINT} during each switching cycle through an external Schottky diode, when the low-side MOSFET turns on.

The high-side MOSFET is turned on by closing an internal switch between BST_ and DH_. This provides the necessary gate-to-source voltage to turn on the high-side MOSFET. See the *Bootstrap Capacitor Selection* section to choose the right size of the bootstrap capacitor.

Shutdown and Startup (EN_ and SS_)

The two controllers of the IC can be independently shut down and enabled using the EN1 and EN2 pins. Pulling either of these pins below 1.25V (typ) shuts down the corresponding controller. Pulling both EN1 and EN2 below 0.7V disables both controllers and most internal circuits, including the V_{CCINT} LDOs. In this state, the device draws only 10µA (typ) of quiescent current.

The EN_ pin can be open or externally pulled up to a voltage between 1.25V (typ) and 5.5V to turn on the corresponding controller. Figure 1 shows the possible EN_ pin configurations.

The startup of each controller's output voltage is controlled by the voltage on the relevant SS_ pin for that controller. When the voltage on the SS_ pin is less than the 0.8V internal reference, the device regulates the FB_ voltage to the SS_ pin voltage instead of the 0.8V internal fixed reference. This allows the SS_ pin to be used to program the output-voltage soft-start time by connecting an external capacitor from the SS_ pin to GND. An internal 5µA pullup current charges this capacitor, creating a voltage ramp on the SS_ pin. As the SS_ voltage rises linearly from 0 to 0.8V, the output voltage rises smoothly from zero to its final value.

Alternatively, the SS_ pin can be used to track the output to that of another supply at startup. This requires connecting the SS_ pin to an external resistor-divider from the supply that needs to be tracked to GND. Figure 2 shows the possible ways of configuring the SS_ pin.

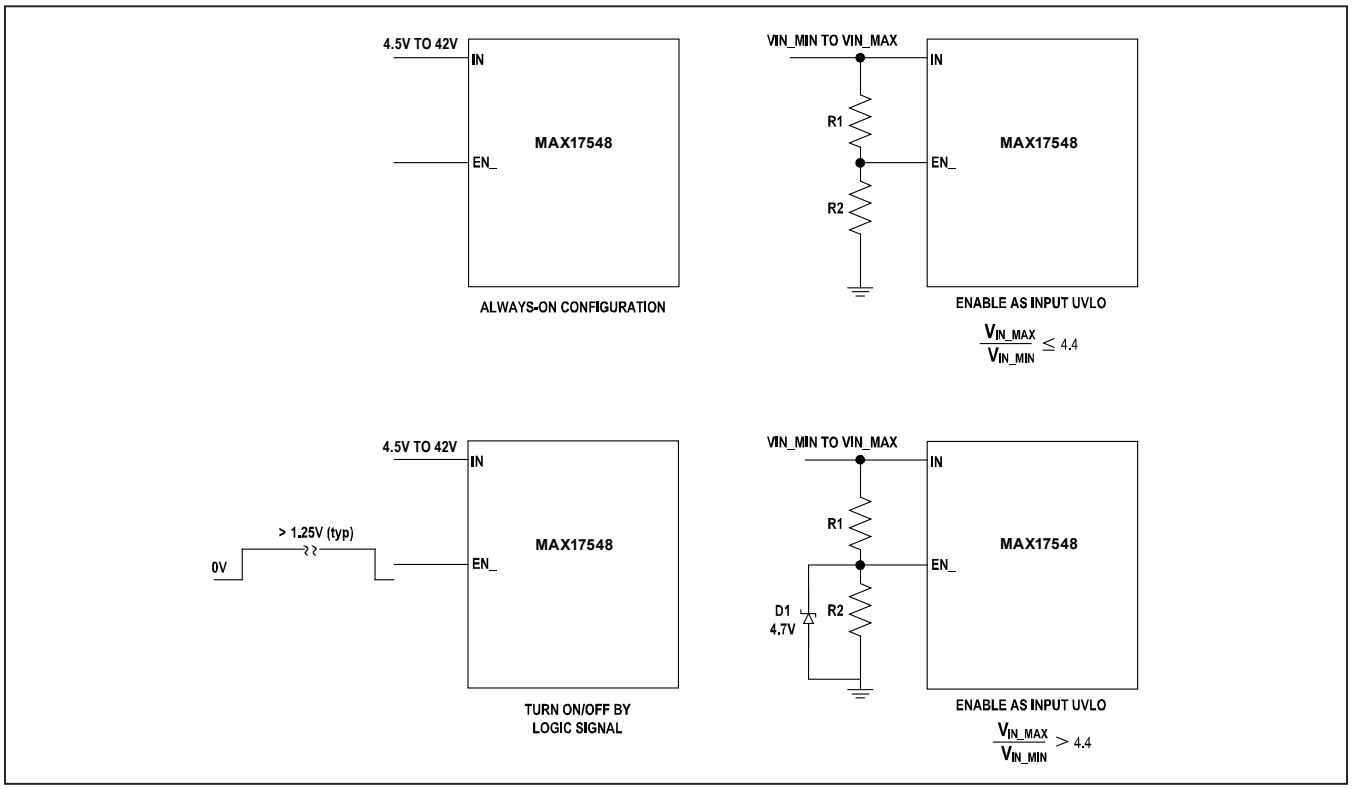


Figure 1. Possible EN_ Pin Configurations

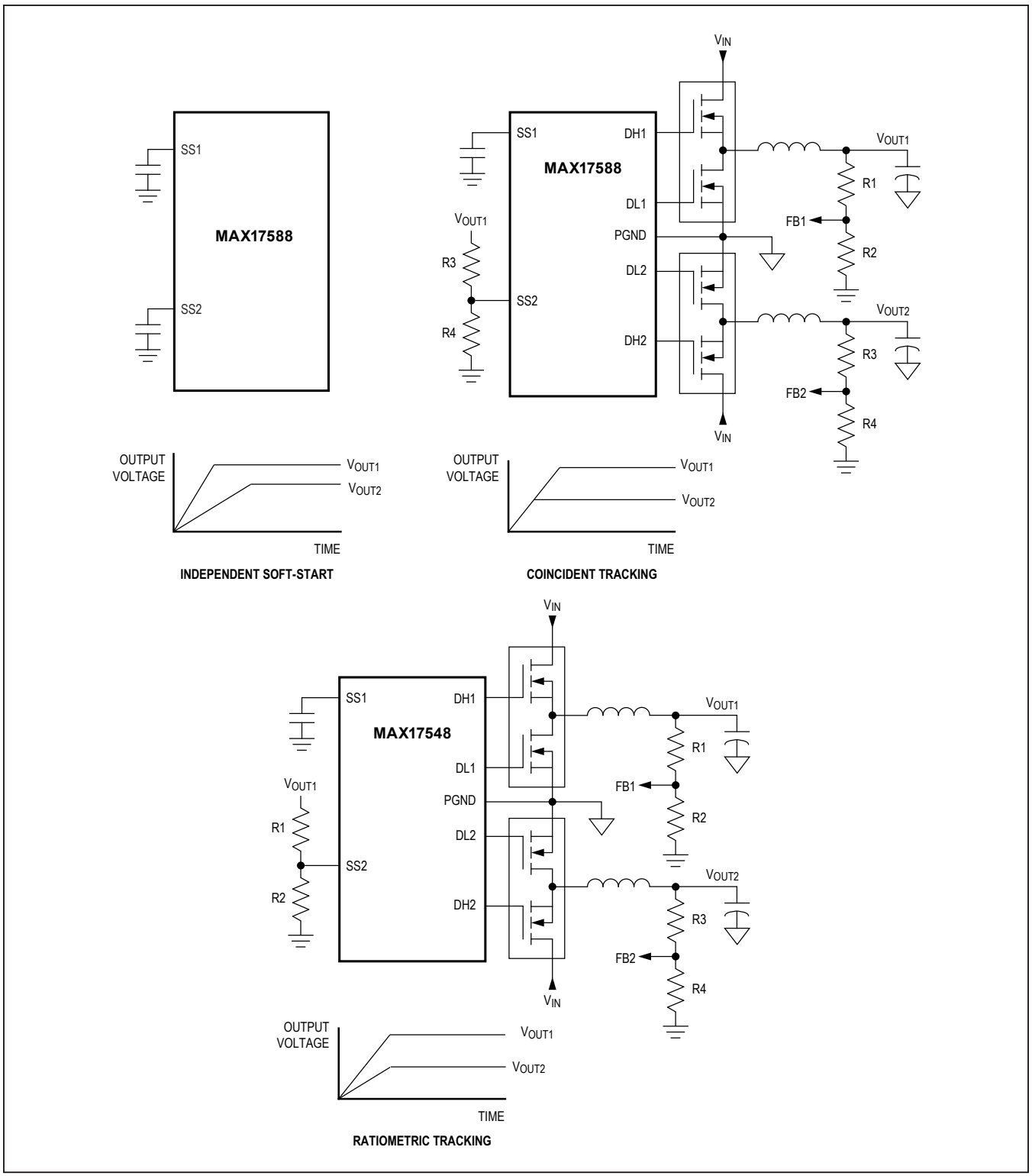


Figure 2. Possible SS_ Pin Configurations

Light-Load Current Operation (SKIP)

The MAX17548 can be configured to operate either in discontinuous-conduction (DCM) mode for high light-load efficiency or fixed-frequency pulse-width-modulation (PWM) mode. To select DCM mode of operation, connect the SKIP pin to a DC voltage between 1.25V and V_{CCINT} - 1.5V. To select PWM mode of operation, connect SKIP to V_{CCINT}.

DCM Mode

In DCM mode, the IC turns off the low-side MOSFET of the regulator close to the zero-crossing of the inductor current in each switching cycle. This operation minimizes negative current in the inductor, reducing loss due to current flowing from the output to the input. Therefore, the inductor current in each cycle is a triangular waveform whose peak is proportional to the load current demand. The controller operates at a constant frequency while adjusting the peak current in the inductor for load and input-voltage variations. However, under light-load and/or high input-voltage conditions, there exists a minimum on-time constraint for the controller. The minimum on-time is the smallest controllable pulse width that the controller can generate. This imposes a lower limit on the peak inductor current that can be programmed in the inductor and causes a fixed amount of energy to be delivered to the output, regardless of the energy requirement of the load. If the load is such that the amount of energy delivered during minimum on-time is more than the load energy, the output voltage rises above its nominal set value. This results in skipping of switching cycles to regulate the average output voltage to the set point. This operation results in an effective switching frequency that is lower than the programmed switching frequency, which improves the regulator efficiency. As the load current increases to a point where the valley of the inductor current rises above zero, the regulator operation moves into PWM mode.

PWM Mode

Each controller of the device operates in PWM mode whenever SKIP is connected to V_{CCINT}. The inductor current is allowed to go negative in this mode. In PWM mode, under normal operating conditions, the high-side MOSFET turns on at an edge of the internal clock. An internal error amplifier compares the feedback voltage at the FB_ pin to a fixed internal reference voltage and generates an error current. This error current flows through the compensation network at the COMP_ pin and generates control voltage for the inner current loop. The on-time of the high-side MOSFET in a switching cycle is determined by comparing the control voltage at the COMP_ pin with the sum of the current-sense voltage at CS_+, CS_-, and the internal slope-compensation voltage. The inductor current ramps up during high-side MOSFET turn-on time. Once the high-side MOSFET is turned off, the low-side MOSFET is turned on. During low-side MOSFET turn-on time, the inductor current ramps down. The low-side MOSFET remains on until the next clock edge. PWM mode of operation has the advantages of low output-voltage ripple and constant-frequency operation, which is beneficial in applications that are sensitive to operating frequency. Under minimum on-time conditions described in the *DCM Mode* section, the device skips high-side turn-on events in PWM mode also, to regulate the output voltage. This results in low-frequency operation with regard to inductor current and output-voltage-ripple waveforms.

Frequency Selection (RT)

The selection of switching frequency is a tradeoff between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching losses and gate-drive losses, but requires a larger inductor and/or capacitor to maintain low output-ripple voltage. The switching frequency of the device can be programmed between 100kHz and 2.2MHz using the RT pin. Connect RT to V_{CCINT} to program a default frequency of 535kHz switching frequency, and to GND to program 350kHz switching frequency. Figure 3 shows the switching frequency for different RT values.

The following formula can be used to find the required resistor for a given switching frequency.

$$R_{RT} = \frac{f_{SW} + 133}{8.8}$$

0 to 180° Phase Operation

The IC allows the user to configure the phase shift between the two output channels of the device. Table 1 gives selectable phase-shift configurations based on SEL_PH.

The advantages of operation with 180° phase shift between channels are:

- Reduction of input and output capacitor RMS current.
- Lower input-voltage ripple.

Table 1. Configuring Phase Shift Using SEL_PH

SEL_PH	LX1/LX2 PHASING
V_{CCINT}	0°/0°
Open	0°/180°

Output Overvoltage Protection

The output overvoltage-protection circuit protects the load under output overvoltage conditions. If the output voltage rises by more than 10% of its nominal value, the high-side MOSFET is turned off until the overvoltage condition clears.

The state of the low-side MOSFET during output overvoltage conditions depends on the selected operating mode. If PWM mode of operation is selected, the low-side MOSFET remains on until the output overvoltage condition clears. In this case, the current through the low-side MOSFET can reach a large value depending on the amount of overvoltage and output capacitance. If DCM mode of operation is selected, the low-side MOSFET is turned off whenever inductor current reaches zero. In this mode, the low-side MOSFET is turned on every 10 clock cycles to refresh the BST_ capacitor. This causes a slightly negative average inductor current that, in addition to the load current present, can slowly discharge the output.

Power-Good (PGOOD1 and PGOOD2) Pins

The IC features independent open-drain power-good (PGOOD1, PGOOD2) pins. The PGOOD_ pins pull low when the corresponding FB_ pin voltage is outside ±10% of the 0.8V reference voltage. During soft-start, PGOOD_ is low. When the FB_ pin voltage is within -10% of the reference voltage, PGOOD_ can be pulled up by an external resistor to a source voltage no greater than 6V.

Foldback Current Limit

Under overload conditions, when the output voltage falls to less than 70% of its nominal level, foldback current limiting is activated. In this mode, the peak inductor current is progressively lowered from 100% to 50% of programmed value, in proportion to the FB_ voltage. Foldback current-limit mode is disabled during the soft-start duration.

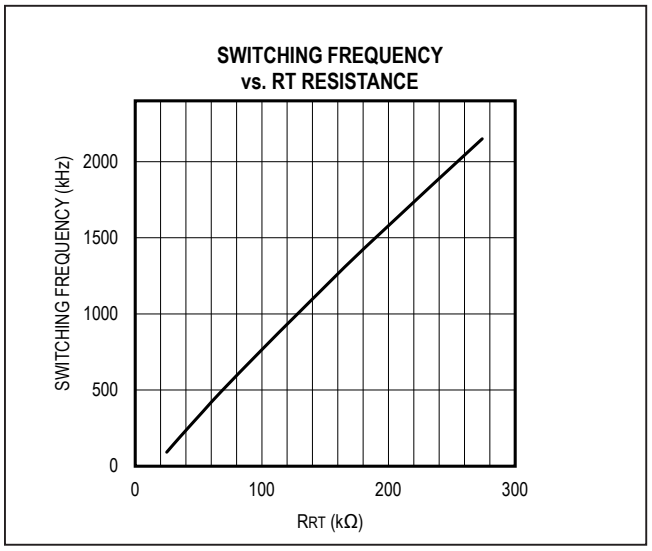


Figure 3. RT vs. Switching Frequency

Peak Current-Limit Programming (ILIM)

The IC provides cycle-by-cycle peak current limiting based on the ILIM pin setting. ILIM is a three-level logic input. Table 2 gives cycle-by-cycle peak positive current-limit thresholds based on the ILIM pin configuration.

The internal current-sense amplifier gain depends on the ILIM pin configuration. Table 3 gives current-sense amplifier gain for different ILIM pin configurations.

Under overload or short-circuit conditions, the IC regulates the cycle-by-cycle peak current-sense voltage across the current-sense pins to the peak current-limit threshold set using the ILIM pin until output voltage falls to approximately 70% of its nominal value. If the output voltage falls below 70% of its nominal value, foldback current-limit operation commences, where the peak current-limit threshold is lowered proportional to the fall in the output voltage, as measured at the FB_ pin.

Startup Into Prebiased Output

The IC supports monotonic startup into a prebiased output voltage. During startup, if the FB_ pin voltage is higher than the SS_ pin voltage, the high-side MOSFET is held off and the low-side MOSFET is turned on for a duration of 150ns for every 10 clock cycles to refresh the BST_ capacitor. This causes a slightly negative average inductor current that can slowly discharge the output. Once the SS_ pin voltage reaches FB_ voltage, normal soft-start

Table 2. Peak Current-Limit Thresholds for Different ILIM Settings

ILIM PIN CONFIGURATION	POSITIVE CURRENT-LIMIT THRESHOLD (TYP)
V_{CCINT}	75mV
Open	50mV
GND	30mV

Table 3. Current-Sense Amplifier Gain for Different ILIM Settings

ILIM PIN CONFIGURATION	CURRENT-SENSE AMPLIFIER GAIN
V_{CCINT}	13.3
Open	20
GND	33.3

operation occurs, and the output voltage smoothly ramps up from the prebiased value.

Operating Input Voltage Range

For a step-down converter, the minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN_MIN} = \frac{V_{OUT} + I_{LOAD(MAX)} \times (R_{DS(ON)_LOW} + DCR)}{1 - f_{SW_MAX} \times t_{OFF_MIN}} + I_{LOAD(MAX)} \times (R_{DS(ON)_HI} - R_{DS(ON)_LOW})$$

$$V_{IN_MAX} = \frac{V_{OUT}}{(f_{SW_MAX} \times t_{ON_MIN})}$$

where V_{OUT} is the steady-state output voltage, $I_{LOAD(MAX)}$ is the maximum load current, DCR is the DC resistance of the inductor, f_{SW_MAX} is the maximum switching frequency, $R_{DS(ON)_HI}$ are the on-state resistances of the high-side and low-side MOSFETs, t_{OFF_MIN} is the worst-case minimum off-time (160ns), and t_{ON_MIN} is the worst-case minimum on-time (155ns) from the Electrical Characteristics table.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature of the device exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing it to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. The device restarts with soft-start when recovering from thermal shutdown.

Applications Information

Setting the Input Undervoltage-Lockout Level

The EN_ pins can be used as input undervoltage-lockout detectors with a typical hysteresis of 100mV. As shown in Figure 1, the input voltage at which each controller of the IC turns on, can be set with a resistor-divider connected to corresponding EN_ from IN to GND.

Select R2 = 10kΩ and calculate R1 based on the following equation:

$$R1 = R2 \times \frac{(VIN_{UVLO} - 1.25)}{1.25}$$

where VIN_{UVLO} is the input voltage at which the controller should be enabled.

Setting the Output Voltage

The output voltage of each controller is set by connecting a resistor-divider to FB_ from the corresponding output to GND (Figure 4). Select R1 using the following equation, based on the offset introduced on the output voltage by the FB_ leakage. Let α be the offset introduced on the output voltage:

$$R1 \le \frac{\alpha}{I_{FB_}}$$

where $I_{FB_}$ is the FB_ leakage current (±100nA max). For example, for V_{OUT} = 5V, α = 0.1% of V_{OUT} (= 5mV).

$$R1 \le \frac{5mV}{0.1\mu A}$$

R1 ≤ 50kΩ

Calculate R2 with the following equation:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{0.8} - 1\right)}$$

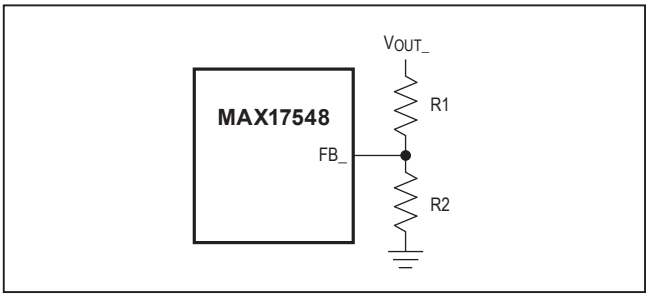


Figure 4. Output-Voltage Programming

Soft-Start Capacitor

Soft-start time is programmed by connecting a capacitor from the SS_ pin to GND. An internal 5µA current source charges the capacitor at the SS_ pins providing a linear ramping voltage for output-voltage reference. The soft-start time is calculated based on the following equation:

$$t_{SS} = C_{SS} \times \frac{0.8\,V}{5\mu A}$$

Inductor Selection

Three key inductor parameters must be specified to select output inductor:

1) Inductance (L).
2) Inductor saturation current (I_{SAT}).
3) DC resistance of inductor (DCR).

The required inductance (L) is calculated based on the ratio of inductor peak-to-peak ripple AC current to its DC average current (LIR). A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

$$L = \frac{V_{OUT} \times (1 - D)}{LIR \times I_{LOAD} \times f_{SW}}$$

where V_{OUT} is the output voltage, D is the operating duty cycle (= V_{OUT}/V_{IN}), I_{LOAD} is the full-load current, and f_{SW} is the operating switching frequency.

The minimum inductor saturation current should be equal to or greater than maximum inductor peak current given by the following equation:

$$\text{Maximum Inductor Peak Current} = \text{Maximum Load Current} + \Delta I_{LPK\text{-}PK}(max)$$

where $\Delta I_{LPK\text{-}PK}(max)$ is the maximum inductor ripple current and can be calculated as follows:

$$\Delta I_{LPK-PK}(max) = \frac{V_{OUT} \times \left[1 - \frac{V_{OUT}}{V_{INMAX}}\right]}{L \times f_{SW}}$$

Selecting an inductor with lower DCR improves efficiency, but there is a lower limit for DCR based on the minimum peak-to-peak current-sense signal required at the current-sense pins, as described in the *Current Sensing (CS_+ and CS_-)* section.

Current Sensing (CS_+ and CS_-)

The CS_+ and CS_- pins are the inputs to the internal current-sense amplifiers. The common-mode operating voltage range on these pins is 0 to 24V, enabling the IC to regulate output voltages up to a nominal 24V.

Whether the current sensing is done by an external current-sense resistor or inductor DCR, the desired current-sense resistance is calculated using the following equation:

$$R_{SENSE} = \frac{V_{CS}}{I_{LOAD(MAX)} + \frac{\Delta I_{LPK\text{-}PK}(max)}{2}}$$

where:

R_{SENSE} is the desired current-sense resistor,

V_{CS} is the selected current-limit threshold based on ILIM pin setting,

$I_{LOAD(MAX)}$ is the maximum load current.

To ensure that the application delivers full-load current over the full operating temperature range, select the minimum value for the V_{CS} parameter from the *Electrical Characteristics* table.

It should be noted that the magnitude of current-sense ripple voltage is critical for a good signal-to-noise ratio to ensure minimum duty-cycle jitter. The worst-case current-sense ripple voltage occurs at minimum operating input voltage, and should be set in the 7mV to 12mV range. The following equation can be used to calculate the worst-case current-sense ripple voltage at the CS_+, CS_- pins:

$$\Delta V_{CSmin} = \Delta I_{LPK-PK}(min) \times R_{SENSE}$$

where $\Delta I_{LPK\text{-}PK(min)}$ is the minimum inductor current ripple, which occurs at minimum operating input voltage. $\Delta I_{LPK\text{-}PK(min)}$ can be calculated using the following equation:

$$\Delta I_{LPK-PK}(min) = \frac{V_{OUT} \times \left[1 - \frac{V_{OUT}}{V_{INMIN}}\right]}{L \times f_{SW}}$$

If ΔV_{CSMIN} is less than the target value, the selected output inductance should be lowered, and R_{SENSE} should be iteratively recalculated until ΔV_{CSMIN} is equal to or greater than the target value (7mV to 10mV, depending on PCB layout), and V_{CSMAX}, as calculated by the following equation is less than the selected V_{CS} from the *Electrical Characteristics* table.

$$V_{CSMAX} = R_{SENSE} \times \left[I_{LOADMAX} + \frac{\Delta I_{LPK-PK}(max)}{2} \right]$$

Because of PCB layout-related noise, operation at the minimum operating voltage should be checked for jitter before finalizing the worst-case current-sense voltage. Care should be taken to ensure that current-sense filter components should be placed close to the IC's current-sense pins. The current-sense traces should be short and differentially routed.

Current Sensing Using an External Sense Resistor

A typical current-sensing circuit using a discrete resistor is shown in Figure 5. The power rating of R_{SENSE} should be selected using the following equation for dissipation in R_{SENSE}:

$$\text{Power losses in } R_{SENSE} = \left[I_{LOAD}^{2} + \left(\frac{\Delta IL^{2}}{12} \right) \right] \times R_{SENSE}$$

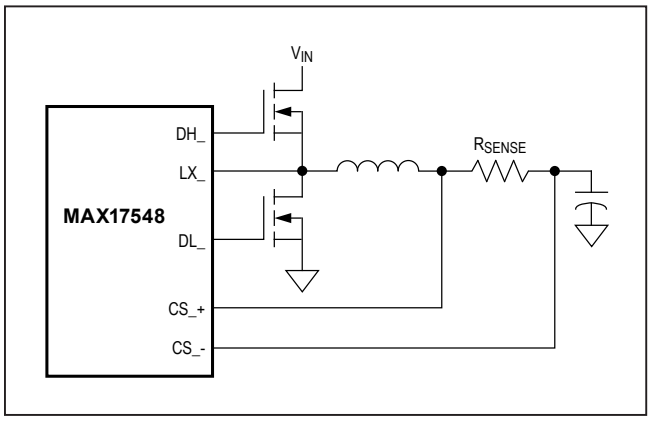


Figure 5. Current Sensing Using an External Sense Resistor

Current Sensing Using Inductor DCR

Current sensing using inductor DCR current improves the system efficiency compared to current sensing using an external sense resistor. The disadvantage of DCR current sensing is that the current limit is not as accurate in comparison to the sense resistor because of wider variation of inductor DCR over temperature, and initial tolerance specified by manufacturers. A typical DCR current-sensing circuit is shown in Figure 6. Place C1 across the CS_ pins. Usually C1 is selected in the 0.1µF to 0.47µF range. Calculate R1 (if R2 is not used) based on following equation:

$$R1 = \frac{L}{DCR \times C1}$$

R2 is used in applications where DCR of inductor is greater than the desired current-sense resistance. In this case, calculate R1 and R2 using the following equation:

$$RP = \frac{L}{DCR \times C1}$$

where RP is the parallel combination of R1 and R2 (= [R1 x R2]/[R1 + R2]).

$$R1 = \frac{DCR \text{ x } RP}{R_{SENSE}}$$

$$R2 = \frac{R1 \times RP}{R1 - RP}$$

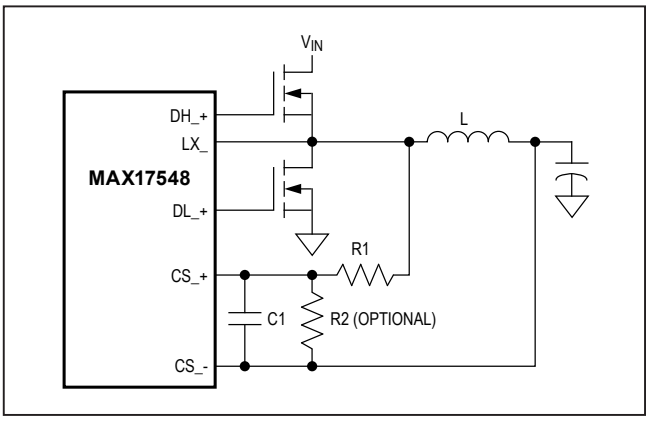


Figure 6. Typical Current Sensing Using Inductor DCR Current

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. Use low-ESR ceramic capacitors at the input. For each output channel, calculate the input capacitance required for a specified input-ripple ΔV_{IN} using the following equations, by neglecting the ripple component due to ESR of input capacitor:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1-D)}{\eta \times \Delta V_{IN} \times f_{SW}}$$

where D = (V_{OUT}/V_{IN}), η is efficiency of power conversion.

The input capacitor RMS current requirement (CIN_{RMS}) can be calculated by the following equation:

$$CIN_{RMS} = I_{LOAD(MAX)} \times \sqrt{D \times (1-D)}$$

where $I_{LOAD(MAX)}$ is the maximum value of load current, D = V_{OUT}/V_{IN}.

Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output-ripple voltage, and transient response. The steady-state output ripple (ΔV_{OUTSS}) has two components (by neglecting the ESL of the output capacitors): one component is due to the voltage drop across the ESR (ΔV_{OUTESR_SS}) and the other component is due to the variation in charge stored in the output capacitor (ΔV_{OUTQ_SS}). By neglecting the output-voltage drop due to ESL of output capacitor, approximate output voltage ripple under steady state is given by:

$$\Delta V_{OUTSS} \approx \Delta V_{OUTESR_SS} + \Delta V_{OUTQ_SS}$$

where ΔV_{OUTSS} is the output-voltage ripple under steady state:

$$\Delta V_{OUTESR_SS} = \Delta IL_{PK-PK} \times ESR$$

$$\Delta V_{OUTQ_SS} = \frac{\Delta IL_{PK-PK}}{8 \times f_{SW} \times C_{OUT}}$$

Calculate the required C_{OUT} and ESR based on the above equations. For ceramic output capacitors, V_{OUTQ_SS} contributes to approximately 80% of the total output-ripple voltage, ΔV_{OUTQSS_SS}. For electrolytic output capacitors, ΔV_{OUTQ_SS} contributes approximately 50% of the total output-voltage ripple. Low-ESR capacitors should be used.

Loop Compensation

The IC uses an internal transconductance error amplifier with its inverting input and output available to the user for external frequency compensation. The output capacitor and compensation network determine the loop stability for a given output inductor and output capacitor.

The controller uses a peak current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor. Current-mode control eliminates the double pole in the feedback loop caused by the inductor and output capacitor in the case of voltage-mode control, resulting in a smaller phase shift and requiring less elaborate error-amplifier compensation.

Typical type-2 compensation used with peak current-mode control is shown in Figure 7. Calculate the compensation resistor (R_Z) using the following equation:

$$R_Z = \frac{2 \times \pi \times f_{CO} \times C_{OUT} \times G_{CS} \times R_{SENSE}}{g_M \times G_{FB}}$$

where:

f_{CO} is the desired crossover frequency that should be chosen between $f_{SW}/10$ and $f_{SW}/20$,

C_{OUT} is the output capacitance,

G_{CS} is the current-sense amplifier gain, which depends on the ILIM setting,

R_{SENSE} is the effective current-sense resistor across the CS_+ and CS_- pins,

g_M is the internal transconductance amplifier gain,

G_{FB} is the output-voltage feedback divider gain, which is equal to (0.8V/output voltage).

C_Z is calculated using the following equation:

$$C_Z = \frac{1}{2 \times \pi \times f_{P_Load} \times R_Z}$$

where F_{P_Load} is the load-pole frequency approximated by the following equation:

$$f_{P_Load} = \frac{1}{2 \times \pi \times C_{OUT} \times \left(\frac{V_{OUT}}{I_{LOAD}}\right)}$$

Calculate C_F using the following equation:

$$C_F = \frac{1}{2 \times \pi \times R_Z \times f_{P_EA}}$$

where f_{P_EA} is the pole frequency created by R_Z and C_F given by the minimum of ESR zero frequency calculated by the following equation or $f_{SW}/2$:

$$f_{Z_ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR}$$

When the output capacitor is composed of n identical capacitors in parallel, the resulting C_{OUT} = n x C_{OUT} (each), and ESR = ESR (each)/n. Note that the location of f_{Z_ESR} for a parallel combination of same capacitors is the same as for an individual capacitor.

Bootstrap Capacitor Selection

The selected high-side nMOSFET determines the appropriate bootstrap capacitance values according to the following equation:

$$C_{BST} = \frac{\Delta Q_{Gate}}{\Delta V_{BST}}$$

where ΔQ_{Gate} is the total gate charge of the high-side MOSFET and ΔV_{BST} is the voltage variation allowed on the high-side MOSFET driver after turn-on. Choose ΔV_{BST} so the available gate-drive voltage is not significantly degraded (e.g., ΔV_{BST} = 100mV) when determining C_{BST}. The bootstrap capacitor should be a low-ESR ceramic capacitor. A minimum value of 100nF is recommended.

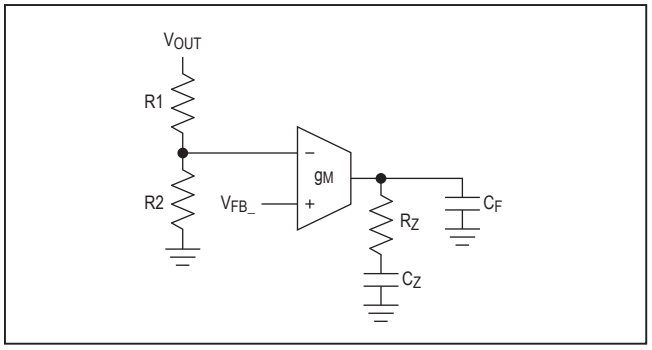


Figure 7. Typical Type-2 Compensation Network

MOSFET Selection

Each controller drives two external logic-level n-channel MOSFETs as the circuit switch elements. The key selection parameters to choose these MOSFETs include:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage (V_{DS}(MAX))
- Miller Plateau voltage on HSMOSFET Gate (V_{MIL})
- Total gate charge (Q_{Gate})
- Output capacitance (C_{OSS})
- Power-dissipation rating and package thermal resistance

Both nMOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. The duty cycles for the high-side and low-side external MOSFETs can be calculated as follows:

High-side MOSFET duty cycle:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Low-side MOSFET duty cycle = 1 - D

High-side MOSFET losses can be approximated using the following formula:

$$P_{HSMOSFET} = P_{HSMOSFET_Conduction} + P_{HSMOSFET_Switching}$$

$$P_{HSMOSFET_Conduction} = I_{LOAD(MAX)}^2 \times R_{DS(ON)} * D$$

$$P_{HSMOSFET_Switching} = f_{SW} \times \left\{ \left[\frac{V_{IN} \times I_{LOAD(MAX)}}{2} \times \frac{Q_{SW} \times R_{DR}}{V_{CCINT} - V_{MIL}} \right] + [V_{IN} \times Q_{rr}] + \left[(1/2) \times C_{OSSHS} \times V_{IN}^2 \right] + \left[(1/2) \times C_{OSSLS} \times V_{IN}^2 \right] \right\}$$

where:

f_{SW} is the operating switching frequency,
$I_{LOAD(MAX)}$ is the maximum load current in the application,
Q_{SW} is the switching charge of the high-side MOSFET, which can be obtained from the MOSFET data sheet,
R_{DR} is the sum of the DH_ pin driver resistance and the HSMOSFET internal gate resistance,

V_{MIL}- V_{GS} on HSMOSFET gate that produces I_{DS} = $I_{LOAD(MAX)}$

Q_{rr} is the reverse-recovery charge of low-side MOSFET body diode (if external Schottky is not placed across low-side MOSFET),

C_{OSSHS} is the effective output capacitance of the high-side MOSFET,

C_{OSSLS} is the effective output capacitance of the low-side MOSFET.

Low-side MOSFET losses can be approximated using the following formula:

$$P_{HSMOSFET} = I_{LOAD(MAX)}^2 \times R_{DS(ON)} \times (1-D) + V_D \times I_{LOAD(MAX)} \times t_{DT} \times f_{SW}$$

where V_D is the forward-drop of the LSMOSFET body diode and t_{DT} is the dead time from the Electrical Characteristics table.

Take the $R_{DS(ON)}$ variation with temperature into account while calculating the above losses and ensure that the losses of each MOSFET do not exceed their power rating. Using a low Q_{rr} Schottky diode across the low-side MOSFET reduces the high-side MOSFET losses.

Power Dissipation within the MAX17548

Gate-charge losses are dissipated by the drivers. Therefore, the gate-driver current taken from the internal LDO regulator and resulting power dissipation must be checked. If V_{CCEXT} is not used to power V_{CCINT}, calculate the approximate IC losses as follows:

$$P_{MAX17558} = V_{IN} \times [(Q_{Gate} \times f_{SW}) + I_{IN}]$$

If V_{CCEXT} is used to power the V_{CCINT}, use the following equation to calculate the approximate IC losses:

$$P_{MAX17558} = V_{CCEXT} \times [(Q_{Gate} \times f_{SW}) + I_{IN}]$$

where:

Q_{Gate} = Total gate charge of high-side and low-side MOSFETs of controller1 + total gate charge of high-side and low-side MOSFETs of controller 2,

I_{IN} is the supply current given in the *Electrical Characteristics* table.

Calculate the IC junction temperature using the following equation and ensure that this value does not exceed +125°C:

$$T_J = [P_{MAX17558} \times Rth_{JA}] + T_A$$

where:

T_J is the IC junction temperature,

$P_{MAX17548}$ is the power losses in the IC,

Rth_{JA} is the IC junction-to-ambient thermal resistance, which is typically 29°C/W for a multilayer board,

T_A is the maximum ambient temperature.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low losses, low output noise, and clean and stable operation. Use the following guidelines for PCB layout:

- Keep input bypass capacitors as close as possible across the drain of the high-side MOSFET and source of the low-side MOSFET.
- If external Schottky diodes are used across the low-side MOSFET, keep the Schottky very close and right across the low-side MOSFET.
- Keep IN, V_{CCINT}, V_{CCEXT} bypass capacitors and BST_ capacitors nearer to IC pins.
- Route high-speed switching nodes (BST_, LX_, DH_, and DL_) away from the sensitive analog areas (RT, COMP_, CS_, and FB_).
- The gate current traces must be short and wide. Use multiple small vias to route these signals if routed from one layer of the PCB to another layer.
- Route current-sense lines parallel, short, and next to each other to minimize the loop formed by these lines.
- Keep current-sense filter capacitors nearer to IC current-sense pins and on the same side of the IC.
- Group all GND-referred and feedback components close to the IC.
- Keep the FB_ and compensation-network nets as small as possible to prevent noise pickup.
- If possible, place all power components on the top side of the board and run the power-stage currents using traces or copper fills on the top side only, without adding vias.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz or higher) to enhance efficiency and minimize trace inductance and resistance.
- On the top side, lay out a large PGND copper area for the output and connect the bottom terminals of the input bypass capacitors, output capacitors, and the source terminals of the low-side MOSFET to that area.
- Refer to the MAX17548 evaluation kit data sheet PCB layout for an example.

Typical Application Circuits

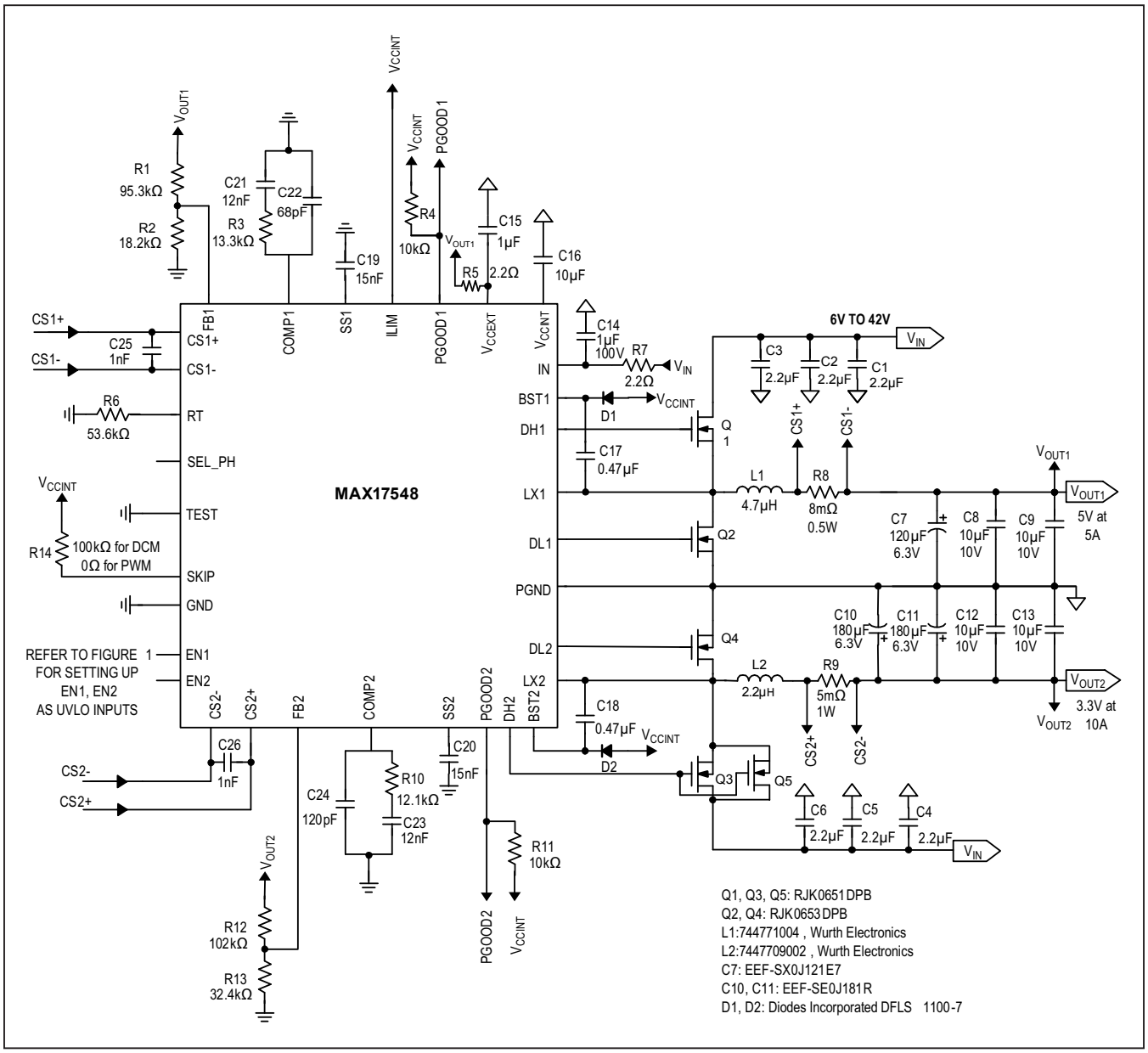


Figure 8. Wide-Input Voltage, High-Efficiency, 5V and 3.3V Output Buck Converter with Resistor-Based Current Sensing (R8, R9).

Typical Application Circuits (continued)

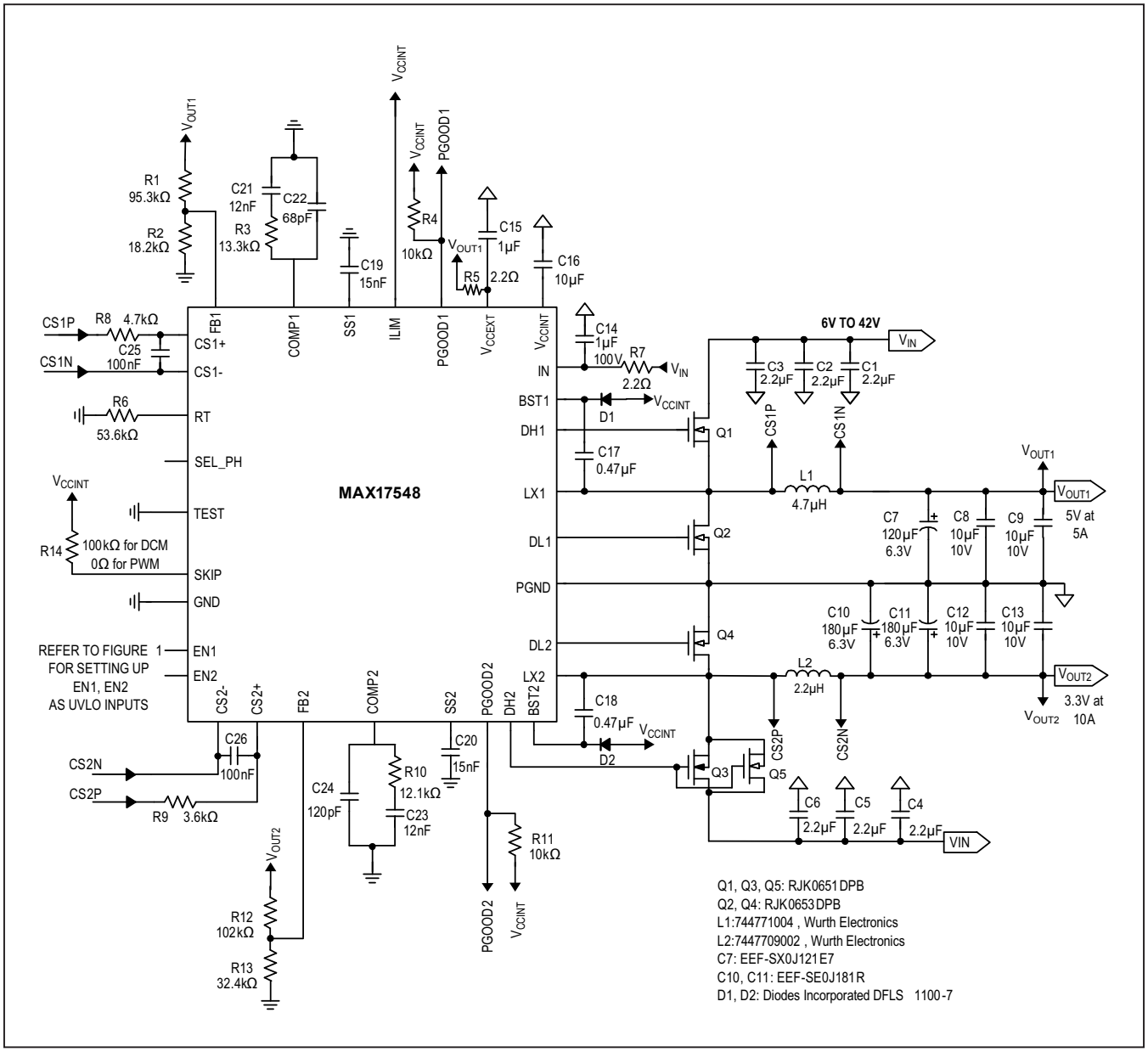


Figure 9. Wide Input Voltage, High-Efficiency, 5V and 3.3V Output Buck Converter with Inductor DCR Current Sensing (L1, L2).

Typical Application Circuits (continued)

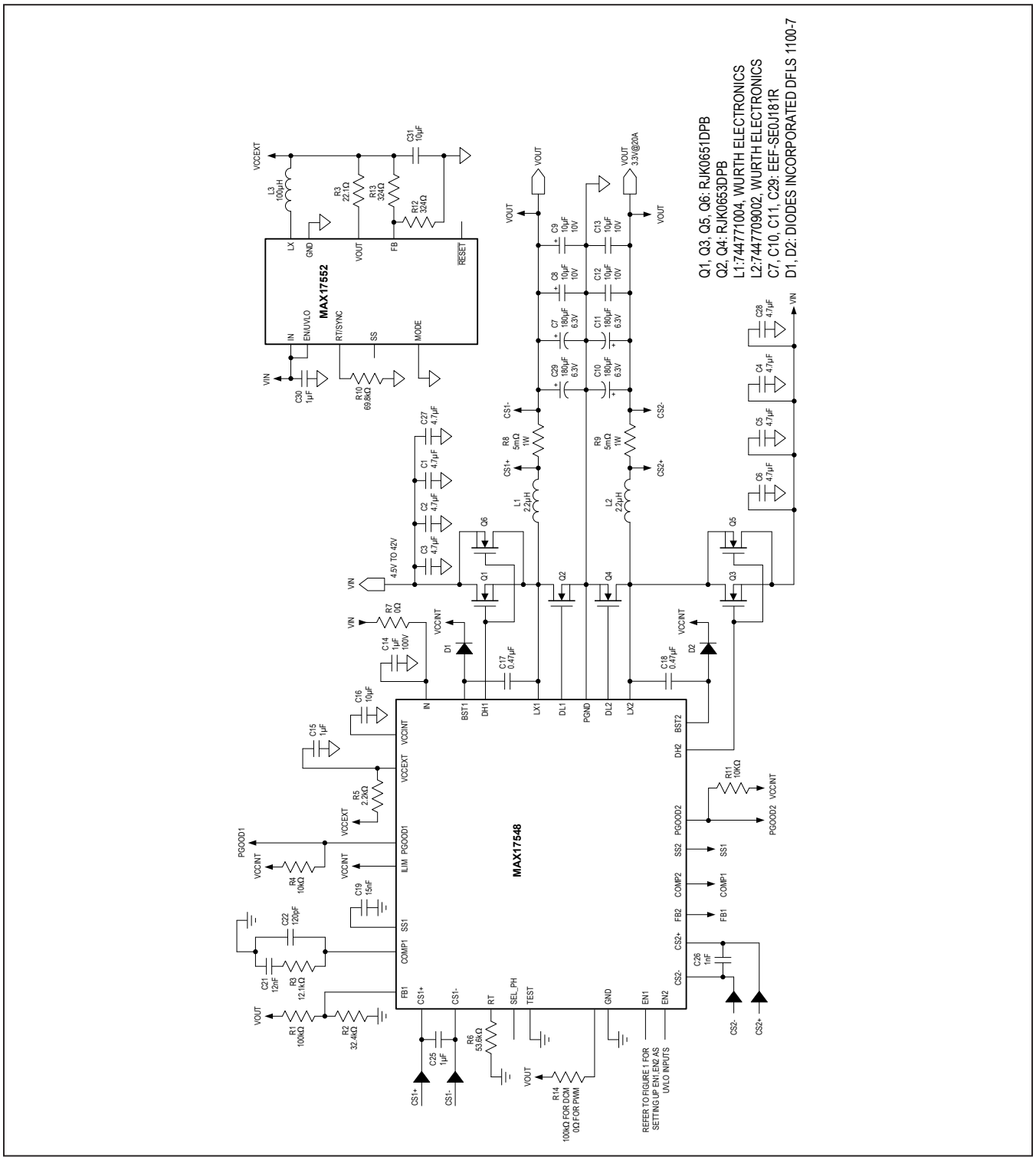


Figure 10. Wide Input Voltage, High-Efficiency, Dual-Phase, 3.3V, 20A Output Buck Converter with Resistor-Based Current Sensing

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+4	21-0140	90-0012

Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX17548ATJ+	-40°C to +125°C	32 TQFN-EP* (5mm x 5mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/17	Initial release	—

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