HD151BF854

2.5 V PLL Clock Buffer for DDR Application

REJ03D0809-0500
(Previous: ADE-205-696D)
Rev.5.00
Apr 07, 2006

Not recommend for new design

Description

The HD151BF854 is a high-performance, low-skew, low-jitter, PLL clock buffer. It is specifically designed for use with DDR (Double Data Rate) PC motherboard application.

Features

- Designed for DDR200/266/333/400 PC mother board clock buffering
- Supports 60 MHz to 210 MHz operation range
- Distributes one to six differential clock outputs pairs
- Spread spectrum clock compatible
- External feedback pin (FBIN) is used to synchronize the outputs to the clock input
- Supports 2.5 V analog supply voltage (AVDD), and 2.5 V VDD
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD151BF854SSEL	SSOP-28 pin	PRSP0028JA-A (FP-28DSAV)	SS	EL (1,000 pcs / Reel)

Key Specifications

- Supply voltages: VDD = AVDD = 2.5 V±0.2 V
- Output clock cycle to cycle jitter = ±75 ps
- Output clock pin to pin skew = 150 ps

Function Table

Inputs		Outputs			PLL
AVDD	CLK	Yn	$\overline{Yn}$	FBOUT	
GND	L	L	H	L	Bypass / Off
GND	H	H	L	H	Bypass / Off
2.5 V (typ.)	L	L	H	L	Running
2.5 V (typ.)	H	H	L	H	Running

H: High level
L: Low level

Pin Arrangement



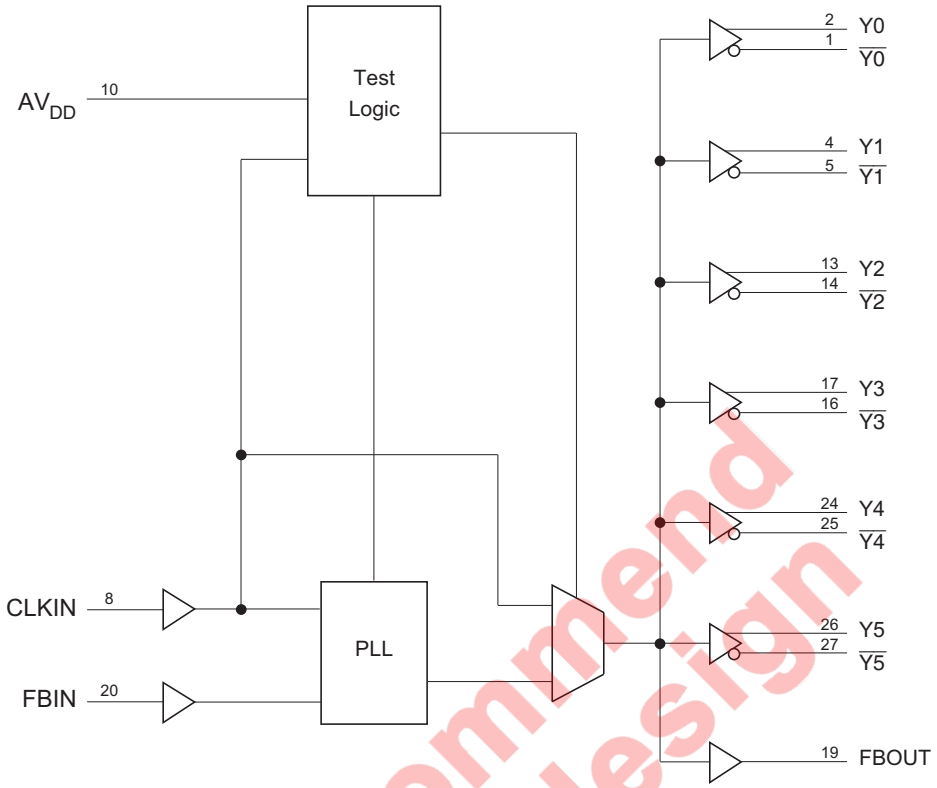
(Top view)

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Pin Functions

Pin name	No.	Type	Description
AGND	11	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AVDD	10	Power	Analog power supply. AVDD provides the power reference for the analog circuitry. In addition, AVDD can be used to bypass the PLL for test purposes. When AVDD is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
CLKIN	8	Input	Clock input. CLKIN provides the clock signal to be distributed by the HD151BF854 clock buffer. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	20	Input	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLKIN and FBIN so that there is nominally zero phase error between CLKIN and FBIN.
FBOUT	19	Output	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
GND	6, 15, 28	Ground	Ground
VDD	3, 12, 23	Power	Power supply
Y	2, 4, 13, 17, 24, 26	Output	Clock outputs. (+Clock) These outputs provide low-skew copies of CLK.
$\overline{Y}$	1, 5, 14, 16, 25, 27	Output	Bar clock outputs. (–Clock) These outputs provide low-skew copies of CLK.
NC	7, 9, 18, 21, 22	NC	Don't connect any VDD or GND.

Logic Diagram



Note: All inputs and outputs are associated with V_{DDQ} = 2.5 V.

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Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	VDD	–0.5 to 3.6	V	
Input voltage	V_{IC}	–0.5 to 3.6	V	CLKIN
	V_I	–0.5 to VDD+0.5	V	
Output voltage *[1]	V_O	–0.5 to VDD+0.5	V	
Input clamp current	I_{IK}	–50	mA	V_I < 0
Output clamp current	I_{OK}	–50	mA	V_O < 0
Continuous output current	I_O	±50	mA	V_O = 0 to VDD
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	AVDD	2.3	2.5	2.7	V	
Output supply voltage	VDD	2.3	2.5	2.7	V	
DC input signal voltage		–0.3	—	VDD+0.3	V	All pins
High level input voltage	V_{IH}	1.7	—	3.6	V	CLKIN
High level input voltage	V_{IH}	1.7	—	VDD+0.3	V	FBIN
Low level input voltage	V_{IL}	–0.3	—	0.7	V	CLKIN, FBIN
Output differential cross point voltage	V_{OX}	0.5×VDD –0.2	—	0.5×VDD +0.2	V	
Output current	I_{OH}	—	—	–12	mA	
	I_{OL}	—	—	12		
Input clock slew rate	SR	1	—	—	V/ns	
Operating temperature	T_a	0	—	70	°C	

Note: Unused inputs must be held high or low to prevent them from floating.

Electrical Characteristics

Item	Symbol	Min	Typ *[1]	Max	Unit	Test Conditions
Input clamp voltage (All inputs)	V_{IK}	—	—	–1.2	V	I_I = –18 mA, VDD = 2.3 V
Output voltage	V_{OH}	VDD–0.2	—	—	V	I_{OH} = –100 µA, VDD = 2.3 to 2.7 V
		1.7	—	VDD		I_{OH} = –12 mA, VDD = 2.3 V
	V_{OL}	—	—	0.2		I_{OL} = 100 µA, VDD = 2.3 to 2.7 V
		—	—	0.6		I_{OL} = 12 mA, VDD = 2.3 V
Input current	I_I	–10	—	10	µA	V_I = 0 V or 2.7 V, VDD = 2.7 V, CLKIN, FBIN
Analog supply current	AI_{CC}	—	—	12	mA	VDD = AVDD = 2.7 V, 170 MHz
Dynamic supply current	DI_{CC}	—	250	300	mA	VDD = AVDD = 2.7 V, 170 MHz, All Yn, $\overline{Yn}$, = open
Input capacitance*[2]	C_I	2.5	—	3.5	pF	CLKIN and FBIN
Delta input capacitance*[2]	C_{DI}	–0.25	—	0.25	pF	

Notes: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
2. Target of design, not 100% tested in production.

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Switching Characteristics

Ta = 25°C, VDD = AVDD = 2.5V

Item	Symbol	Min	Typ	Max	Unit	Test Conditions & Notes
Period jitter	t_{PER}	—	|75|	—	ps	*7, 8
Half period jitter	t_{HPER}	—	|120|	—	ps	*8
Cycle to cycle jitter	t_{CC}	—	|75|	—	ps	
Static phase offset	t_{sPE}	—	|150|	—	ps	*4, 5
Output clock skew	t_{sk}	—	150	—	ps	
Operating clock frequency	$f_{CLK(O)}$	60	—	210	MHz	*1, 2
Application clock frequency	$f_{CLK(A)}$	80	166	210	MHz	*1, 3
Slew rate		1.0	—	2.0	V/ns	20% to 80%
Stabilization time		—	—	0.1	ms	*6

Notes: Target of design, not 100% tested in production.

1. The PLL must be able to handle spread spectrum induced skew. (the specification for this frequency modulation can be found in the latest Intel PC100 Registered DIMM specification)
2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4. Assumes equal wire length and loading on the clock output and feedback path.
5. Static phase offset does not include jitter.
6. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal after power on.
7. Period jitter defines the largest variation in clock period, around a nominal clock period.
8. Period jitter and half period jitter are separate specifications that must be met independently of each other.

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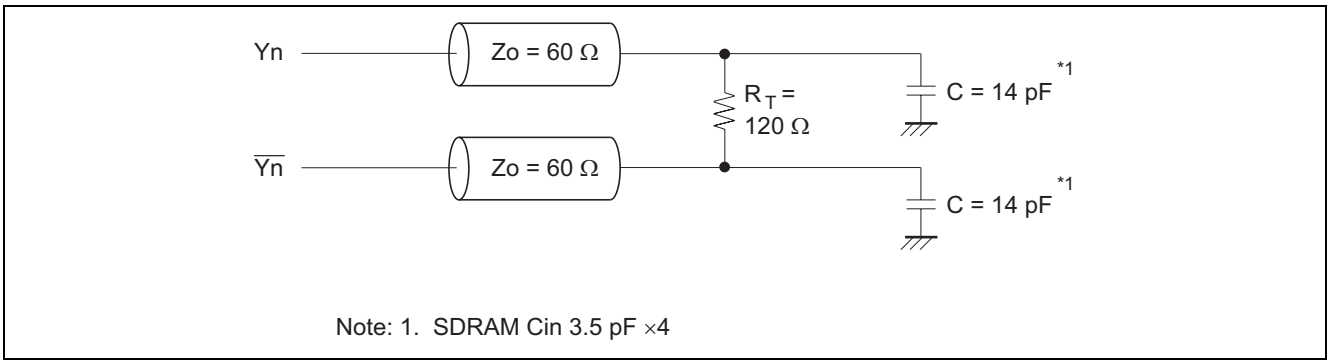


Figure 1 Clock outputs test circuit

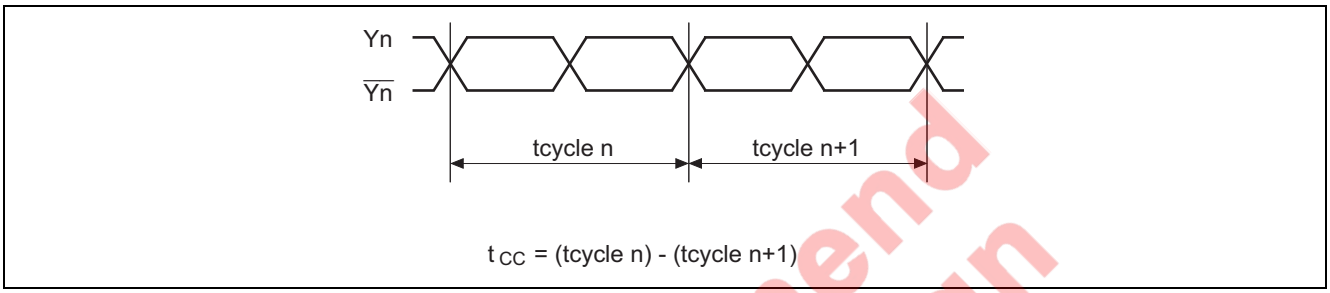


Figure 2 Cycle to cycle jitter

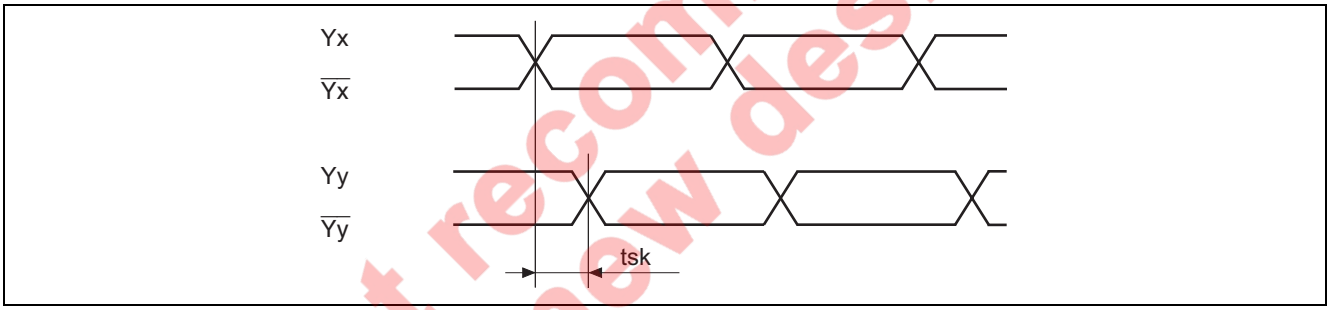
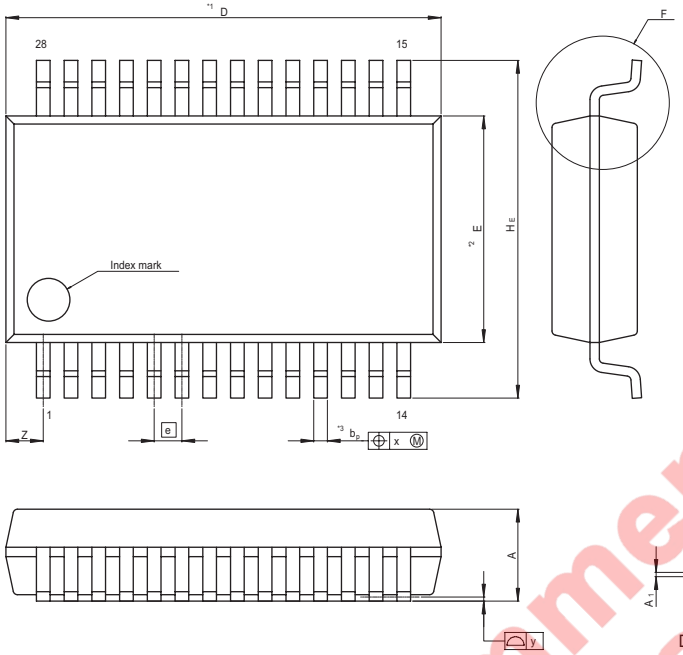


Figure 3 Output clock skew (Differential clock output)

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Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP28-5.3x10.2-0.65	PRSP0028JA-A	FP-28DSA/FP-28DSAV	0.255g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.20	10.50
E	—	5.30	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.10
b_p	0.24	0.32	0.40
b_1	—	0.30	—
c	0.17	0.22	0.27
c_1	—	0.20	—
θ	0°	—	8°
H_E	7.70	7.90	8.10
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	1.025
L	0.45	0.60	0.75
L_1	—	1.30	—

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