# EN71PL032A Base MCP
## Stacked Multi-Chip Product (MCP) Flash Memory and RAM
## 32 Megabit (2M x 16-bit) CMOS 3.0 Volt-only Simultaneous Operation Page Mode Flash Memory and
## 16 Megabit (1M x 16-bit) Pseudo Static RAM

# Distinctive Characteristics
## MCP Features

- **Power supply voltage of 2.7 V to 3.3V**
- **High performance**
  - 70 ns
- **Package**
  - 7 x 9 x 1.2mm 56 ball FBGA
- **Operating Temperature**
  - 25°C to +85°C

## General Description

The EN71PL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- EN29PL032A (Simultaneous Read/Write) Flash memory die.
- Pseudo SRAM.

For detailed specifications, please refer to the individual datasheets listed in the following table.

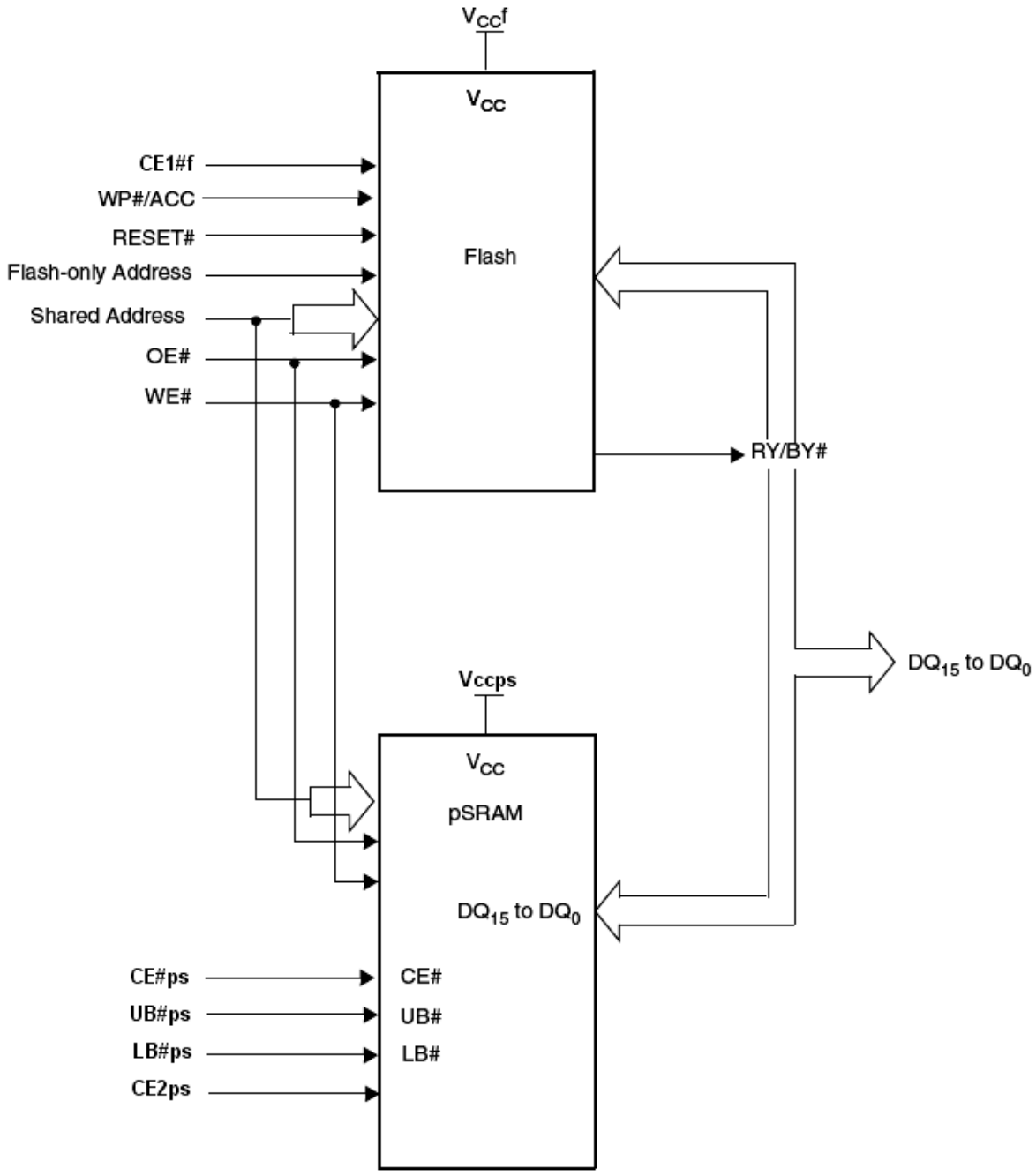
| Device | Document |
|---|---|
| NOR Flash | EN29PL032A |
| Pseudo SRAM | ENPSL16 |

## Product Selector Guide

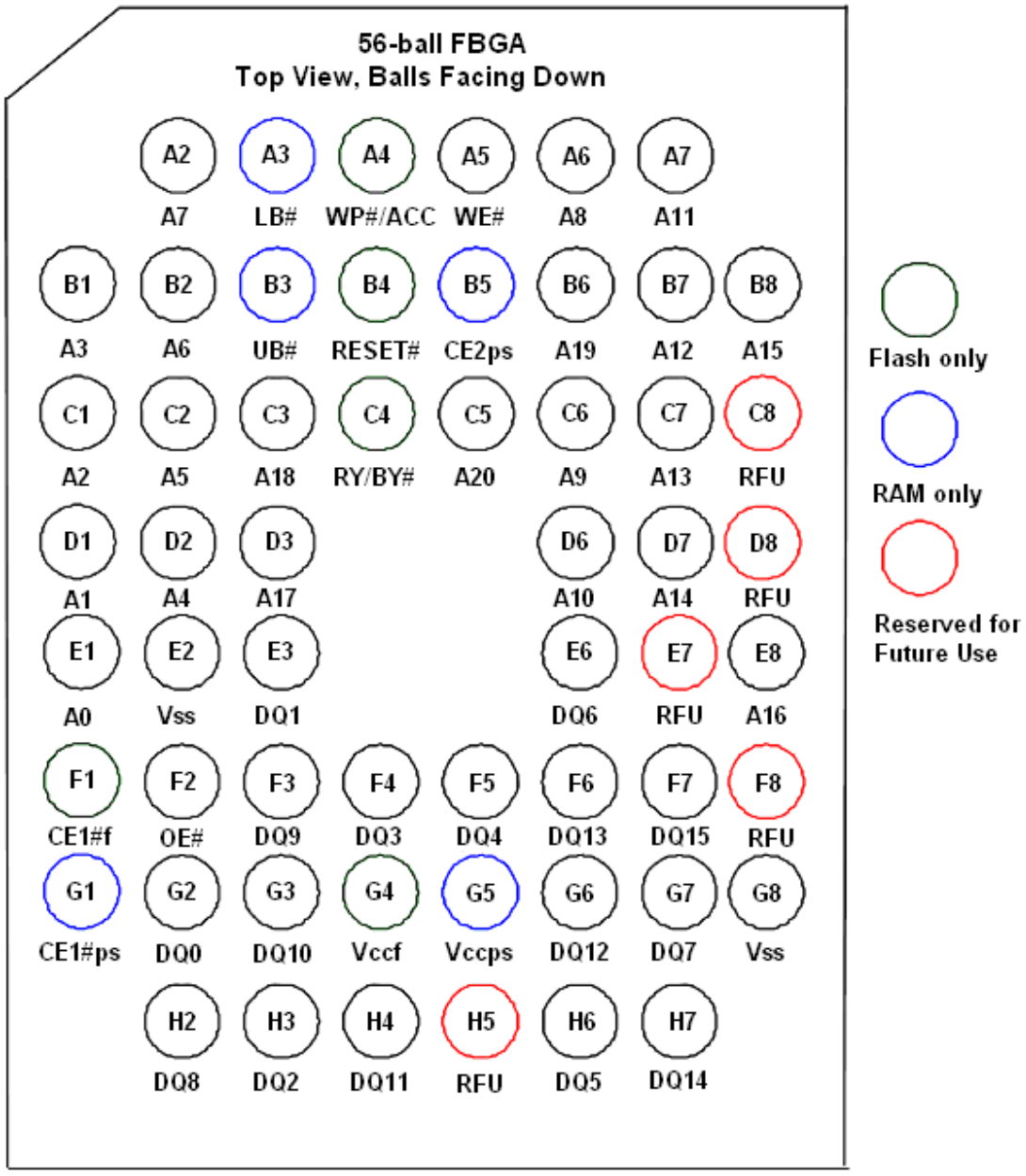
### 32Mb Flash Memory

| | | | |
|---|---|---|---|
| **Device-Model#** | EN71PL032A0A | **pSRAM density** | 16M pSRAM |
| **Flash Access time** | 70ns | **pSRAM Access time** | 70ns |
| **Page read Access time** | 25ns | **pSRAM Page read Access time** | 25ns |
| **Package** | 56 FBGA | | |

## MCP Block Diagram



## Connection Diagram




| MCP | Flash-only Addresses | Shared Addresses |
|---|---|---|
| EN71PL032A0A | A20 | A19 – A0 |

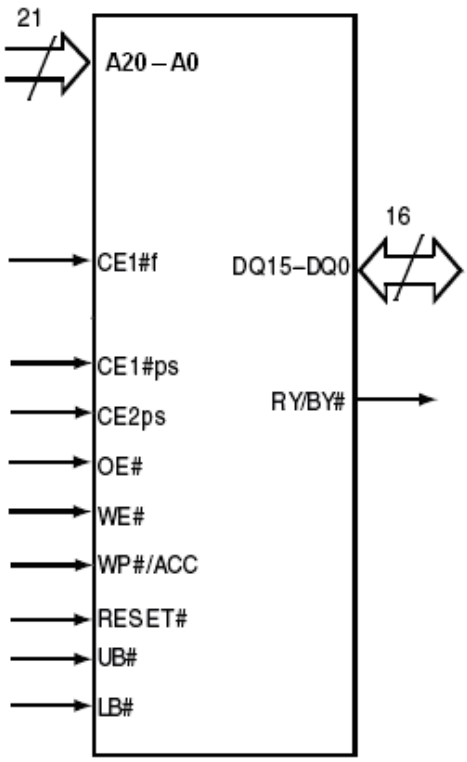
**Note:** A9 = VID for HV Autoselect mode is not available for MCP product.

## Pin Description

| Signal | Description |
|---|---|
| A20–A0 | 21 Address Inputs (Common) |
| DQ15–DQ0 | 16 Data Inputs/Outputs (Common) |
| CE1#f | Chip Enable 1 (Flash) |
| CE1#ps | Chip Enable 1 (pSRAM) |
| CE2ps | Chip Enable 2 (pSRAM) |
| OE# | Output Enable (Common) |
| WE# | Write Enable (Common) |
| RY/BY# | Ready/Busy Output (Flash) |
| UB# | Upper Byte Control (pSRAM) |
| LB# | Lower Byte Control (pSRAM) |
| RESET# | Hardware Reset Pin, Active Low (Flash) |
| WP#/ACC | Hardware Write Protect/Acceleration Pin (Flash) |
| $V_{CC}$f | Flash 3.0 volt-only single power supply |
| $V_{CC}$ps | pSRAM Power Supply |
| $V_{SS}$ | Device Ground (Common) |
| NC | Pin Not Connected Internally |

**Note:** A9 = VID for HV Autoselect mode is not available for MCP product.

## Logic Symbol



## Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

## Eon products’ Top Marking

cFeon

**cFeon Top Marking Example:**

**cFeon**

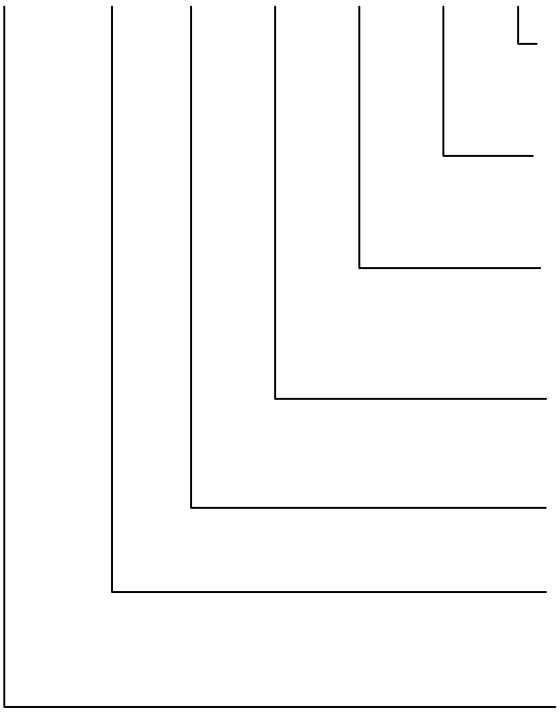
**Part Number: XXXX-XXX**
**Lot Number: XXXXX**
**Date Code: XXXXX**

## For More Information

Please contact your local sales office for additional information about Eon memory solutions.

## ORDERING INFORMATION

EN71PL032 A0 A — 70 C W P



**PACKAGING CONTENT**
P = RoHS compliant

**TEMPERATURE RANGE**
W = Wireless (-25°C to +85°C)

**PACKAGE**
C =56-Ball Fine Pitch Ball Grid Array (FBGA)
0.80mm pitch, 7mm x 9mm package

**SPEED**
70 = 70ns

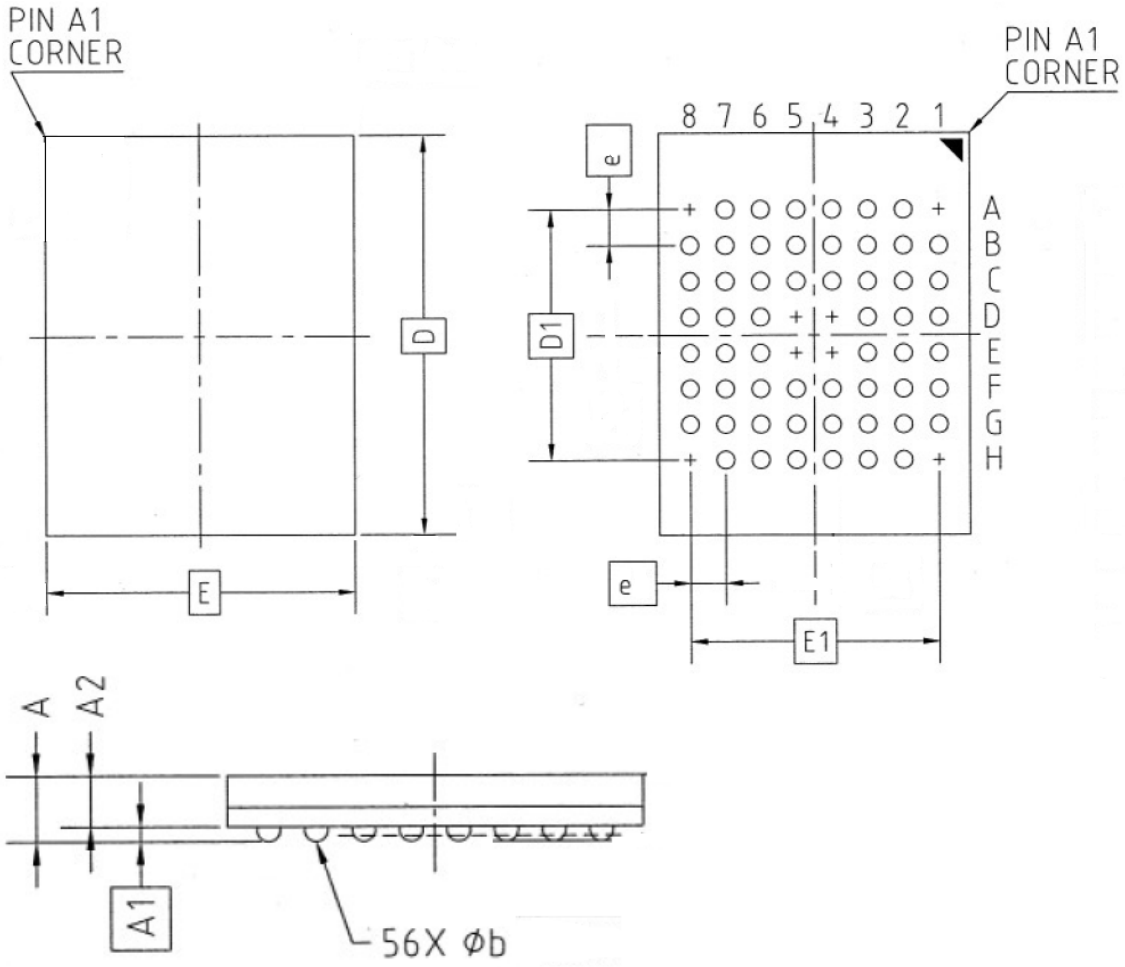
**A** = version identifier

**pSRAM density**
A0 = 16M pSRAM

**BASE PART NUMBER**
EN = Eon Silicon Solution Inc.
71PL = Multi-chip Product (MCP)
3.0V Simultaneous Read/Write,
Page Mode Flash Memory and RAM
032 = 32 Megabit (2M x 16)

## PACKAGE MECHANICAL

**56-ball Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package,
pitch: 0.8mm, ball: 0.4mm**




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOR | MAX |
| A | - - - | - - - | 1.20 |
| A1 | 0.25 | 0.30 | 0.35 |
| A2 | 0.80 | - - - | 0.95 |
| D | 8.95 | 9.00 | 9.05 |
| E | 6.95 | 7.00 | 7.05 |
| D1 | - - - | 5.60 | - - - |
| E1 | - - - | 5.60 | - - - |
| e | - - - | 0.80 | - - - |
| b | 0.35 | 0.40 | 0.45 |

**Note : Controlling dimensions are in millimeters (mm).**

## Revisions List

| Revision No | Description | Date |
|---|---|---|
| A | Initial Release | 2010/11/15 |