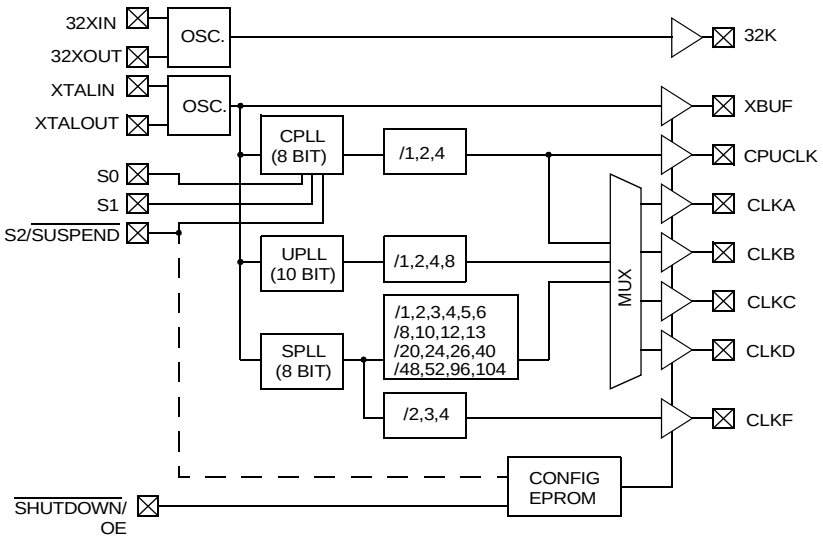
Three-PLL General Purpose EPROM Programmable Clock Generator

Features	Benefits
Three integrated phase-locked loops	Generates up to 3 custom frequencies from external sources
EPROM programmability	Easy customization and fast turnaround
Factory-programmable (CY2291) or field-programmable (CY2291F) device options	Programming support available for all opportunities
Low-skew, low-jitter, high-accuracy outputs	Meets critical industry standard timing requirements
Power-management options (Shutdown, OE, Suspend)	Supports low-power applications
Frequency select option	8 user-selectable frequencies on CPU PLL
Smooth slewing on CPUCLK	Allows downstream PLLs to stay locked on CPUCLK output
Configurable 3.3V or 5V operation	Enables application compatibility
20-pin SOIC Package	Industry-standard packaging saves on board space

Selector Guide

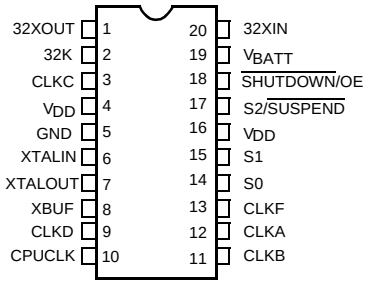
Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2291	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–100 MHz (5V) 76.923 kHz–80 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2291I	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2291F	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–90 MHz (5V) 76.923 kHz–66.6 MHz (3.3V)	***Field Programmable*** Commercial Temperature
CY2291FI	8	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	76.923 kHz–80 MHz (5V) 76.923 kHz–60.0 MHz (3.3V)	***Field Programmable*** Industrial Temperature

Logic Block Diagram



Pin Configurations

CY2291
20-pin SOIC



Pin Summary

Name	Pin Number	Description
32XOUT	1	32.768 kHz crystal feedback.
32K	2	32.768 kHz output (always active if V_{BATT} is present).
CLKC	3	Configurable clock output C.
V_{DD}	4, 16	Voltage supply.
GND	5	Ground.
XTALIN[1]	6	Reference crystal input or external reference clock input.
XTALOUT[1, 2]	7	Reference crystal feedback.
XBUF	8	Buffered reference clock output.
CLKD	9	Configurable clock output D.
CPUCLK	10	CPU frequency clock output.
CLKB	11	Configurable clock output B.
CLKA	12	Configurable clock output A.
CLKF	13	Configurable clock output F.
S0	14	CPU clock select input, bit 0.
S1	15	CPU clock select input, bit 1.
S2/$\overline{\text{SUSPEND}}$	17	CPU clock select input, bit 2. Optionally enables suspend feature when LOW.[3]
$\overline{\text{SHUTDOWN}}$/OE	18	Places outputs in three-state[4] condition and shuts down chip when LOW. Optionally, only places outputs in three-state[4] condition and does not shut down chip when LOW.
V_{BATT}	19	Battery supply for 32.768-kHz circuit.
32XIN	20	32.768-kHz crystal input.

Notes:
1. For best accuracy, use a parallel-resonant crystal, $C_{LOAD} \approx 17$ pF or 18 pF.
2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).
3. Please refer to application note “Understanding the CY2291, CY2292 and CY2295” for more information.
4. The CY2291 has weak pull-downs on all outputs (except 32K). Hence, when a three-state condition is forced on the outputs, the output pins are pulled LOW.

Operation

The CY2291 is a third-generation family of clock generators. The CY2291 is upwardly compatible with the industry standard ICD2023 and ICD2028 and continues their tradition by providing a high level of customizable features to meet the diverse clock generation needs of modern motherboards and other synchronous systems.

All parts provide a highly configurable set of clocks for PC motherboard applications. Each of the four configurable clock outputs (CLKA–CLKD) can be assigned 1 of 30 frequencies in any combination. Multiple outputs configured for the same or related[3] frequencies will have low (≤500 ps) skew, in effect providing on-chip buffering for heavily loaded signals.

The CY2291 can be configured for either 5V or 3.3V operation. The internal ROM tables use EPROM technology, allowing full customization of output frequencies. The reference oscillator has been designed for 10-MHz to 25-MHz crystals, providing additional flexibility. No external components are required with this crystal. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used. Customers using the 32-kHz oscillator should connect a 10-MΩ resistor in parallel with the 32-kHz crystal.

Output Configuration

The CY2291 has five independent frequency sources on-chip. These are the 32-kHz oscillator, the reference oscillator, and three Phase-Locked Loops (PLLs). Each PLL has a specific function. The System PLL (SPLL) drives the CLKF output and provides fixed output frequencies on the configurable outputs. The SPLL offers the most output frequency divider options. The CPU PLL (CPLL) is controlled by the select inputs (S0–S2) to provide eight user-selectable frequencies with smooth slewing between frequencies. The Utility PLL (UPLL) provides the most accurate clock. It is often used for miscellaneous frequencies not provided by the other frequency sources.

All configurations are EPROM programmable, providing short sample and production lead times. Please refer to the application note “Understanding the CY2291, CY2292, and CY2295” for information on configuring the part.

Power Saving Features

The $\overline{\text{SHUTDOWN}}$/OE input three-states the outputs when pulled LOW (the 32-kHz clock output is not affected). If system shutdown is enabled, a LOW on this pin also shuts off the PLLs, counters, the reference oscillator, and all other active components. The resulting current on the V_{DD} pins will be less than 50 μA (for Commercial Temp. or 100 μA for Industrial Temp.) plus 15 μA max. for the 32-kHz subsystem and is typically 10 μA. After leaving shutdown mode, the PLLs will have to re-lock. All outputs except 32K have a weak pull-down so that the outputs do not float when three-stated.[4]

The S2/$\overline{\text{SUSPEND}}$ input can be configured to shut down a customizable set of outputs and/or PLLs, when LOW. All PLLs and any of the outputs except 32K can be shut off in nearly any combination. The only limitation is that if a PLL is shut off, all outputs derived from it must also be shut off. Suspending a PLL shuts off all associated logic, while suspending an output simply forces a three-state condition.[3]

The CPUCLK can slew (transition) smoothly between 8 MHz and the maximum output frequency (100 MHz at 5V/80 MHz at 3.3V for Commercial Temp. parts or 90 MHz at 5V/66.6 MHz at 3.3V for Industrial Temp. and for field-programmed parts). This feature is extremely useful in “Green” PC and laptop applications, where reducing the frequency of operation can result in considerable power savings. This feature meets all 486 and Pentium® processor slewing requirements.

CyClocks™ Software

CyClocks is an easy-to-use application that allows you to configure any one of the EPROM programmable clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. CyClocks also has a power calculation feature that allows you to see the power consumption of your specific configuration. You can download a copy of CyClocks for free on Cypress’s website at www.cypress.com.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmers is a portable programmer designed to custom program our family of EPROM Field Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Storage Temperature ..... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... 260°C

Junction Temperature ..... 150°C

Package Power Dissipation ..... 750 mW

Static Discharge Voltage ..... ≥2000V (per MIL-STD-883, Method 3015)

Operating Conditions[5]

Parameter	Description	Part Numbers	Min.	Max.	Unit
V_{DD}	Supply Voltage, 5.0V operation	All	4.5	5.5	V
V_{DD}	Supply Voltage, 3.3V operation	All	3.0	3.6	V
V_{BATT}	Battery Backup Voltage	All	2.0	5.5	V
T_A	Commercial Operating Temperature, Ambient	CY2291/CY2291F	0	+70	°C
	Industrial Operating Temperature, Ambient	CY2291I/CY2291FI	–40	+85	°C
C_{LOAD}	Max. Load Capacitance 5.0V Operation	All		25	pF
C_{LOAD}	Max. Load Capacitance 3.3V Operation	All		15	pF
f_{REF}	External Reference Crystal	All	10.0	25.0	MHz
	External Reference Clock[6, 7, 8]	All	1	30	MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)		0.05	50	ms

Electrical Characteristics, Commercial 5.0V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
$V_{OH–32}$	32.768-kHz HIGH-Level Output Voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5			V
$V_{OL–32}$	32.768-kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}–0.5V			<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Commercial	V_{DD} = V_{DD} Max., 5V operation			75	100	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active, excluding V_{BATT}	CY2291/CY2291F		10	50	µA
I_{BATT}	V_{BATT} Power Supply Current	V_{BATT} = 3.0V			5	15	µA

Notes:

5. Electrical parameters are guaranteed by design with these operating conditions, unless otherwise noted.
6. External input reference clock must have a duty cycle between 40% and 60%, measured at $V_{DD}/2$.
7. Please refer to application note “Crystal Oscillator Topics” for information on AC-coupling the external input reference clock.
8. The oscillator circuit is optimized for a crystal reference and for external reference clocks up to 20 MHz. For external reference clocks above 20 MHz, it is recommended that a 150Ω pull-up resistor to V_{DD} be connected to the Xout pin.
9. Xtal inputs have CMOS thresholds.
10. Load = Max., V_{IN} = 0V or V_{DD}, Typical (–104) configuration, CPUCLK = 66 MHz. Other configurations will vary. Power can be approximated by the following formula (multiply by 0.65 for 3V operation): $I_{DD}=10+0.06•(F_{CPLL}+F_{UPLL}+2•F_{SPLL})+0.27•(F_{CLKA}+F_{CLKB}+F_{CLKC}+F_{CLKD}+F_{CPUCLK}+F_{CLKF}+F_{XBUF})$.

Electrical Characteristics, Commercial 3.3V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
$V_{OH–32}$	32.768-kHz HIGH-Level Output Voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5			V
$V_{OL–32}$	32.768-kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}–0.5V			<1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			<1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Commercial	V_{DD} = V_{DD} Max., 3.3V operation			50	65	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active, excluding V_{BATT}	CY2291/CY2291F		10	50	µA
I_{BATT}	V_{BATT} Power Supply Current	V_{BATT} = 3.0V			5	15	µA

Electrical Characteristics, Industrial 5.0V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
$V_{OH–32}$	32.768-kHz HIGH-Level Output Voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5			V
$V_{OL–32}$	32.768-kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}–0.5V			< 1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Industrial	V_{DD} = V_{DD} Max., 5V operation			75	110	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active, excluding V_{BATT}	CY2291I/CY2291FI		10	100	µA
I_{BATT}	V_{BATT} Power Supply Current	V_{BATT} = 3.0V			5	15	µA

Electrical Characteristics, Industrial 3.3V

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	I_{OH} = 4.0 mA		2.4			V
V_{OL}	LOW-Level Output Voltage	I_{OL} = 4.0 mA				0.4	V
$V_{OH–32}$	32.768-kHz HIGH-Level Output Voltage	I_{OH} = 0.5 mA		V_{BATT} 0.5			V
$V_{OL–32}$	32.768-kHz LOW-Level Output Voltage	I_{OL} = 0.5 mA				0.4	V
V_{IH}	HIGH-Level Input Voltage[9]	Except crystal pins		2.0			V
V_{IL}	LOW-Level Input Voltage[9]	Except crystal pins				0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}–0.5V			< 1	10	µA
I_{IL}	Input LOW Current	V_{IN} = +0.5V			< 1	10	µA
I_{OZ}	Output Leakage Current	Three-state outputs				250	µA
I_{DD}	V_{DD} Supply Current[10] Industrial	V_{DD} = V_{DD} max., 3.3V operation			50	70	mA
I_{DDS}	V_{DD} Power Supply Current in Shutdown Mode[10]	Shutdown active, excluding V_{BATT}	CY2291I/CY2291FI		10	100	µA
I_{BATT}	V_{BATT} Power Supply Current	V_{BATT} = 3.0V			5	15	µA

Switching Characteristics, Commercial 5.0V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	CY2291	10 (100 MHz)		13000 (76.923 kHz)	ns
			CY2291F	11.1 (90 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHZ		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 15]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter ($f_{OUT} > 50$ MHz)			<250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-Up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-Up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2291	8		100	MHz
			CY2291F	8		90	MHz

Notes:
11. XBUF duty cycle depends on XTALIN duty cycle.
12. Measured at 1.4V.
13. Measured between 0.4V and 2.4V.
14. Jitter varies with configuration. All standard configurations sample tested at the factory conform to this limit. For more information on jitter, please refer to the application note: “Jitter in PLL-Based Systems.”
15. CLKF is not guaranteed to be in phase with CLKA-D, even if it is referenced off the same PLL.

Switching Characteristics, Commercial 3.3V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 3.3V operation	CY2291	12.5 (80 MHz)		13000 (76.923 kHz)	ns
			CY2291F	15 (66.6 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHZ		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 15]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)			<250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-Up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-Up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2291	8		80	MHz
			CY2291F	8		66.6	MHz

Switching Characteristics, Industrial 5.0V

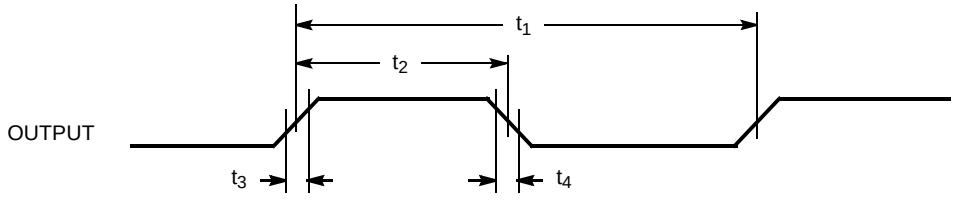
Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 5V operation	CY2291I	11.1 (90 MHz)		13000 (76.923 kHz)	ns
			CY2291FI	12.5 (80 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHZ		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 15]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter (f_{OUT} > 50 MHz)			<250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-Up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-Up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2291I	8		90	MHz
			CY2291FI	8		80	MHz

Switching Characteristics, Industrial 3.3V

Parameter	Name	Description		Min.	Typ.	Max.	Unit
t_1	Output Period	Clock output range, 3.3V operation	CY2291I	15 (66.6 MHz)		13000 (76.923 kHz)	ns
			CY2291FI	16.66 (60 MHz)		13000 (76.923 kHz)	ns
	Output Duty Cycle[11]	Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} \geq 66$ MHZ		40%	50%	60%	
		Duty cycle for outputs, defined as $t_2 \div t_1$[12] $f_{OUT} < 66$ MHZ		45%	50%	55%	
t_3	Rise Time	Output clock rise time[13]			3	5	ns
t_4	Fall Time	Output clock fall time[13]			2.5	4	ns
t_5	Output Disable Time	Time for output to enter three-state mode after SHUTDOWN/OE goes LOW			10	15	ns
t_6	Output Enable Time	Time for output to leave three-state mode after SHUTDOWN/OE goes HIGH			10	15	ns
t_7	Skew	Skew delay between any identical or related outputs[3, 12, 15]			< 0.25	0.5	ns
t_8	CPUCLK Slew	Frequency transition rate		1.0		20.0	MHz/ ms
t_{9A}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9A} Max. – t_{9A} min.),% of clock period ($f_{OUT} \leq 4$ MHz)			<0.5	1	%
t_{9B}	Clock Jitter[14]	Peak-to-peak period jitter (t_{9B} Max. – t_{9B} min.) (4 MHz $\leq f_{OUT} \leq$ 16 MHz)			<0.7	1	ns
t_{9C}	Clock Jitter[14]	Peak-to-peak period jitter (16 MHz < $f_{OUT} \leq$ 50 MHz)			<400	500	ps
t_{9D}	Clock Jitter[14]	Peak-to-peak period jitter ($f_{OUT} > 50$ MHz)			<250	350	ps
t_{10A}	Lock Time for CPLL	Lock Time from Power-Up			<25	50	ms
t_{10B}	Lock Time for UPLL and SPLL	Lock Time from Power-Up			<0.25	1	ms
	Slew Limits	CPU PLL Slew Limits	CY2291I	8		66.6	MHz
			CY2291FI	8		60	MHz

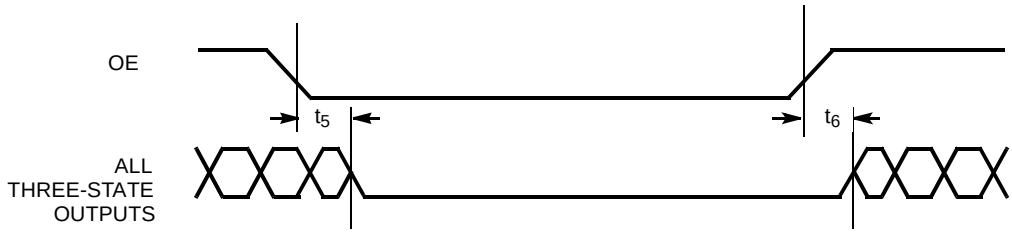
Switching Waveforms

All Outputs, Duty Cycle and Rise/Fall Time

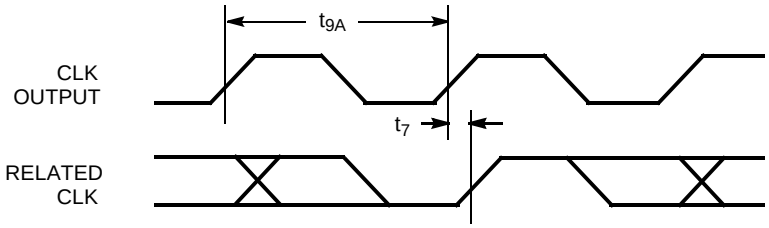


Switching Waveforms (continued)

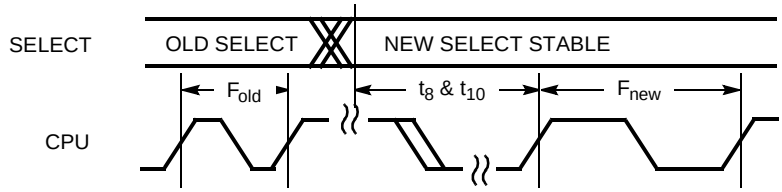
Output Three-State Timing[4]



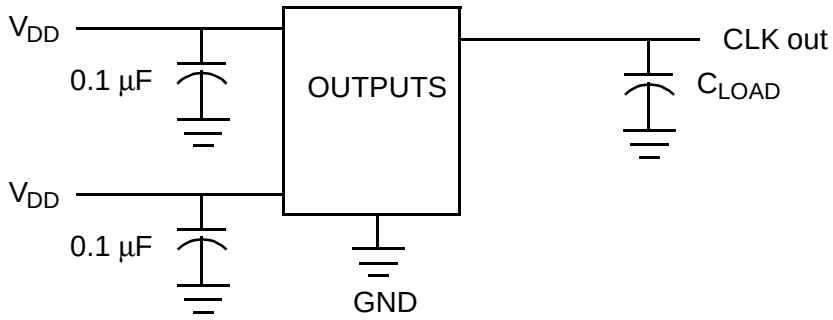
CLK Outputs Jitter and Skew



CPU Frequency Change



Test Circuit



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2291SC–XXX	S5	20-Pin SOIC	Commercial	5.0V
CY2291SL–XXX	S5	20-Pin SOIC	Commercial	3.3V
CY2291F	S5	20-Pin SOIC	Commercial	3.3V or 5.0V
CY2291SI–XXX	S5	20-Pin SOIC	Industrial	3.3V or 5.0V
CY2291FI	S5	20-Pin SOIC	Industrial	3.3V or 5.0V

CyClocks is a trademark of Cypress Semiconductor Corporation.
Pentium is a registered trademark of Intel Corporation.

Custom Configuration Request Procedure

The CY229x are EPROM-programmable devices that may be configured in the factory or in the field by a Cypress Field Application Engineer (FAE). The output frequencies requested will be matched as closely as the internal PLL divider and multiplier options allow. All custom requests must be submitted to your local Cypress FAE or sales representative. The method to use to request custom configurations is:

Use CyClocks™ software. This software automatically calculates the output frequencies that can be generated by the CY229x devices and provides a print-out of final pinout which can be submitted (in electronic or print format) to your local FAE or sales representative. The CyClocks software is available free of charge from the Cypress website (http://www.cypress.com) or from your local sales representative.

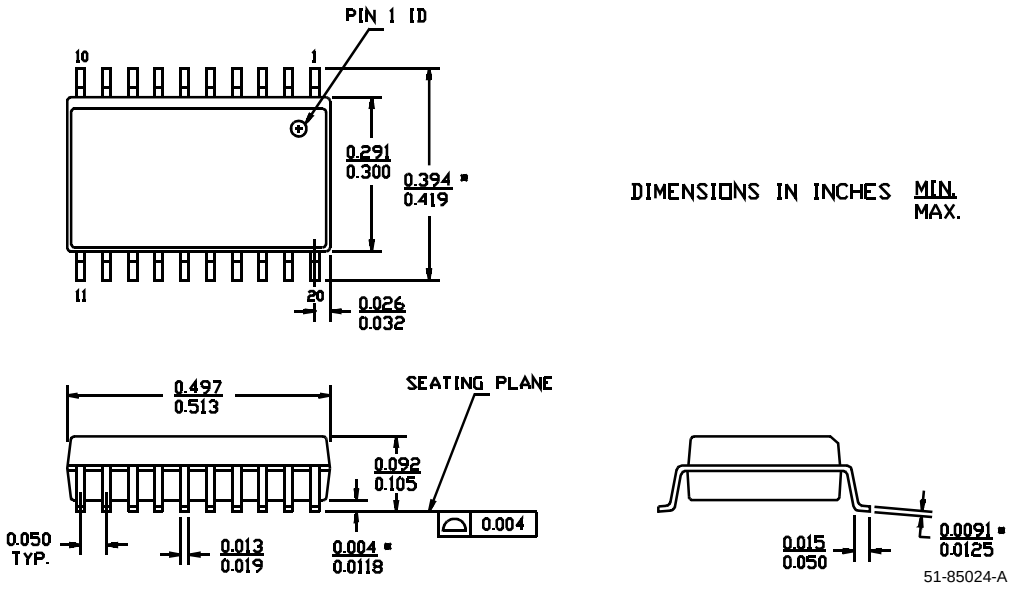
Once the custom request has been processed you will receive a part number with a 3-digit extension (e.g., CY2292SC-128) specific to the frequencies and pinout of your device. This will be the part number used for samples requests and production orders.

Package Characteristics

Package	θ_{JA} (C/W)	θ_{JC} (C/W)	Transistor Count
20-pin SOIC	125	25	9271

Package Diagram

20-Lead (300-Mil) Molded SOIC S5



© Cypress Semiconductor Corporation, 2001. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress Semiconductor product. Nor does it convey or imply any license under patent or other rights. Cypress Semiconductor does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress Semiconductor products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress Semiconductor against all charges.

Document Title: CY2291 Three-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07189				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110321	10/28/01	SZV	Change from Spec number: 38-00410 to 38-07189
*A	121836	12/14/02	RBI	Power up requirements added to Operating Conditions Information