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## 4 Revision History

### Changes from Revision B (May 2016) to Revision C

Page

• Added bq2962 REG options .....	<b>1</b>
• Changed Part number to bq2960, bq2961, bq2962 to identify each spin family throughout the datasheet .....	<b>1</b>
• Added bq2962 device to Recommended Operating Conditions .....	<b>2</b>
• Added bq296202, bq296203, bq296212, bq296213 .....	<b>3</b>
• Added bq2962 pinout .....	<b>4</b>
• Added bq2962 device to Recommended Operating Conditions .....	<b>5</b>
• Added bq2962 VREG specification .....	<b>7</b>
• Added bq2962 regulator programmable option .....	<b>10</b>
• Changed figure title to apply to bq2962 family .....	<b>17</b>
• Changed figure title to apply to bq2962 .....	<b>20</b>

### Changes from Revision A (January 2016) to Revision B

Page

• Added bq296114 to <a href="#">Device Comparison Table</a> .....	<b>3</b>
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### Changes from Original (November 2013) to Revision A

Page

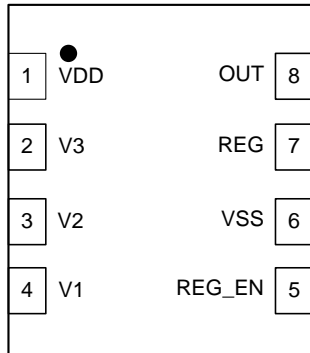
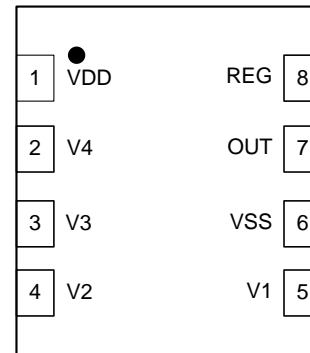
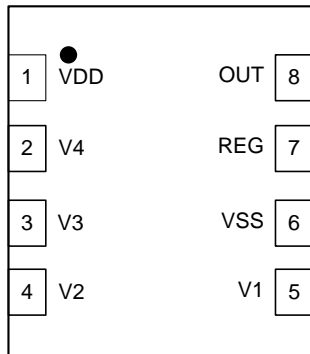
• Changed the device listing in the data sheet header information to: bq2961 .....	<b>1</b>
• Changed bq296106, '107, '111 From: Preview To: Released status .....	<b>3</b>
• Added bq296112 to <a href="#">Device Comparison Table</a> .....	<b>3</b>
• Added bq296113 to <a href="#">Device Comparison Table</a> .....	<b>3</b>
• Added Available the bq2961xy configuration range to <a href="#">Device Comparison Table</a> .....	<b>3</b>

## 5 Device Comparison Table

bq2961 Family	bq2962 Family	OVP (V)	OVP DELAY (s)	UV (V)	LDO (V)
bq296100 <sup>(1)</sup>	—	4.35	6.5	2.5	3.3
bq296101 <sup>(1)</sup>	—	4.40	6.5	2.5	3.3
bq296102 <sup>(1)</sup>	bq296202 <sup>(1)</sup>	4.45	6.5	2.5	3.3
bq296103	bq296203 <sup>(1)</sup>	4.50	6.5	2.5	3.3
bq296104 <sup>(1)</sup>	—	4.35	6.5	2.8	3.3
bq296105 <sup>(1)</sup>	—	4.40	6.5	2.8	3.3
bq296106	—	4.45	6.5	2.8	3.3
bq296107	—	4.50	6.5	2.8	3.3
bq296108 <sup>(1)</sup>	—	4.50	6.5	2.4	3.3
bq296109 <sup>(1)</sup>	—	4.325	3.0	2.5	3.3
bq296110 <sup>(1)</sup>	—	4.45	3.0	2.5	3.3
bq296111	—	4.45	4.0	2.5	3.3
bq296112	bq296212 <sup>(1)</sup>	4.50	3.0	2.5	3.3
bq296113	bq296213 <sup>(1)</sup>	4.35	3.0	2.5	3.3
bq296114	—	4.50	4.0	2.5	3.3
bq2961xy	bq2962xy	3.85V - 4.60V in 50mV step	3.0, 4.0, 5.5, 6.5	2.0V - 2.8V in 50mV step	1.8, 2.5, 3.3 (bq2961) 3, 3.15, 3.3 (bq2962)

(1) Product Preview only

## 6 Pin Configuration and Functions

**2s-to-3s bq2960xy  
(Top View)**

**2s-to-4s bq2962xy  
(Top View)**

**2s-to-4s bq2961xy  
(Top View)**


### Pin Functions

NAME	PIN			TYPE <sup>(1)</sup>	DESCRIPTION
	BQ2960	BQ2961	BQ2962		
OUT	8	8	7	OA	Analog Output drive for overvoltage fault signal, CMOS Output High or Open Drain Active Low.
PWPD	9	9	9	P	TI recommends connecting the exposed pad to VSS on PCB.
REG	7	7	8	OA	Regulated Supply Output. Requires an external ceramic capacitor for stability.
REG_EN	5	—	—	IA	Regulated Supply Output Enable. A "high" to enable REG output and "low" to disable REG output.
V1	4	5	5	IA	Sense input for positive voltage of the lowest cell from the bottom of the stack.
V2	3	4	4	IA	Sense input for positive voltage of the second cell from the bottom of the stack.
V3	2	3	3	IA	Sense input for positive voltage of the third cell from the bottom of the stack.
V4	—	2	2	IA	Sense input for positive voltage of the fourth cell from the bottom of the stack.
VDD	1	1	1	P	Power supply input
VSS	6	6	6	P	Electrically connected to integrated circuit ground and negative terminal of the lowest cell in the stack.

(1) IA = Analog input, OA = Analog Output, P = Power connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VDD – VSS	–0.3	30	V
Input voltage range	V4 – V3, V3 – V2, V2 – V1, V1 – VSS	–0.3	30	
	REG – VSS	–0.3	3.6	
	REG_EN – VSS	–0.3	28	
Output voltage range	OUT – VSS	–0.3	30	
Continuous total power dissipation, P <sub>TOT</sub>		See <a href="#">Thermal Information</a> .		
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>		300	300	°C
Storage temperature, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub> <sup>(1)</sup>	Supply voltage, V <sub>DD</sub> <sup>(1)</sup> , bq2960xy	3		15	V
	Supply voltage, V <sub>DD</sub> <sup>(1)</sup> , bq2961xy, bq2962xy	3		20	
	Supply voltage, V <sub>DD</sub> with REG output on	4			
Input voltage range	V <sub>n</sub> – V <sub>n-1</sub> , V1 – VSS	0		5	V
	REG_EN	0		15	V
Operating ambient temperature range, T <sub>A</sub>		–40		110	°C

- (1) See [Typical Application](#).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq2960xy	UNIT
		DSG (WSON)	
		8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	62	°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	72	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	32.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.6	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	33	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case(bottom) thermal resistance	10	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 7.5 Electrical Characteristics

Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 14.4\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$ , and  $V_{DD} = 3\text{ V}$  to  $15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Voltage Protection Thresholds</b>						
$V_{OV}$	$V_{(PROTECT)}$ Overvoltage Detection	$R_{IN} = 1\text{ k}\Omega$	Applicable Voltage: 3.85 V to 4.6 V in 50 mV steps			V
$V_{HYS}$	OV Detection Hysteresis		250	300	400	mV
$V_{OA}$	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	$T_A = -40^\circ\text{C}$	-40		40	mV
		$T_A = 0^\circ\text{C}$	-20		20	mV
		$T_A = 60^\circ\text{C}$	-24		24	mV
		$T_A = 110^\circ\text{C}$	-54		54	mV
		$T_A = 110^\circ\text{C}$	-54		54	mV
<b>Supply and Leakage Current</b>						
$I_{DD}$	Supply Current	$(V_n - V_{n-1}) = 3.8\text{ V}$ and $(V1 - V_{SS}) > V_{UVREG}$ , $V_{DD} = \text{top } V_n$ voltage, $I_{REG} = 0\text{ mA}$ , $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$		4	6	$\mu\text{A}$
		$(V_n - V_{n-1}) = 3.8\text{ V}$ and $(V1 - V_{SS}) > V_{UVREG}$ , $V_{DD} = \text{top } V_n$ voltage, $I_{REG} = 0\text{ mA}$ , $T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$			8	$\mu\text{A}$
		$(V_n - V_{n-1}) = 3.8\text{ V}$ and $(V1 - V_{SS}) < V_{UVREG}$ , $V_{DD} = \text{top } V_n$ voltage, $T_A = 0^\circ\text{C}$ to $60^\circ\text{C}$		1	2	$\mu\text{A}$
		$(V_n - V_{n-1}) = 3.8\text{ V}$ and $(V1 - V_{SS}) < V_{UVREG}$ , $V_{DD} = \text{top } V_n$ voltage, $T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$			4	$\mu\text{A}$
$I_{IN}$	Input Current at $V_x$ Pins	$(V_n - V_{n-1}) = (V1 - V_{SS}) = 3.8\text{ V}$ , $V_{DD} = \text{top } V_n$ voltage, $T_A = 25^\circ\text{C}$	-0.1		0.1	$\mu\text{A}$
<b>Output Drive OUT, CMOS Active High</b>						
$V_{OUT}$	Output Drive Voltage, Active High	$(V_n - V_{n-1})$ or $(V1 - V_{SS}) > V_{OV}$ , $I_{OH} = 100\text{ }\mu\text{A}$ , $V_{DD} = \text{top } V_n$ voltage	6			V
		If three of four cells are short circuited, only one cell remains powered and $> V_{OV}$ , $V_{DD} = V_n$ (the remaining cell voltage), $I_{OH}$ $= 100\text{ }\mu\text{A}$		$V_{DD} - 0.3$		V
		$(V_n - V_{n-1})$ and $(V1 - V_{SS}) < V_{OV}$ , $V_{DD} = \text{sum of the cell stack}$ voltage, $I_{OL} = 100\text{ }\mu\text{A}$ measured into OUT pin		250	400	mV
$I_{OUTH}$	OUT Source Current (during OV)	$(V_n - V_{n-1})$ , $(V3 - V2)$ , or $(V1 - V_{SS}) > V_{OV}$ , $V_{DD} = \text{top } V_n$ voltage, forced OUT = 0 V, measured out of OUT pin			4.5	mA
$I_{OUTL}$	OUT Sink Current (no OV)	$(V_n - V_{n-1})$ and $(V1 - V_{SS}) < V_{OV}$ , $V_{DD} = \text{top } V_n$ voltage, forced OUT = VDD, measured into OUT pin. Pull-up resistor $R_{PU} = 5\text{ k}\Omega$ to VDD	0.5		14	mA
<b>Internal Fixed Delay Timer</b>						
$t_{DELAY}$	OV Delay Time <sup>(1)</sup>	Internal Fixed Delay, 3 second delay option	2.4	3	3.6	s
		Internal Fixed Delay, 4 second delay option	3.2	4	4.8	s
		Internal Fixed Delay, 5.5 second delay option	4.4	5.5	6.6	s
		Internal Fixed Delay, 6.5 second delay option	5.2	6.5	7.8	s
$t_{DELAY\_CTM}$	Fault Detection Delay Time in Test Mode OV Delay Time	Internal Fixed delay		15		ms

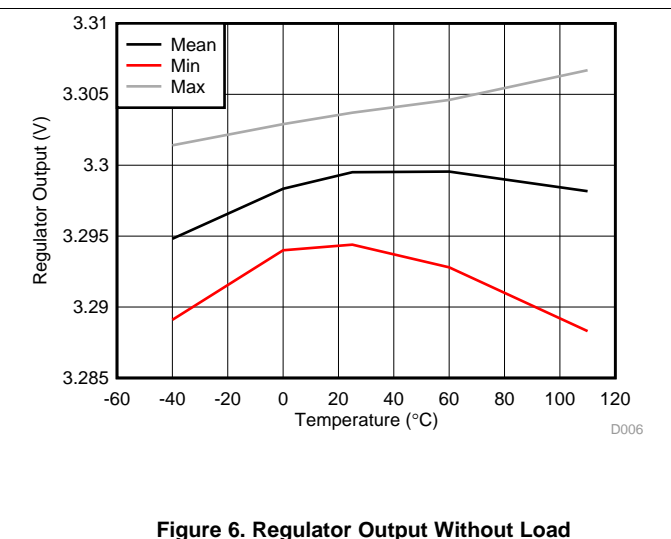
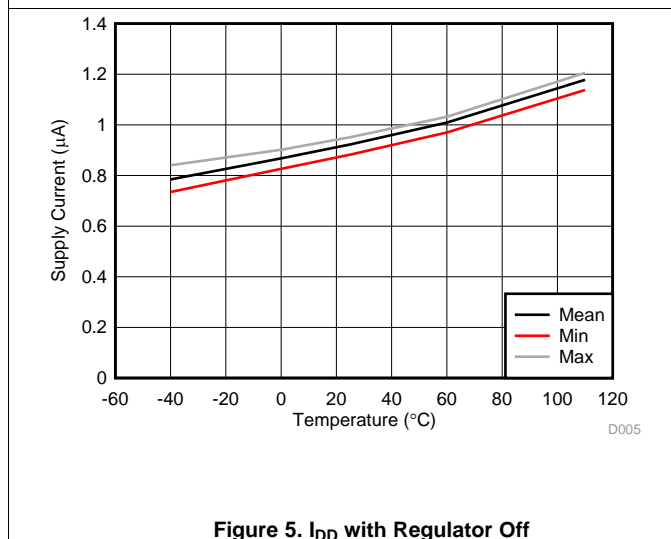
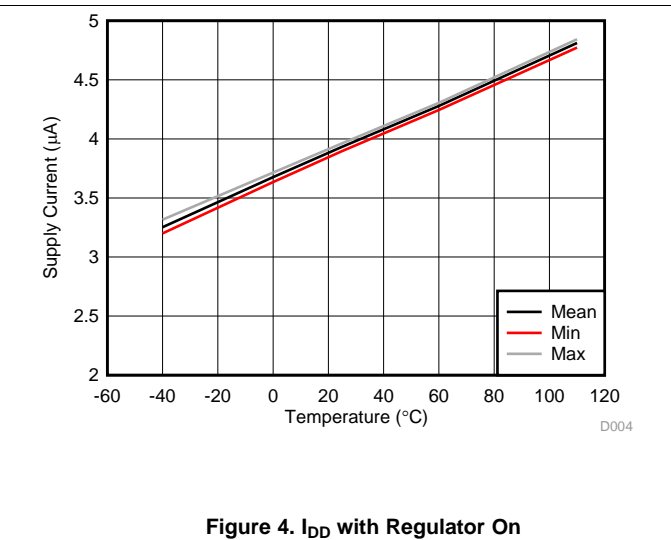
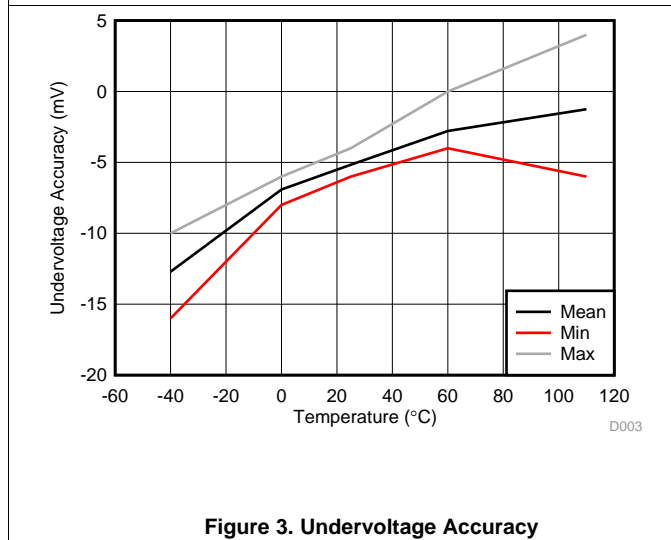
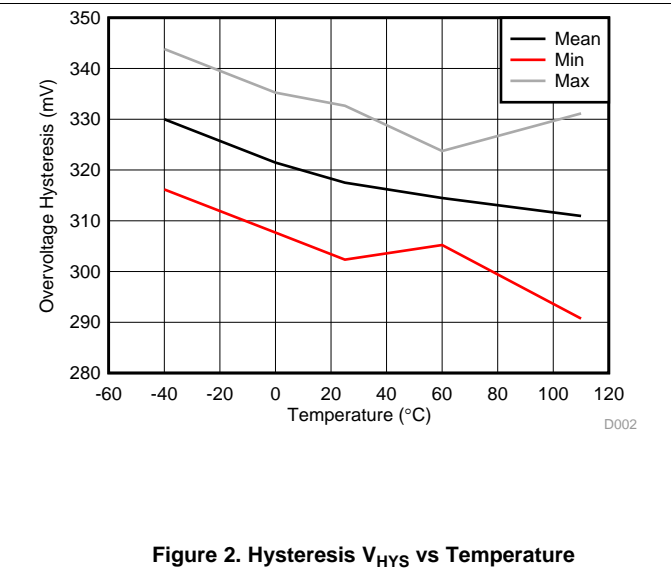
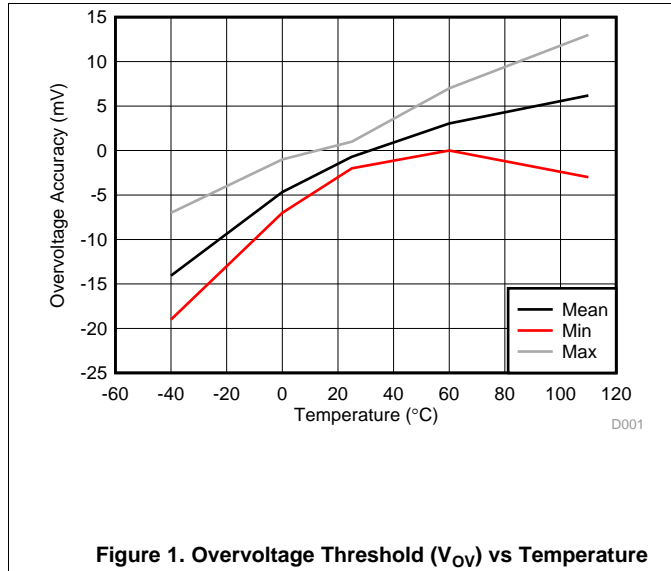
(1) Specified by design. Not 100% tested in production.

## Electrical Characteristics (continued)

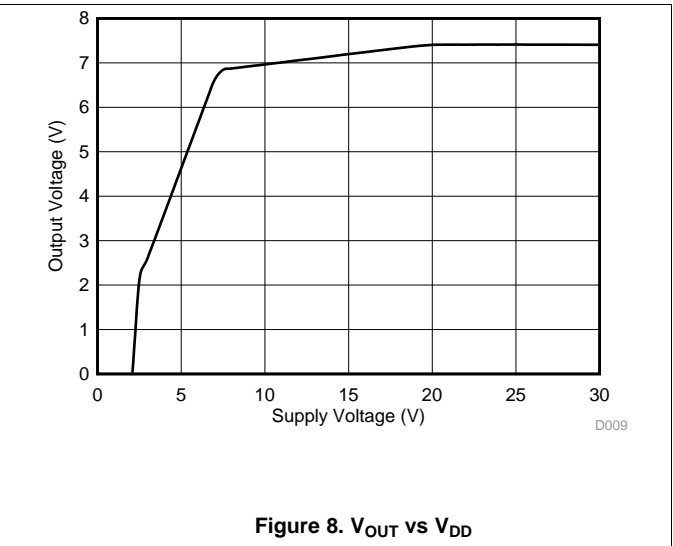
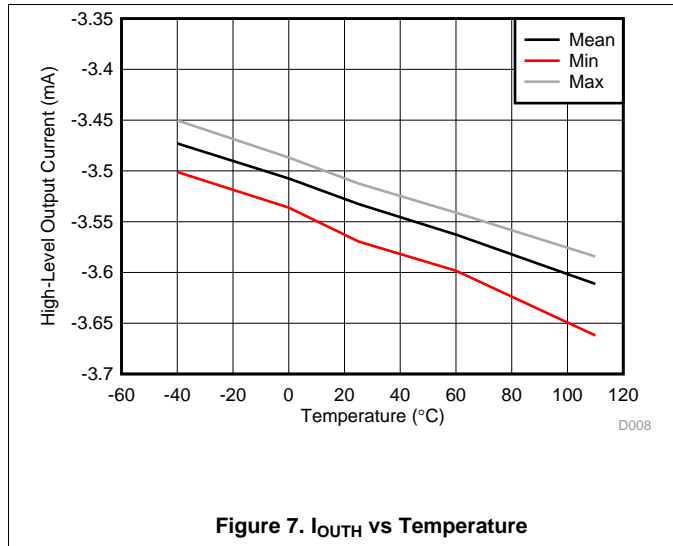
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 14.4\text{ V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $110^\circ\text{C}$ , and  $V_{DD} = 3\text{ V}$  to  $15\text{ V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>Regulated Supply Output, REG</b>							
$V_{REG}$	REG Supply	$V_{DD} \geq 4\text{ V}$ , $I_{REG} = 0\text{ }\mu\text{A}$ to $1\text{ mA}$ , $C_{REG} = 0.47\text{ }\mu\text{F}$	$V_{REG} = 3.3\text{ V}$ , bq2960, bq2961, bq2962	3.2	3.3	3.4	V
			$V_{REG} = 3.15\text{ V}$ , bq2962	3.05	3.15	3.25	V
			$V_{REG} = 3.0\text{ V}$ , bq2962	2.9	3	3.1	V
			$V_{REG} = 2.5\text{ V}$ , bq2960, bq2961	2.425	2.5	2.575	V
			$V_{REG} = 1.8\text{ V}$ , bq2960, bq2961	1.746	1.8	1.854	V
$I_{REG}$	REG Current Output	$V_{DD} \geq 4\text{ V}$ , $C_{REG} = 0.47\text{ }\mu\text{F}$		0	1	mA	
$I_{REG\_SC\_Limit}$	REG Output Short Circuit Current Limit	$REG = V_{SS}$ , $C_{REG} = 0.47\text{ }\mu\text{F}$		4		mA	
$R_{REG\_PD}$	REG pull-down resistor	REG is disabled		20	30	45	k $\Omega$
<b>Regulated Supply Output Enable, REG_EN</b>							
$V_{IH}$	High-level Input			1.6		V	
$V_{IL}$	Low-level Input				0.4	V	
$I_{LKG}$	Input Leakage Current	$V_{IH} < 6\text{ V}$			0.1	$\mu\text{A}$	
<b>Regulated Supply Undervoltage Self-disable</b>							
$V_{UVREG}$	Undervoltage detection	Factory Configuration: 2.0 V to 2.8 V in 50 mV steps, $T_A = 25^\circ\text{C}$		-50	50	mV	
$V_{UVHYS}$	Undervoltage Detection Hysteresis			250	300	400	mV
$t_{UVDELAY}$	Undervoltage Detection Delay			4.5	6	7.5	s
$V_{UVQUAL}$	Cell voltage to qualify for UV detection				0.5	V	

## 7.6 Typical Characteristics



**Typical Characteristics (continued)**



## 8 Detailed Description

### 8.1 Overview

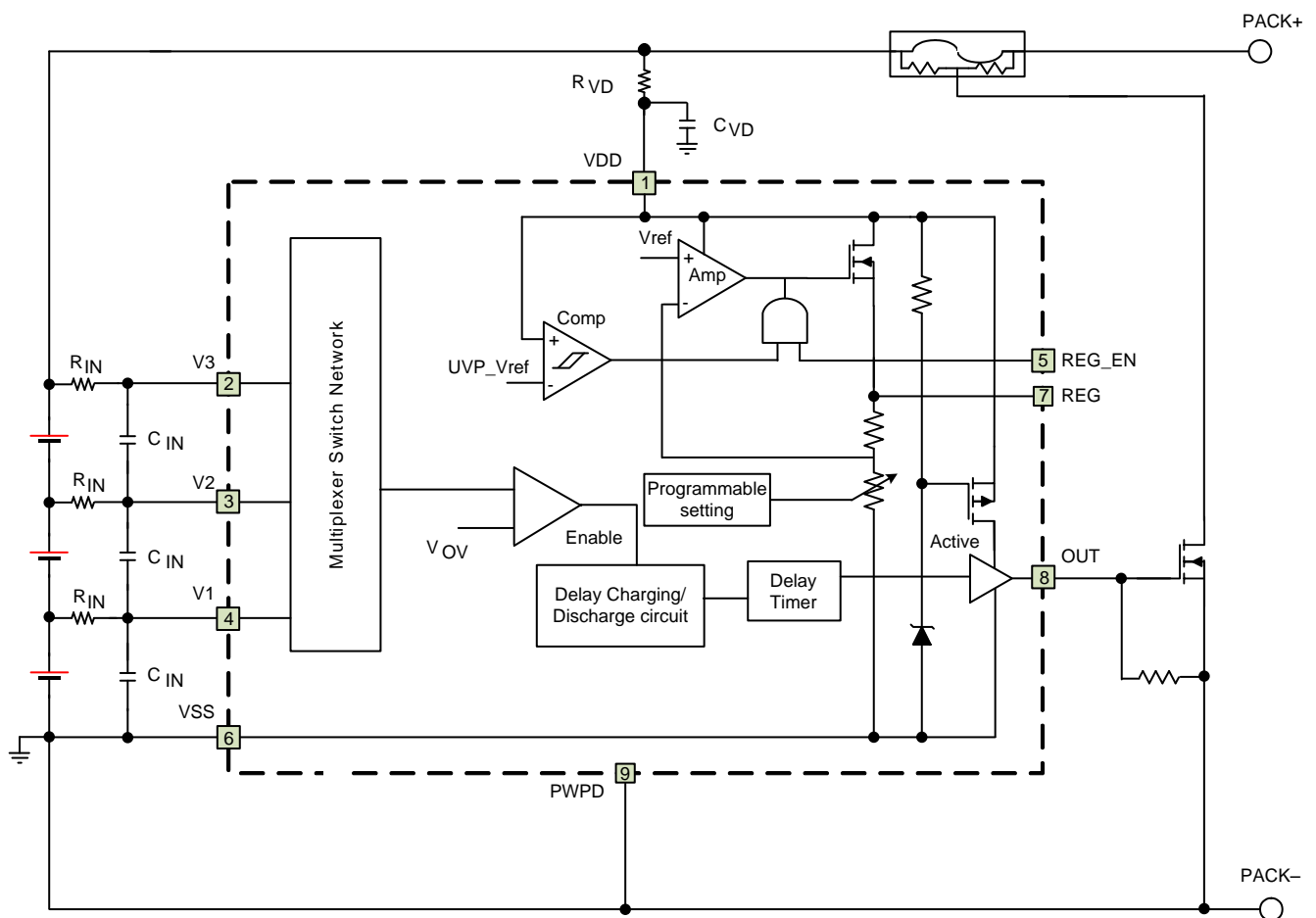
The bq2960, bq2961 and bq2962 are second-level overvoltage (OV) protectors with a regulated output. Each cell is monitored independently by comparing the actual cell voltage to an overvoltage threshold  $V_{OV}$ . The overvoltage threshold is preprogrammed at the factory with a range between 3.85 V to 4.65 V.

The regulated output is enabled unless any of the cell voltages fall below the  $V_{UVREG}$  threshold. This threshold is preprogrammed at the factory with a range between 2 V to 2.8 V. For bq2960xy family, an external control pin, REG\_EN, is available to enable or disable the regulated output in addition to the  $V_{UVREG}$  detection.

**Table 1. Programmable Parameters**

OVERVOLTAGE RANGE (V)	OVERVOLTAGE DELAY (s)	UNDERVOLTAGE RANGE (V)	REGULATOR (V)
3.85 to 4.6 in 50 mV step	3, 4, 5.5, 6.5	2.0 to 2.8 in 50 mV step	1.8, 2.5, 3.3 (bq2960, bq2961) 3.0, 3.15, 3.3 (bq2962)

### 8.2 Functional Block Diagram



**Figure 9. bq2960 Block Diagram**



## Feature Description (continued)

The REG output has protection for overcurrent, using a current limit protection circuit, and also detects and protects for excessive power dissipation due to short circuit of the external load. This pin requires a ceramic 1- $\mu$ F capacitor connection to VSS for improved stability, noise immunity, and ESD performance of the supply output. This capacitor must be placed close to the REG and VSS pins for connection.

### 8.3.1.5 Regulated Supply Output Enable, REG\_EN (bq2960 Only)

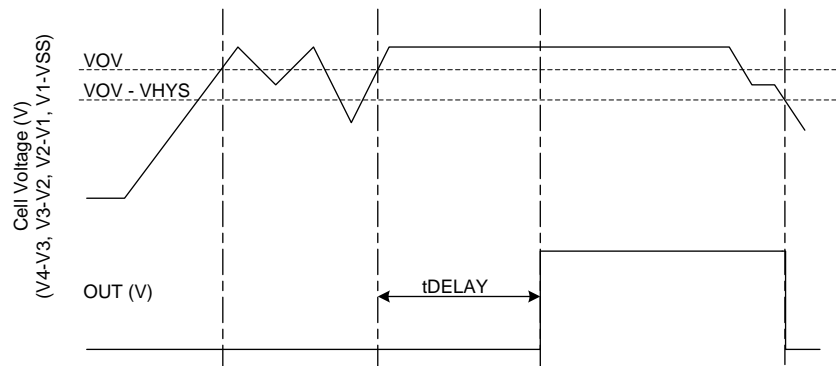
This terminal is a high voltage input drain to enable and disable the regulated supply output, REG terminal. When the VREG\_EN >  $V_{IH}$ , the REG terminal output is enabled including the cell undervoltage detection function to self-disable the regulated supply. When the VREG\_EN <  $V_{IL}$ , the REG terminal output, the cell undervoltage detection and the regulated supply self-disable functions are disabled.

To keep the REG output enabled at all times, the recommendation is to connect the REG\_EN to the V1 termination. There is a 6-V clamp to protect the REG\_EN terminal from a high voltage input. By connecting REG\_EN to V1, the clamp circuit is not active.

When the REG output is enabled, VREG\_EN >  $V_{IH}$ , the REG output can be self-disabled if any of the cell voltages are <  $V_{UVREG}$ . The self-disable function is used to reduce power consumption when the battery pack is deeply depleted.

### 8.3.2 Overvoltage Sensing for OUT

In the bq296xxx device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{OV}$ . If any cell voltage exceeds the programmed OV value, an internal timer circuit is activated. This timer circuit causes a factory pre-programmed fixed delay before the OUT terminal goes from inactive to active state.



**Figure 11. Timing for Overvoltage Sensing for OUT**

### 8.3.3 Regulated Output Voltage and REG\_EN Pin

For bq2960 and bq2961, there are three factory-preprogrammed options for the regulated output voltage, 3.3 V, 2.5 V, and 1.8 V. For bq2962, the regulated output voltage options are 3.3 V, 3.15 V, and 3.0 V. bq2962xy can potentially provide other regulated voltage output between 3.3 V to 3.0 V, contact Texas Instruments for detail.

At power up, the regulated output is on by default. If any cell voltage is below  $V_{UVREG}$  at device power up, the regulated output will remain on until the  $t_{UV\_DELAY}$  time has passed, the regulated out turns off after the delay time.

During discharge, if any cell voltage falls below the  $V_{UVREG}$  threshold for  $t_{UV\_DELAY}$  time, the regulated output is self-disabled. The regulated output turns on again when all the cell voltages are above  $V_{UVREG} + V_{UVHYS}$ .

Feature Description (continued)

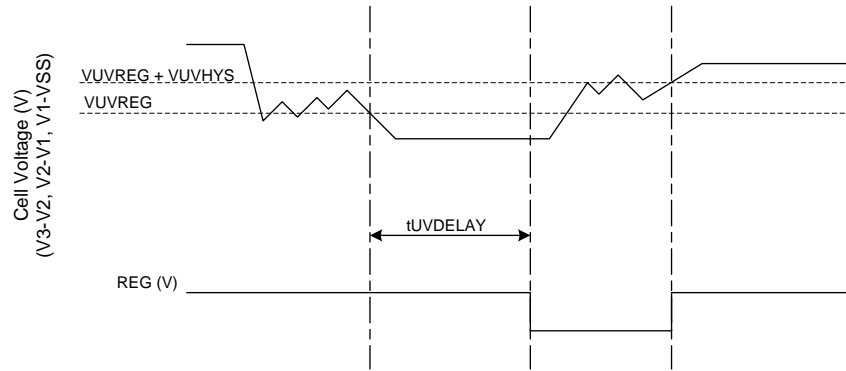


Figure 12. REG Output Timing

For bq2960 family, an external REG\_EN pin is available to enable and disable the regulated output function. To enable both the regulated output and the undervoltage self-disable features, the REG\_EN pin must be above  $V_{IH}$ . A microcontroller can be used to control the REG\_EN pin. Alternatively, connecting the REG\_EN pin to the bottom cell is another option to enable the regulated output function always.



## Device Functional Modes (continued)

### 8.4.3 UNDERVOLTAGE Mode

The UNDERVOLTAGE mode is detected if any of the cell voltage across (V1–VSS), (V2–V1), (V3–V2), or (V4–V3) is below the  $V_{UVREG}$  threshold for  $t_{UV\_DELAY}$  time. In this mode, the regulated output is disabled. To return to the NORMAL mode, all the cell voltages must be above  $(V_{UVREG} + V_{UVHYS})$ .

For a low cell configuration,  $V_n$  pin can be shorted to the  $(V_n - 1)$  pin. The device ignores any differential cell voltage below  $V_{UVQUAL}$  threshold for undervoltage detection.

### 8.4.4 CUSTOMER TEST MODE

The Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay-timer parameter once the circuit is implemented into the battery pack. To enter CTM, the VDD pin should be set at least 10 V higher than V3 (see Figure 14). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit CTM, remove the VDD to VC3 voltage differential of 10 V, so that the decrease in the value automatically causes an exit.

**CAUTION**

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the device into CTM. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V3–V2), (V2–V1) and (V1–VSS). Stressing the pins beyond the rated limits can cause permanent damage to the device.

Figure 14 shows the timing for the Customer Test Mode.

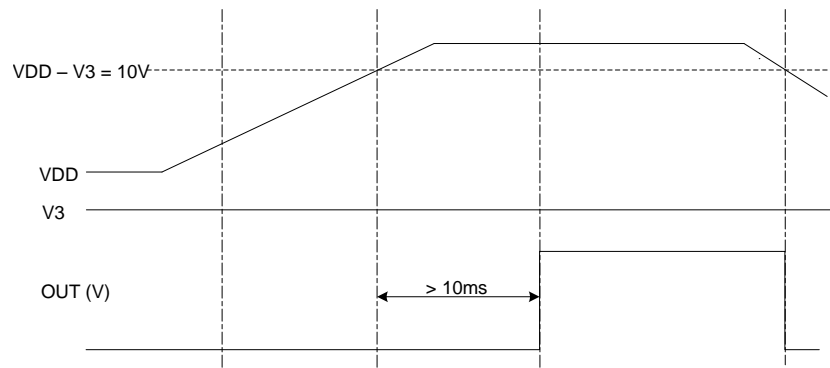


Figure 14. Timing for Customer Test Mode

Figure 15 shows the measurement for current consumption of the product for both VDD and  $V_x$ .

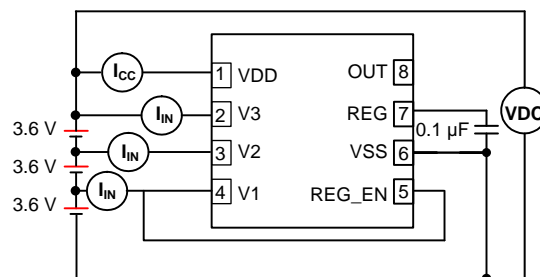


Figure 15. Configuration for Integrated Circuit Current Consumption Test

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The bq296xxx is a family of second-level protectors used for overvoltage protection of the battery pack in the application. A regulated output is available to drive a small circuit with maximum  $I_{REG}$  loading. The device OUT pin is active high, which drives a NMOS FET that connects the fuse to ground in the event of a fault condition. This provides a shorted path to use the battery and/or charger power to blow the fuse and cut the power path.

### 9.2 Typical Application

Figure 13 shows the recommended reference design components.

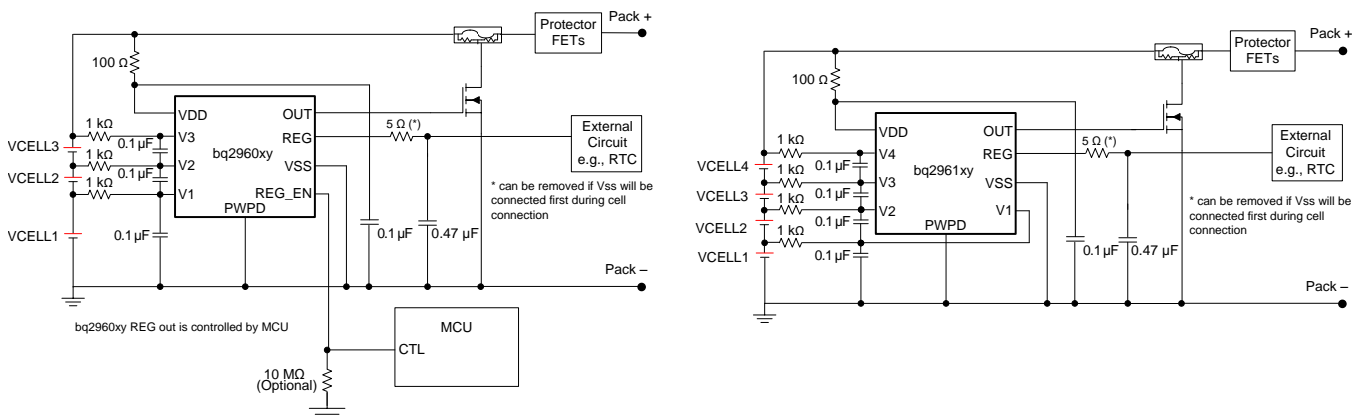


Figure 16. Application Schematic

#### 9.2.1 Design Requirements

### NOTE

Changes to the ranges stated in Table 2 will impact the accuracy of the cell measurements.

Table 2. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	$R_{IN}$	900	1000	4700	$\Omega$
Voltage monitor filter capacitance	$C_{IN}$	0.01	0.1	1.0	$\mu F$
Supply voltage filter resistance	$R_{VD}$	0.1	—	1	$K\Omega$
Supply voltage filter capacitance	$C_{VD}$	—	0.1	1.0	$\mu F$
REG output capacitance	$C_{REG}$	0.47	1	—	$\mu F$

### NOTE

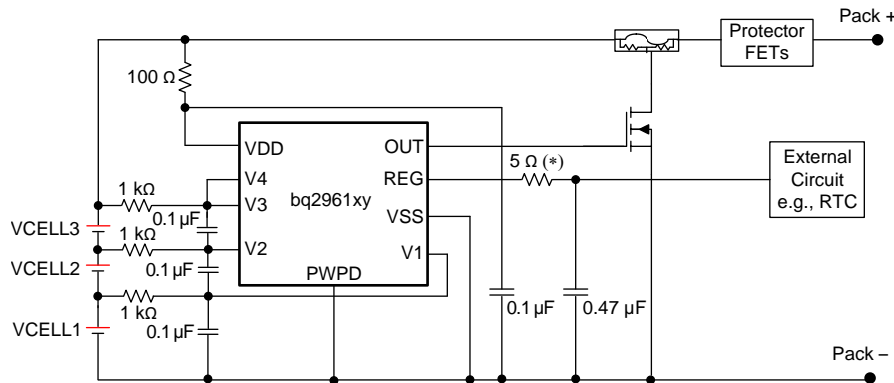
The device is calibrated using an  $R_{IN}$  value = 1 k $\Omega$ . Using a value other than the recommended value changes the accuracy of the cell voltage measurements and  $V_{OV}$  trigger level.

## 9.2.2 Detailed Design Procedure

### NOTE

The device VSS must be connected first during PCB test or cell attachment. Failure to do so can damage the REG pin.

1. If VSS pin cannot be connected first, it is required to add a resistor of a minimum of 5 ohms to a maximum of 10 ohms (a 5-ohm resistor is used in the reference schematic, [Figure 17](#)) in series with the REG capacitor. When VSS is floating, the REG capacitor always charges up to the VDD voltage. When VSS is finally connected, the REG capacitor will be discharged. Adding a small resistor in series reduces the current strength and avoids any potential damage to the REG pin. The 5-ohm resistor can be placed in series with the REG connect circuit (as shown in [Figure 17](#)) or in series of the REG capacitor (as shown in [Figure 18](#)). Placing the resistor in series with the REG circuit results in a small drop of VREG (for example: max loading of 1 mA with a 5-ohm resistor will drop 5 mV on VREG), but such a connection can protect against rush current discharge from both REG capacitor or external filter capacitor connected to the REG pin. Placing the resistor in series with the REG capacitor is an alternative to avoid additional drop in VREG if the filter capacitor used by the external circuit is much smaller than the REG capacitor.
2. After VSS is connected, the device allows random cell connect to the Vx pin.
3. Cell should be connected to the lower V<sub>n</sub> pin; the unused V<sub>n</sub> pin should be shorted to the (V<sub>n-1</sub>) pin. See [Figure 17](#) for details.



**Figure 17. 3-Series bq2961 Schematic (also apply to bq2962)**

4. A zener diode can be added to the REG pin to VSS as shown in [Figure 18](#). This is recommended to protect the circuit connected to the REG pin if floating VSS in the field is a risk concern. When VSS is floating (during cell connection when VSS is not connected first or in system fault with BAT– wire broken), the REG voltage always pulls up to VDD. In a 4-S configuration, the REG voltage can reach approximately 16 V with VSS floating. Adding a zener diode clamps the REG voltage to a safe level for the external circuits connected to the REG pin. Having the zener diode can also protect the external circuits if REG pin is shorted to OUT pin or any other high-voltage output terminal. If a zener diode is used, TI recommends putting the diode on the battery side with the bq296xxx device to allow protection on both the REG pin as well as the circuit connected to REG under floating VSS condition. The resistor in series with the REG pin is not required in this case.

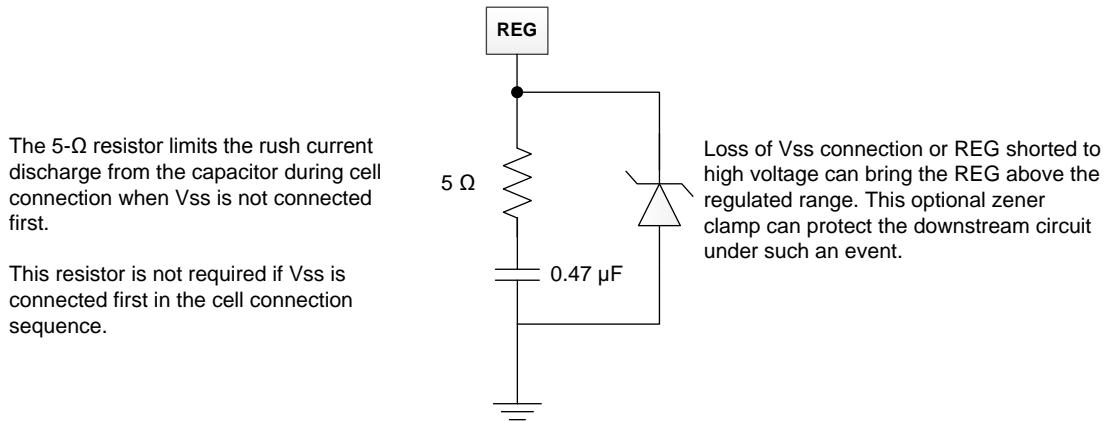


Figure 18. 5-V Zener Diode

- For 2- to 3-series applications, if an external control for the regulated output is required, select the bq2960xy family. Otherwise, select the bq2961xy family.

### 9.2.3 Application Curves

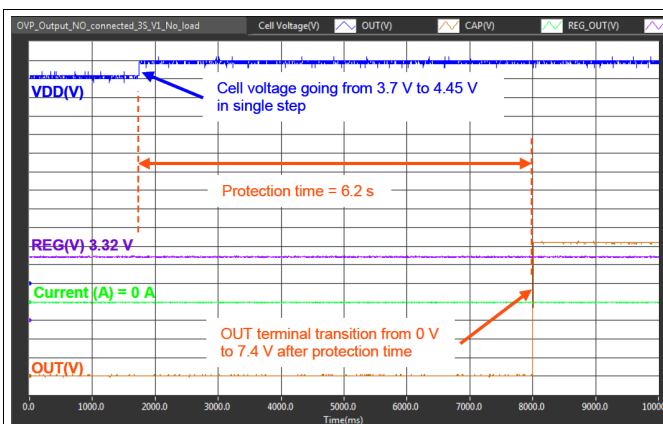


Figure 19. Overvoltage Protection

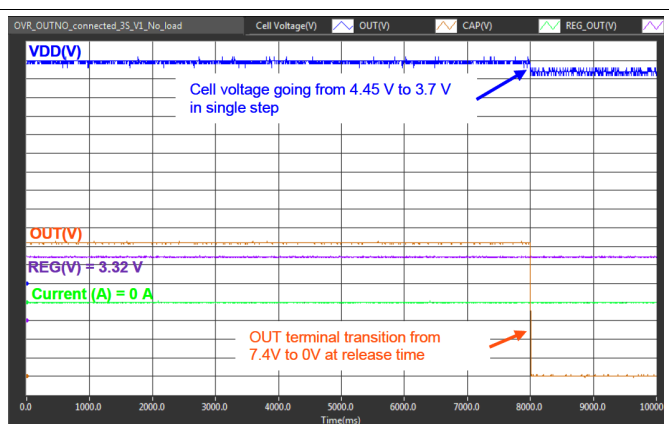


Figure 20. Overvoltage Protection Release

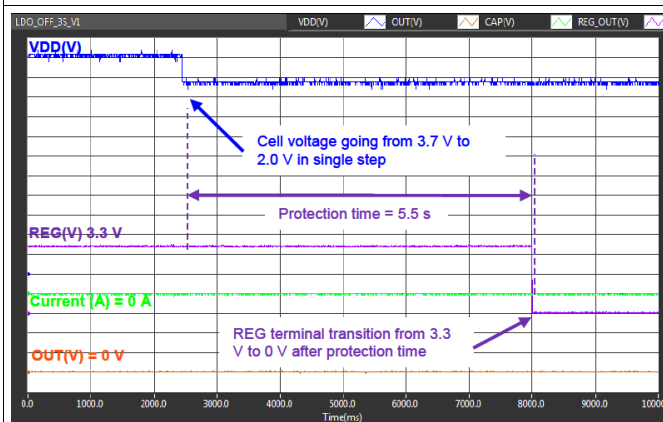


Figure 21. Undervoltage Detection to Turn off Regulator

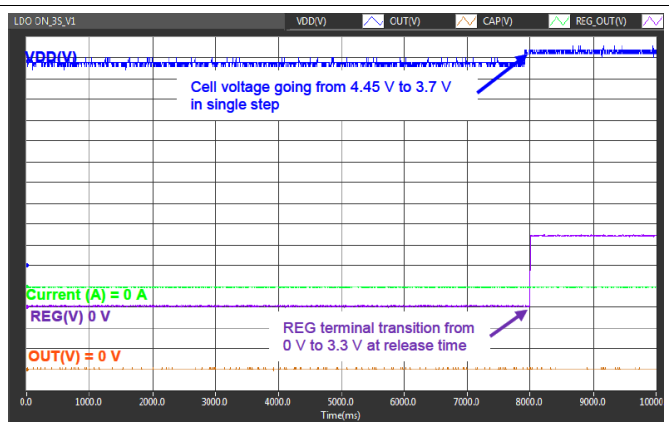


Figure 22. Undervoltage Release to Switch on Regulator

9.2.4 Other Schematics

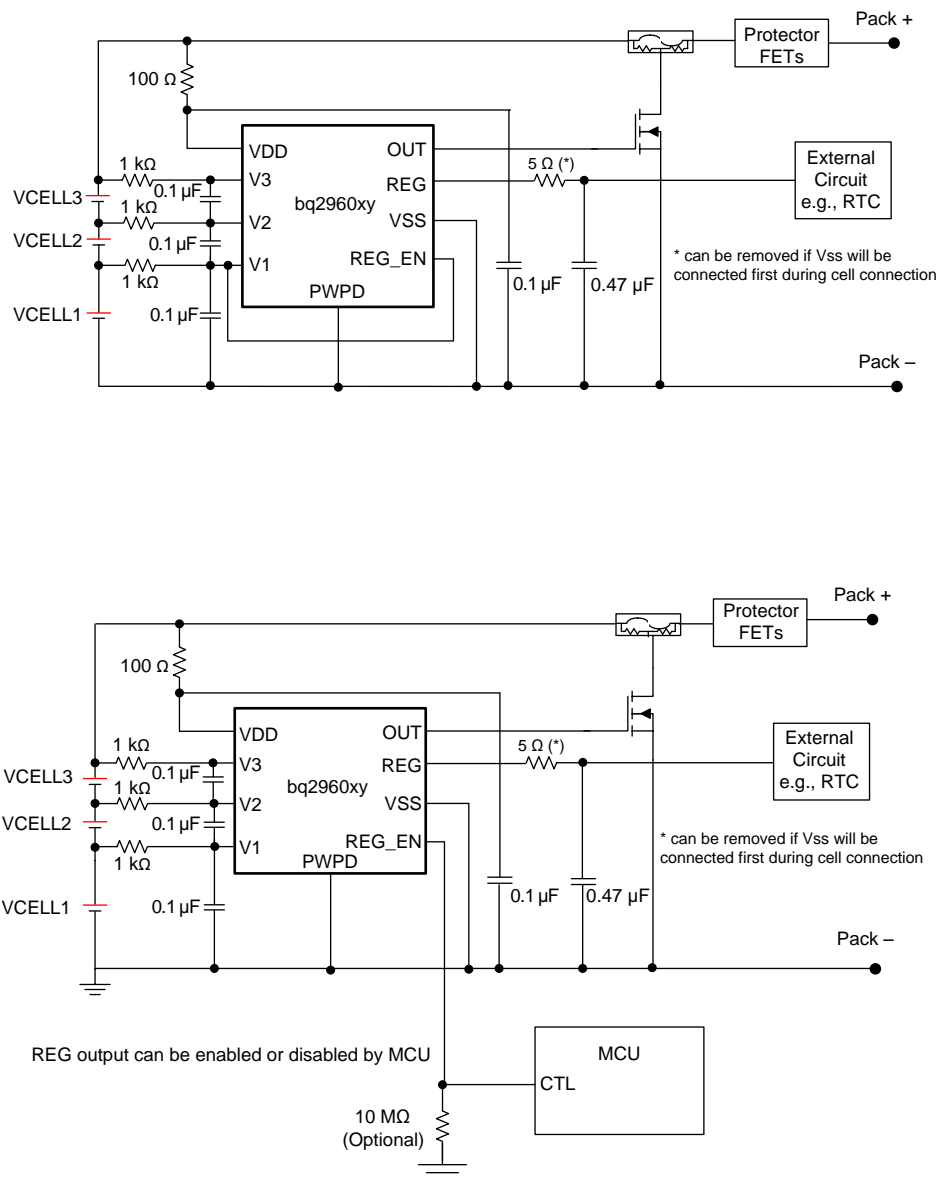
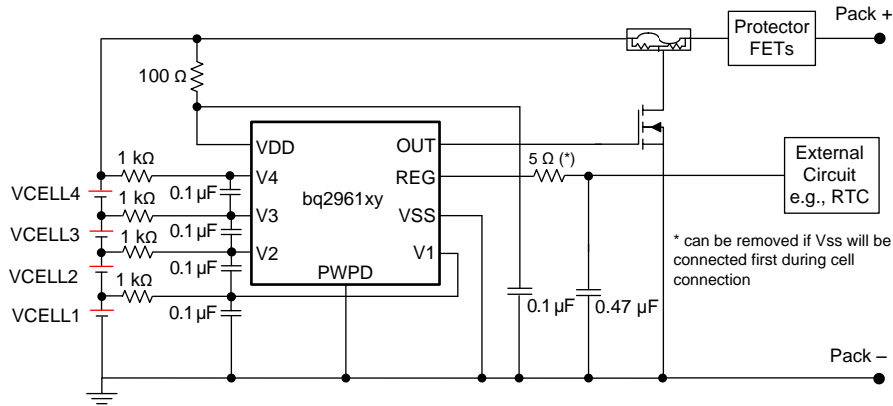


Figure 23. bq2960 Schematic with REG Output Always Enabled



**Figure 24. bq2961 Schematic (also apply to bq2962)**

## 10 Power Supply Recommendations

The maximum power is 15 V for bq2960 and 20 V for bq2961 and bq2962 on VDD.

### NOTE

Connect VSS first during power up.

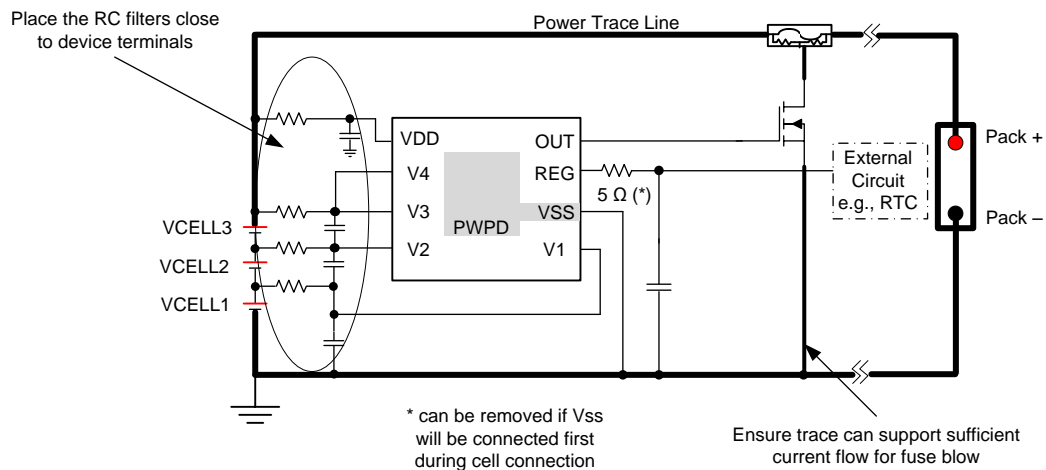
## 11 Layout

### 11.1 Layout Guidelines

Use the following layout guidelines.

1. Ensure the RC filters for the V<sub>x</sub> pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for REG should be placed close to the device terminals.
3. Ensure the trace connecting the fuse to the gate, source of the NFET to the Pack– is sufficient to withstand the current during a fuse blown event.

### 11.2 Layout Example



**Figure 25. Layout Example**

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296103DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	<a href="#">Samples</a>
BQ296103DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6103	<a href="#">Samples</a>
BQ296106DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	<a href="#">Samples</a>
BQ296106DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6106	<a href="#">Samples</a>
BQ296107DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	<a href="#">Samples</a>
BQ296107DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6107	<a href="#">Samples</a>
BQ296111DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	<a href="#">Samples</a>
BQ296111DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6111	<a href="#">Samples</a>
BQ296112DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	<a href="#">Samples</a>
BQ296112DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6112	<a href="#">Samples</a>
BQ296113DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	<a href="#">Samples</a>
BQ296113DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6113	<a href="#">Samples</a>
BQ296114DSGR	ACTIVE	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	<a href="#">Samples</a>
BQ296114DSGT	ACTIVE	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 110	6114	<a href="#">Samples</a>
BQ296202DSGR	PREVIEW	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6202	
BQ296202DSGT	PREVIEW	WSO	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6202	
BQ296203DSGR	PREVIEW	WSO	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6203	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ296203DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6203	
BQ296212DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6212	
BQ296212DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6212	
BQ296213DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6213	
BQ296213DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	6213	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

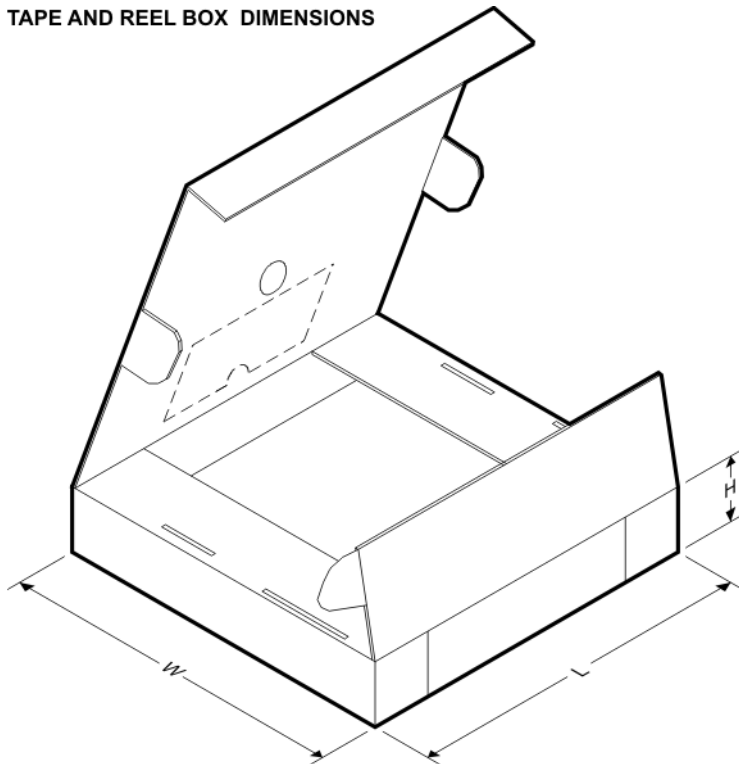
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296103DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296103DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296106DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296107DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296111DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296112DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296113DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296113DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296114DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296202DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296203DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ296212DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296212DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ296213DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS



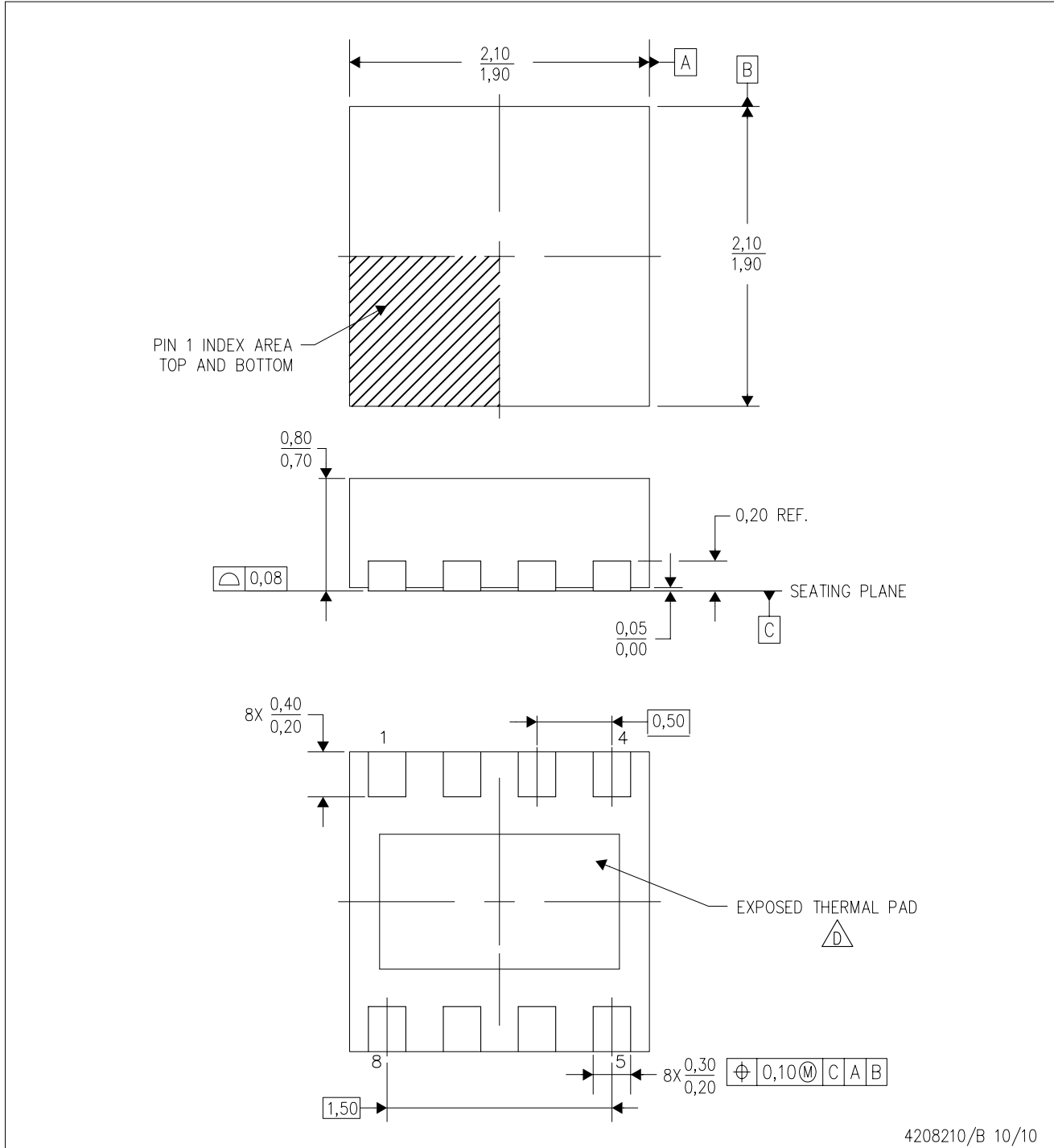
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296103DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296103DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296106DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296106DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296107DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296107DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296111DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296111DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296112DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296112DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296113DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296113DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296114DSGR	WSON	DSG	8	3000	210.0	185.0	35.0


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ296114DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296202DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296202DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296203DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296203DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296212DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296212DSGT	WSON	DSG	8	250	210.0	185.0	35.0
BQ296213DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
BQ296213DSGT	WSON	DSG	8	250	210.0	185.0	35.0

DSG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4208210/B 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-229.

## THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

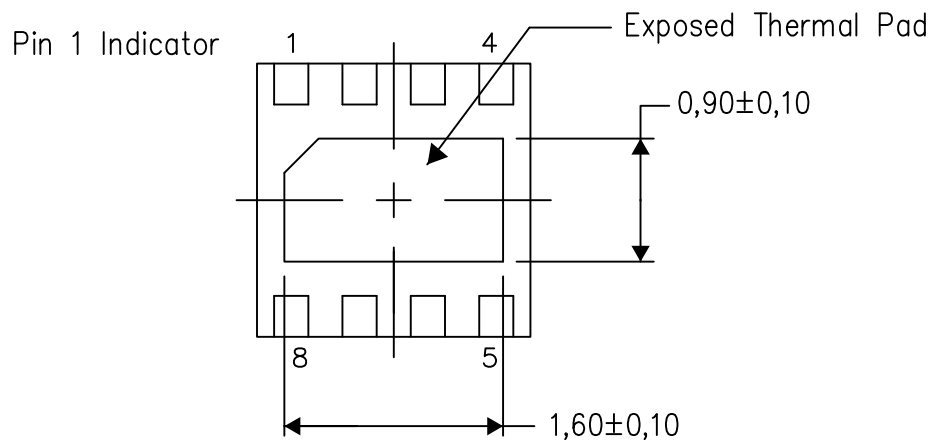
PLASTIC SMALL OUTLINE NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4208347/1 06/15

NOTE: All linear dimensions are in millimeters



## IMPORTANT NOTICE

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