Keysight M3300A

PXIe Arbitrary Waveform Generator and Digitizer Combo with Optional Real-Time Sequencing and FPGA Programming

500 MSa/s, 16 Bits, 2/4 Channel AWG + 100 MSa/s, 14 Bits, 4/8 Channel Digitizer

Data Sheet

KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

Fast, Flexible, High-Performance Control, Testing and Prototyping

The M3300A combines high-performance with arbitrary waveform generator channels and digitizer channels in the same module providing the ideal tool for testing and prototyping in control or communications applications. Performance meets simplicity thanks to easy-to-use programming libraries, real-time sequencing technology (Hard Virtual Instrumentation or HVI), and graphical FPGA programming technology.

Features

Outputs (AWG)
- 500 MSa/s, 16 Bits, 2/4 Channels

Inputs (digitizer)
- 100 MSa/s, 14 Bits, 4/8 Channels

Output features
- AWGs, function generators, AM/FM/PM modulators
- Advanced triggering and marking functionalities

Input features
- Powerful data acquisition system (DAQ)
- Advanced triggering and marking functionalities

Less than 400 ns input to output latency

Optional HW programming for high-performance applications
- Real-time sequencing (HVI technology)
- FPGA programming
  - Xilinx Kintex-7 325T or 410T FPGA

Up to 2 GB of onboard RAM (~ 1 Gsamples)

Mechanical/interface
- 2 slots 3U (PXIe)
- Up to 1.6 GB/s transfer BW with P2P capabilities (PCIe Gen 2)
- Independent DMA channels for fast and efficient data transfer

Applications

General purpose AWGs & digitizers

High-performance control

Communications: BB/IF SDR, channel emulation, transceiver testing

Aerospace & defense (A/D): RADAR, electronic warfare (EW)

Hardware-in-the-loop (HIL), automated test equipment (ATE)

Scientific research

Quantum computing

Programming technology and software tools

Software programming

- Easy-to-use native programming libraries for most common languages: C, C++, Visual Studio, LabVIEW, MATLAB, Python, and more

Hardware programming (optional)

- Real-time sequencing (Hard Virtual Instrumentation or HVI technology)
  - Graphical flowchart-style M3601A design environment (-HV1 option required on HW)
  - Ultra-fast, fully-parallelized, hard real-time execution
  - Ultra-fast, time-deterministic decision-making
  - Off-the-shelf inter-module synchronization & data exchange
- FPGA programming
  - Graphical M3602A FPGA design environment (-FP1 option required on HW)
  - No FPGA know-how required
  - Include high-level to low-level design elements: off-the-shelf DSP blocks, MATLAB/ Simulink designs, Xilinx CORE Generator IP cores, Xilinx VIVADO/ISE projects, VHDL or Verilog code
  - Ultra-fast, one-click compiling and on-the-fly programming

No programming

- Ready-to-use SD1 SPF (software front panels)

M31XX/M32XX/M33XX family product table

Product	Type	Outputs (AWGs)				Inputs (Digitizers)			
		Speed (MSa/s)	Bits	Ch	BW (MHz)	Speed (MSa/s)	Bits	Ch	BW (MHz)
M3202A	AWG	1000	14	2/4	DC-400				
M3201A	AWG	500	16	2/4	DC-200				
M3102A	Digitizer					500	14	2/4	DC-200
M3100A	Digitizer					100	14	4/8	DC-100
M3302A	Combo	500	16	2	DC-200	500	14	2	DC-200
M3300A	Combo	500	16	2/4	DC-200	100	14	4/8	DC-100

Functional block diagram

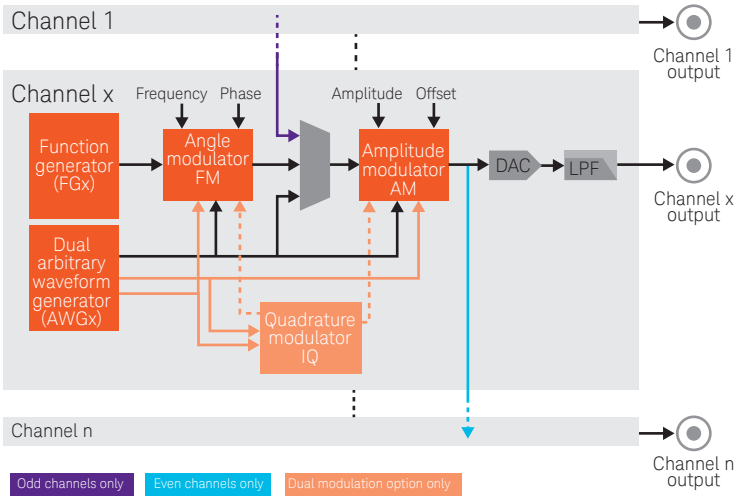


Figure 1. M3300A output functional block diagram, all channels have identical output structure

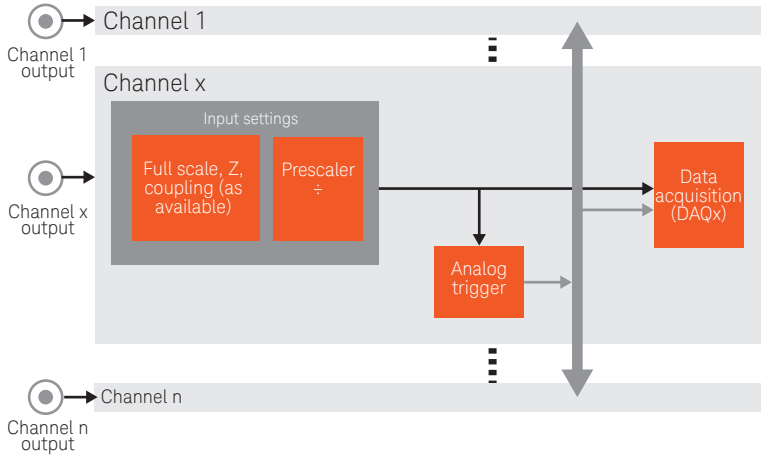


Figure 2. M3300A input functional block diagram, all channels have identical input structure

Ordering information

Product	Description
M3300A	PXI combo AWG + digitizer: 500/100 MSa/s, 16/14 bits
Options	**Description**
M3300A-C24 / -C48	√ Two channels AWG + four channels DIG / four channels AWG + eight channels DIG
M3300A-CLF	√ Fixed sampling clock, low jitter
M3300A-DM1	Dual modulation capability for the AWG (amplitude and angle simultaneously)
M3300A-M01 / -M12 / -M20	√ Memory 16 MB, 8 MSamples / 128 MB, 60 MSamples / 2 GB, 1 GSamples
HW programming options	**Description**
M3300A-HVI	Enabled HVI programming, requires an HVI design environment license (M3601A)
M3300A-FP1	Enabled FPGA programming, requires -K32 or -K41 option and an FPGA design environment license (M3602A)
M3300A-K32 / -K41	FPGA, Xilinx 7K325T / 7K410T, required for -FP1 option only (needs memory option -M20)

All options must be selected at time of purchase and are not upgradable
√ These options represent the standard configuration

Related software	Description
M3601A	HVI design environment
M3602A	FPGA design environment

Output specifications (AWG)

Specifications summary

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
Inputs and outputs								
Channels (single-ended mode)		2			4		Out	
Channels (differential mode)		1			2		Out	Differential uses 2 channels
Reference clock[1]		1			1		Out	
Reference clock[2]		1			1		In	
Triggers/markers[1, 3]		1			1		In/out	Reconfigurable
Triggers/markers[2, 3]		8			8		In/out	Reconfigurable
Output channels overview								
Sampling rate		500			500		MSa/s	Fixed sampling clock
Voltage resolution		16			16		Bits	
Output frequency	DC		200	DC		200	MHz	
Real-time BW			200			200	MHz	
Output voltage	–1.5		1.5	–1.5		1.5	Volts	
Built-in functionalities								
Function generators		2			4			1 per channel
Dual AWGs		2			4			1 per channel
IQ modulators		2			4			1 per channel
Frequency modulators		2			4			1 per channel
Phase modulators		2			4			1 per channel
Amplitude modulators		2			4			1 per channel
DC offset modulators		2			4			1 per channel
Onboard memory								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later

Table 1. General specifications

I/O specifications

	M3300A-C24			M3300A-C48				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Comments**
Output channels								
Sampling rate		500			500		MSa/s	Fixed sampling clock
Output frequency	DC		200	DC		200	MHz	Limited by a reconstruction filter
Output voltage	–1.5		1.5	–1.5		1.5	Volts	On a 50 Ω load
Source impedance		50			50		Ω	
Reference clock output								
Frequency		10 or 100			10 or 100		MHz	Generated from the internal clock, user selectable
Voltage		800			800		mV_{pp}	On a 50 Ω load
Power		2			2		dBm	On a 50 Ω load
Source impedance		50			50		Ω	AC coupled
External I/O trigger/marker								
V_{IH}	2		5	2		5	V	
V_{IL}	0		0.8	0		0.8	V	
V_{OH}	2.4		3.3	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	0		0.5	V	On a high Z load
Input impedance		10			10		K Ω	
Source impedance		TTL			TTL		–	
Speed			500			500	Mbps	

Table 2. Input/output specifications

Function generators (FGs) specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Function generators		2			4		–	1 per channel
Waveform types		4			4		–	Sinusoidal, triangular, square and DC
Frequency range	0		200	0		200	MHz	
Frequency resolution		45			45		Bits	
Frequency resolution		5.7			5.7		µHz	
Phase range	0		360	0		360	Deg	
Phase resolution		24			24		Bits	
Phase resolution		21.5			21.5		µdeg	
Speed performance								
Frequency change rate			100			100	MChanges/s	With HVI technology
Frequency modulation rate			500			500	MSamples/s	With AWGs and angle modulators
Phase change rate			100			100	MChanges/s	With HVI technology
Phase modulation rate			500			500	MSamples/s	With AWGs and angle modulators

Table 3. Function generators (FGs) specifications

Amplitude and offset specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Amplitude/offset range	–1.5		1.5	–1.5		1.5	Volts	Amplitude + offset values
Amplitude/offset resolution		16			16		Bits	
Amplitude/offset resolution		45.8			45.8		µV	
Speed performance								
Amplitude/offset change rate			500			500	MChanges/s	With HVI technology
Amplitude/offset modulation rate			500			500	MSamples/s	With AWGs and amplitude modulators

Table 4. Amplitude and offset specifications

Arbitrary waveform generators (AWGs) specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Dual AWGs		2			4			1 Dual AWG per output channel
Aggregated speed (16 bits)			2000			4000	MSa/s	For all onboard waveforms combined
Aggregated speed (32 bits)			1000			2000	MSa/s	For all onboard waveforms combined
Waveform multiple		5			5		Samples	Waveform length must be a multiple of this value
16-bit waveform length	15		957M	15		957M	Samples	Maximum depends on onboard RAM
32-bit waveform length	10		478M	10		478M	Samples	Maximum depends on onboard RAM
Waveform length efficiency		93.5			93.5		%	Effic. = waveform size/waveform size in RAM
Trigger		Selec.			Selec.			External Trigger (input connector, backplane triggers), software trigger
AWG specifications (16-bit single waveform)								
Speed			500			500	MSa/s	Per AWG
Resolution		16			16		Bits	
AWG destination		Selec.			Selec.			Amplitude, offset, frequency or phase
AWG specifications (16-bit dual waveform)								
Speed (waveform A)			500			500	MSa/s	Per AWG
Speed (waveform B)			500			500	MSa/s	Per AWG
Resolution (waveform A)		16			16		Bits	
Resolution (waveform B)		16			16		Bits	
AWG destination (waveform A)		Selec.			Selec.			Amplitude, offset or I
AWG destination (waveform B)		Selec.			Selec.			Frequency, phase or Q
AWG specifications (32-bit single waveform)								
Speed			100			100	MSa/s	Per AWG, minimum prescaler: 1
Resolution		32			32		Bits	
AWG destination		Selec.			Selec.			Amplitude, offset, frequency or phase
AWG specifications (32-bit dual waveform)								
Speed (waveform A)			100			100	MSa/s	Per AWG, minimum prescaler: 1
Speed (waveform B)			100			100	MSa/s	Per AWG, minimum prescaler: 1
Resolution (waveform A)		32			32		Bits	
Resolution (waveform B)		32			32		Bits	
AWG destination (waveform A)		Selec.			Selec.			Amplitude or offset
AWG destination (waveform B)		Selec.			Selec.			Frequency or phase

Table 5. Arbitrary waveform generators (AWGs) specifications

Angle modulators specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Frequency modulators		2			4			1 per output channel
Phase modulators		2			4			1 per output channel
Carrier signal source		FGs			FGs			Table 3 on page 8
Modulating signal source		AWGs			AWGs			Table 5 on page 9
Frequency modulators (16-bit modulating waveform)								
Deviation	–Dev. gain		+Dev. gain	–Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		200	0		200	MHz	
Deviation gain resolution		16			16		Bits	
Frequency modulators (32-bit modulating waveform)								
Deviation	–Dev. gain		+Dev. gain	–Dev. gain		+Dev. gain	MHz	
Modulating signal resolution		32			32		Bits	AWG waveform
Modulating signal BW	0		50	0		50	MHz	AWG Nyquist limit
Deviation gain	0		200	0		200	MHz	
Deviation gain resolution		16			16		Bits	
Phase modulators (16-bit modulating waveform)								
Deviation	–Dev. gain		+Dev. gain	–Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		180	0		180	Deg	
Deviation gain resolution		16			16		Bits	~ 5.5 mdeg
Phase modulators (32-bit modulating waveform)								
Deviation	–Dev. gin		+Dev. gain	–Dev. gain		+Dev. gain	Deg	
Modulating signal resolution		16			16		Bits	AWG waveform is truncated
Modulating signal BW	0		50	0		50	MHz	AWG Nyquist limit
Deviation gain	0		180	0		180	Deg	
Deviation gain resolution		16			16		Bits	~ 5.5 mdeg

Table 6. Angle modulators specifications

Amplitude modulators specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Amplitude modulators		2			4			1 per output channel
Offset modulators		2			4			1 per output channel
Carrier signal source		FGs			FGs			Table 3 on page 8
Modulating signal source		AWGs			AWGs			Table 5 on page 9
Amplitude & offset modulators (16-bit modulating waveform)								
Deviation	–Dev. gain		+Dev. gain	–Dev. gain		+Dev. gain	V_p	
Modulating signal resolution		16			16		Bits	AWG waveform
Modulating signal BW	0		250	0		250	MHz	AWG Nyquist limit
Deviation gain	0		1.5	0		1.5	V_p	
Deviation gain resolution		16			16		Bits	Limited by the output DAC
Amplitude & offset modulators (32-bit modulating waveform)								
Deviation	–Dev. gain		+Dev. gain	–Dev. gain		+Dev. gain	Vp	
Modulating signal resolution		16			16		Bits	AWG waveform is truncated
Modulating signal BW	0		50	0		50	MHz	AWG Nyquist limit
Deviation gain	0		1.5	0		1.5	V_p	
Deviation gain resolution		16			16		Bits	Limited by the output DAC

Table 7. Amplitude modulators specifications

IQ Modulators Specifications

Parameter	M3300A Min	Typ	Max	Units	Comments
General specifications					
IQ modulators		2			1 per output channel
Carrier signal source		FGs			Table 3 on page 8
Modulating signal source		AWGs			Table 5 on page 9
External I/O trigger/marker					
Amplitude deviation	–1.5		1.5	Vp	
Phase deviation	–180		180	Deg	
I modulating signal resolution		16		Bits	AWG waveform
I modulating signal BW	0		250	MHz	AWG Nyquist limit
Q modulating signal resolution		16		Bits	AWG waveform
Q modulating signal BW	0		250	MHz	AWG Nyquist limit

Table 8. IQ modulators specifications

Clock system specifications

Parameter	M3300A-C24 Min	Typ	Max	M3300A-C48 Min	Typ	Max	Units	Comments
General specifications								
Clock frequency		500			500		MHz	Fixed sampling clock

Table 9. Clock system specifications

AC performance

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Analog output jitter			<2			<2	ps	RMS (cycle-to-cycle)
AWG trigger to output jitter			<2			<2	ps	RMS (cycle-to-cycle) for any trigger referenced to the chassis clock; independent of input trigger jitter if input jitter < 4nS peak-to-peak
Trigger resolution		10			10		ns	
Channel-to-channel skew			<20			<20	ps	Between ch 0 & ch 1, and ch 2 & ch 3
			<50			<50	ps	Between any channel
			150			150	ps	Between modules, chassis dependant [2]
Clock output jitter			<2			<2	ps	RMS (cycle-to-cycle)
Clock accuracy and stability			25			25	ppm	PXIe, cPCIe versions; chassis dependent[1].
AC specifications								
Spurious-free dynamic range (SFDR)								P_{out} = 4 dBm, measured from DC to max frequency
f_{out} = 10 MHz		63			63		dBc	
f_{out} = 40 MHz		63			63		dBc	
f_{out} = 80 MHz		64			64		dBc	
f_{out} = 120 MHz		69			69		dBc	
f_{out} = 160 MHz		67			67		dBc	
f_{out} = 200 MHz		63			63		dBc	
Crosstalk (adjacent channels)								
f_{out} = 10 MHz		<–105			<–105		dB	
f_{out} = 40 MHz		–85			–85		dB	
f_{out} = 80 MHz		–75			–75		dB	
f_{out} = 120 MHz		–88			–88		dB	
f_{out} = 160 MHz		–73			–73		dB	
f_{out} = 200 MHz		–85			–85		dB	
Crosstalk (non-adjacent channels)								
f_{out} = 10 MHz		<–105			<–105		dB	
f_{out} = 40 MHz		–86			–86		dB	
f_{out} = 80 MHz		–78			–78		dB	
f_{out} = 120 MHz		<–105			<–105		dB	
f_{out} = 160 MHz		–92			–92		dB	
f_{out} = 200 MHz		–100			–100		dB	
Phase noise (SSB)								
offset = 1 KHz		<–127			<–127		dBc/Hz	
offset = 10 KHz		<–133			<–133		dBc/Hz	
offset = 100 KHz		<–138			<–138		dBc/Hz	
Average noise power density		<–142			<–142		dBm/Hz	

1. This value corresponds to a M9505A chassis. This value can be improved with an external chassis clock or a system timing module.
2. This value corresponds to a M9005A PXIe chassis.

Table 10. AC performance

AC performance graphs

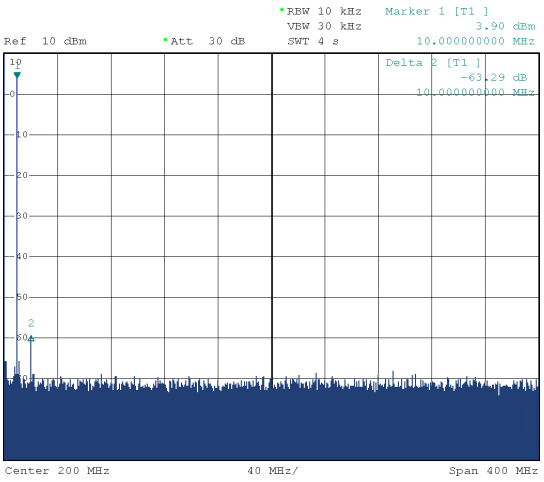


Figure 3. Single-tone spectrum @ f_{out} = 10 MHz

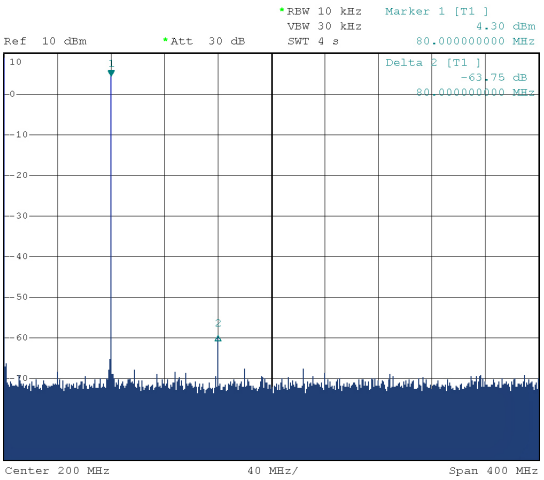


Figure 4. Single-tone spectrum @ f_{out} = 80 MHz

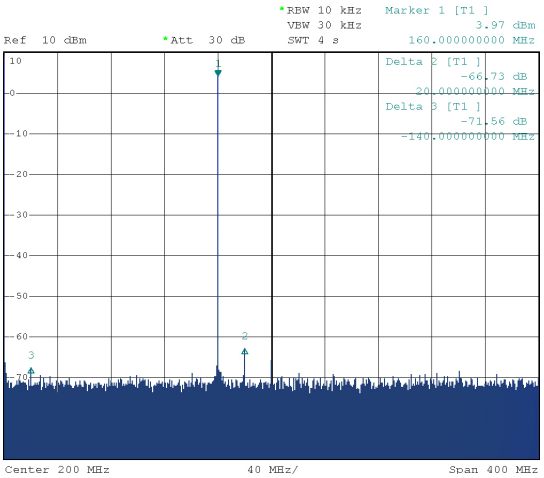


Figure 5. Single-tone spectrum @ f_{out} = 160 MHz

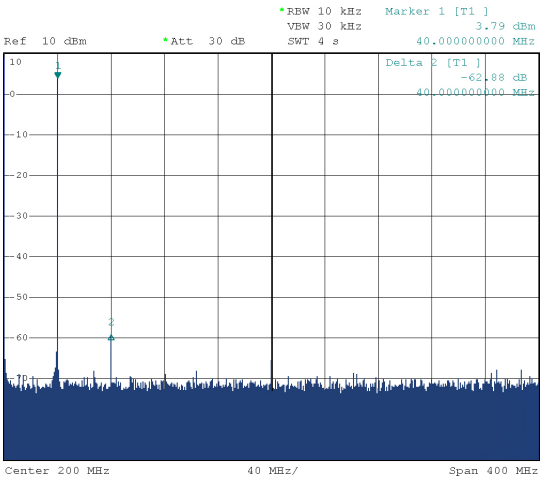


Figure 6. Single-tone spectrum @ f_{out} = 40 MHz

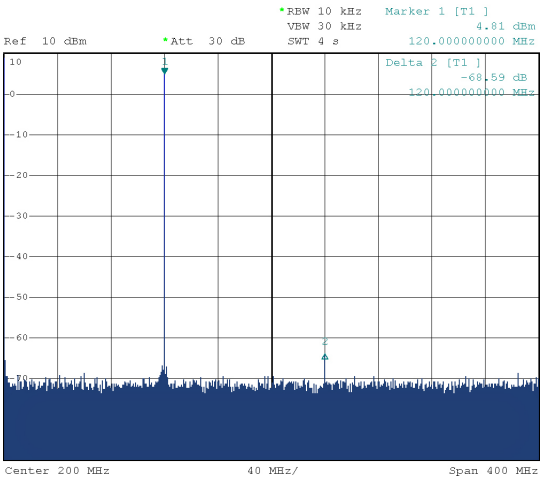


Figure 7. Single-tone spectrum @ f_{out} = 120 MHz

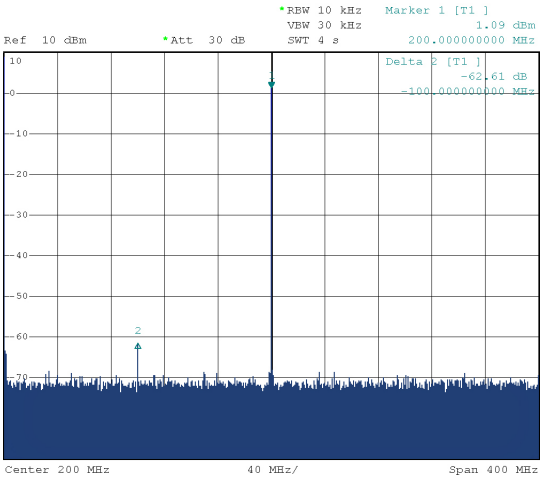


Figure 8. Single-tone spectrum @ f_{out} = 200 MHz

Input specifications (digitizer)

Specifications summary

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
Inputs and outputs								
Channels		4			8		Out	
Reference clock[1]		1			1		Out	
Reference clock[2]		1			1		In	
Triggers/markers[1, 3]		1			1		In/out	Reconfigurable
Triggers/markers[2, 3]		8			8		In/out	Reconfigurable
Input channels overview								
Sampling rate		100			100		MSa/s	
Voltage resolution		14			14		Bits	
Input frequency[4]	DC		100	DC		100	MHz	
Real-time BW		50			50		MHz	
Built-in functionalities								
Input conditioning blocks		4			8			1 per channel
Analog trigger processors		4			8			1 per channel
Data acquisition blocks		4			8			1 per channel
Onboard memory								
RAM memory	16		2048	16		2048	MBytes	

1. At front panel
2. At backplane
3. Markers available from firmware version v3.0 or later
4. 100 MHz refer to the Front End bandwidth. This digitizer can operate in 1st and 2nd Nyquist zones (using undersampling technique), but its real-time BW is limited by Nyquist to some 50 MHz. As an example for a band-limited signal of 70 MHz with a 10 MHz signal bandwidth the aliased component will appear between 25 to 35 MHz (30 ± 5 MHz).

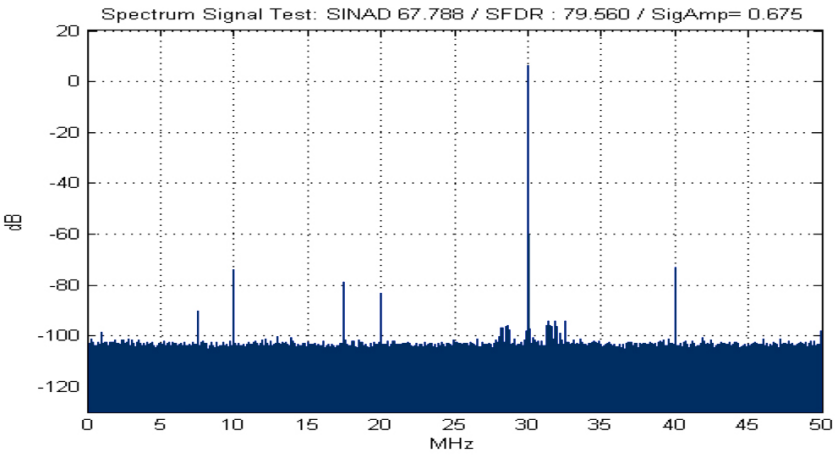
Table 11. General specifications

I/O specifications

Analog input characteristics	
Number of channels	C24 or C48
Sampling rate	100 MSa/s option CLF
Configurable inputs: impedance	50Ω or 1 MΩ (HiZ)
Configurable inputs: Coupling	AC or DC
Input voltage range (50Ω)	400 mVpp to 6Vpp (continue: variable attenuator at input)
Input voltage range (HiZ)	200 mVpp to 20Vpp (continue: variable attenuator at input)
Bandwidth limit filters	100 MHz
Effective number of bits (ENOB)1	10.8 bits @30MHz (typical)
Noise floor	-142 dBm/Hz @30 MHz (typical)
SINAD	67 dB @30 MHz (typical)
Spurious free dynamic range (SFDR) + Total Harmonic Distorsion	79 dBc (typical)

Table 12. Input/output specifications

M3300A



Parameter	M3300A Min	Typ	Max	Units	Comments
Reference clock output					
Frequency		10 or 100		MHz	Generated from the internal clock. User selectable
Voltage		800		mVpp	On a 50 Ω load
Power		2		dBm	On a 50 Ω load
Source impedance		50		Ω	AC coupled
External I/O trigger/marker					
V_{IH}	2		5	V	
V_{IL}	0		0.8	V	
V_{OH}	2.4		3.3	V	On a high Z load
V_{OL}	0		0.5	V	On a high Z load
Input impedance		10		K Ω	
Source impedance		TTL		-	
Speed			500	Mbps	

Table 12b.

Data acquisition blocks (DAQs) specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
DAQs		4			8			1 per channel
Aggregated speed			400			800	MSa/s	For all onboard DAQs combined
Acquisition burst multiple		5			5		Samples	Burst length must be a multiple of this value
Acquisition RAM capacity	15		957M	15		957M	Samples	Maximum depends on onboard RAM
Acquisition RAM capacity effic.		93.5			93.5		%	Effic. = waveform size/waveform size in RAM
Trigger		Selec.			Selec.			Hardware trigger (analog channels, input trigger, backplane triggers), Software trigger
DAQ specifications								
Speed			100			100	MSa/s	Per DAQ
Resolution		14			14		Bits	

Table 13. Data acquisition blocks (DAQs) specifications

Clock system specifications

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
General specifications								
Clock frequency		100			100		MHz	

Table 14. Clock system specifications

System specifications

Environmental specifications (PXI Express)

Parameter	M3300A-C24 Min	M3300A-C24 Typ	M3300A-C24 Max	M3300A-C48 Min	M3300A-C48 Typ	M3300A-C48 Max	Units	Comments
System bus								
Slots		2			2		Slots	PXI Express (CompactPCI Express compatible)
PCI Express type	Gen 1		Gen 2	Gen 1		Gen 2	–	Automatic gen negotiation, chassis dependent
PCI Express link	1		4	1		4	Lanes	Automatic lane negotiation, chassis dependent
PCI Express speed	400		1600	400		1600	MBytes/s	Depends on # of lanes, chassis, congestion, and more
Sustainable throughput	200		800	200		800	MPoints/s	Depends on # of lanes, chassis, congestion, and more
Power dissipation								
3.3 V PXIe power supply		3			3		A	~ 10 W
12 V PXIe power supply		3.5			3.5		A	~ 40 W

Table 15. Environmental specifications (PXI Express)

Environmental		
Temperature range	Operating Non-operating	0 to +55°C (10,000 feet) -40 to +70 °C (up to 15,000 feet)
Max operative altitude		2000 m (10,000 feet)
Operating Humidity range (%RH)		10 to 95% at 40 °C
Non-operating Humidity range (%RH): 5 to 95		5 to 95%
Calibration interval		1 year
EMC		Complies with European EMC Directive – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A This ISM device Compliace with Canadian ICES-001 Cet appareil ISM est conforme à la norme NMB-001 du Canada. This ISM device Compliace with Australian and New Zealand RCM This ISM device Compliace with South Korea EMC KCC

Table 16. Environmental

Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

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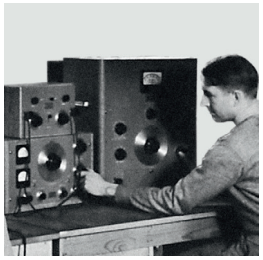

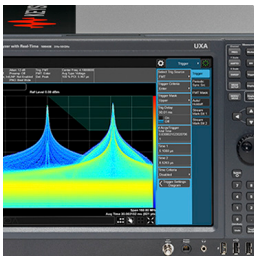

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