TMP102-Q1 采用 SOT563 封装且具有SMBus 和两线制串行接口的低功耗数字温度传感器

1 特性

- 具有符合 AEC-Q100 标准的以下结果：
  - 温度 1 级：-40°C 至 125°C 的环境工作温度范围
  - 人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 组件充电模式 (CDM) ESD 分类等级 C6
- SOT563 封装 (1.6mm × 1.6mm) 尺寸较 SOT23 减小 68%
- 未经校准时的精度：
  - -25°C 到 85°C 时为 2°C（最大值）
  - -40°C 到 125°C 时为 3°C（最大值）
- 低静态电流：
  - 10μA 激活电流（最大值）
  - 1μA 关断电流（最大值）
- 电源范围：1.4V 至 3.6V
- 分辨率：12 位
- 数字输出： SMBus™、两线制和 I^2C 接口兼容性
- 美国国家标准与技术研究所 (NIST) 可追溯

2 应用

- 汽车空调
- 信息娱乐处理器管理
- 空气流量传感器
- 电池控制单元
- 引擎控制单元
- UREA 传感器
- 抽水机
- HID 灯
- 安全气囊控制单元

3 说明

TMP102-Q1 器件是一款数字温度传感器，在要求高精度的应用中是 NTC 和 PTC 热敏电阻的理想替代品。该器件在未经校准或无外部组件信号调节的情况下可提供的精度为 ±0.5°C。器件温度传感器为高度线性化产品，无需复杂计算或查表即可得知温度。片载 12 位模数转换器提供的分辨率低至 0.0625°C。

1.6mm × 1.6mm SOT563 封装尺寸较 SOT23 封装减小 68%。TMP102-Q1 器件 具备 SMBus、两线制和 I^2C 接口兼容性，最多允许四个器件位于同一总线上。此外，该器件还 具备 SMBus 报警功能。器件的额定工作电压范围是 1.4V 至 3.6V，整个工作范围内最大静态电流为 10μA。

TMP102-Q1 器件是各种通信、计算机、消费类产品、环境、工业、和仪器应用中扩展温度测量 的理想选择。器件的额定工作温度范围为 -40°C 至 +125°C。

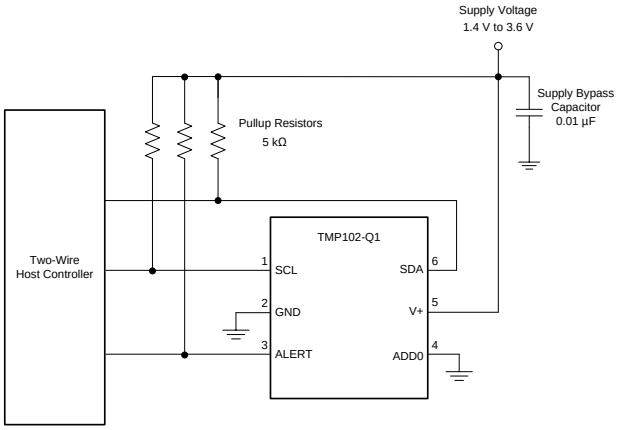
TMP102-Q1 生产单元已完全通过可追溯 NIST 的传感器测试，并且已借助可追溯 NIST 的设备使用 ISO/IEC 17025 标准认可的校准进行验证。

器件信息(1)

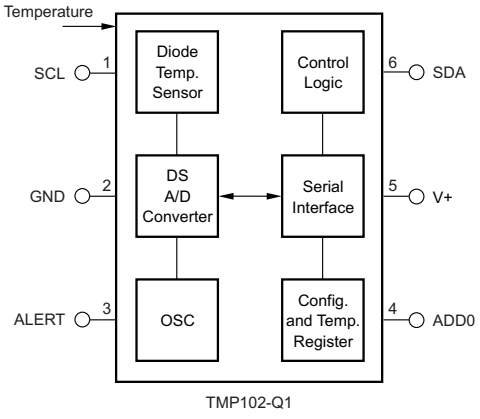
器件型号	封装	封装尺寸（标称值）
TMP102-Q1	SOT563 (6)	1.60mm x 1.20mm

(1) 如需了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化电路原理图



方框图



目录

1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 3
6.1 Absolute Maximum Ratings ... 3
6.2 ESD Ratings ... 3
6.3 Recommended Operating Conditions ... 3
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 4
6.6 Timing Requirements ... 5
6.7 Typical Characteristics ... 6
7 **Detailed Description** ... 7
7.1 Overview ... 7
7.2 Functional Block Diagram ... 7
7.3 Feature Description ... 7
7.4 Device Functional Modes ... 14
7.5 Programming ... 15
8 **Application and Implementation** ... 20
8.1 Application Information ... 20
8.2 Typical Application ... 20
9 **Power Supply Recommendations** ... 22
10 **Layout** ... 22
10.1 Layout Guidelines ... 22
10.2 Layout Example ... 22
11 器件和文档支持 ... 23
11.1 文档支持 ... 23
11.2 社区资源 ... 23
11.3 商标 ... 23
11.4 静电放电警告 ... 23
11.5 Glossary ... 23
12 机械、封装和可订购信息 ... 23

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (March 2015) to Revision C — **Page**

- 已添加 TI 设计 ... 1
- 已添加“美国国家标准与技术研究所 (NIST) 可追溯” 特性 要点 ... 1
- 已在 *说明*部分 ... 1
- 添加了 *社区资源*部分 ... 23

Changes from Revision A (November 2014) to Revision B — **Page**

- 更新了电路原理图上的引脚编号 ... 1
- Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature parameter to the *Absolute Maximum Ratings* table ... 3
- Changed typ, max values for the Accuracy (temperature error) parameter ... 4
- Changed the frequency from 2.85 to 3.4 MHz in the *POWER SUPPLY* section of the *Electrical Characteristics* table ... 4
- Changed the *Temperature Error vs Temperature* graph in the *Typical Characteristics* section ... 6
- Changed the *Temperature Error at 25°C* graph in the *Typical Characteristics* section ... 6

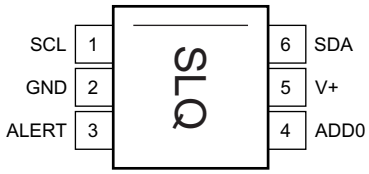
Changes from Original (October 2014) to Revision A — **Page**

- Changed the frequency from 2.8 to 2.85 MHz in the *POWER SUPPLY* section of the *Electrical Characteristics* table ... 4

Copyright © 2014–2015, Texas Instruments Incorporated

5 Pin Configuration and Functions

DRL Package
6-Pin SOT563
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SCL	I	Serial clock. Open-drain output; requires a pullup resistor.
2	GND	—	Ground
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	ADD0	I	Address select. Connect to GND or V+
5	V+	I	Supply voltage, 1.4 V to 3.6 V
6	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
Supply voltage		3.6	V
Input voltage(2)	–0.5	3.6	V
Output voltage		3.6	V
Operating temperature	–55	150	°C
Junction temperature		150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input voltage rating applies to all TMP102-Q1 input voltages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.4	3.3	3.6	V
T_A	Operating free-air temperature	–40		125	°C

Copyright © 2014–2015, Texas Instruments Incorporated

6.4 Thermal Information

THERMAL METRIC(1)		TMP102-Q1 DRL (SOT563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	200	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C and V_S = 1.4 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–40		125	°C
	Accuracy (temperature error)	–25°C to 85°C		±0.5	±2	°C
		–40°C to 125°C		±1	±3	
		Versus supply		0.2	0.5	°C/V
	Resolution			0.0625		°C
DIGITAL INPUT/OUTPUT						
	Input capacitance			3		pF
V_{IH}	Input logic high		0.7 × (V+)		3.6	V
V_{IL}	Input logic low		–0.5		0.3 × (V+)	V
I_I	Input current	0 < V_I < 3.6 V			1	µA
$V_{OL(SDA)}$	Output logic on the SDA pin	V+ > 2 V, I_{OL} = 3 mA	0		0.4	V
		V+ < 2 V, I_{OL} = 3 mA	0		0.2 × (V+)	
$V_{OL(ALERT)}$	Output logic on the ALERT pin	V+ > 2 V, I_{OL} = 3 mA	0		0.4	V
		V+ < 2 V, I_{OL} = 3 mA	0		0.2 × (V+)	
	Resolution			12		Bit
	Conversion time			26	35	ms
	Conversion modes	CR1 = 0, CR0 = 0		0.25		Conv/s
		CR1 = 0, CR0 = 1		1		
		CR1 = 1, CR0 = 0 (default)		4		
		CR1 = 1, CR0 = 1		8		
	Timeout time			30	40	ms
POWER SUPPLY						
	Operating supply range		1.4		3.6	V
I_Q	Average quiescent current	Serial bus inactive, CR1 = 1, CR0 = 0 (default)		7	10	µA
		Serial bus active, SCL frequency (f) = 400 kHz		15		
		Serial bus active, SCL frequency (f) = 3.4 MHz		85		
I_{SD}	Shutdown current	Serial bus inactive		0.5	1	µA
		Serial bus active, SCL frequency (f) = 400 kHz		10		
		Serial bus active, SCL frequency (f) = 3.4 MHz		80		

Copyright © 2014–2015, Texas Instruments Incorporated

6.6 Timing Requirements

see the *Timing Diagrams* section for additional information

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.85	MHz
$t_{(BUF)}$	Bus-free time between STOP and START condition	See *Two-Wire Timing Diagrams*.	600		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	repeated start condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP Condition Setup Time		600		160		ns
$t_{(HDDAT)}$	Data hold time		100	900	25	105	ns
$t_{(SUDAT)}$	Data setup time		100		25		ns
$t_{(LOW)}$	SCL-clock low period	V+ , see *Two-Wire Timing Diagrams*	1300		210		ns
$t_{(HIGH)}$	SCL-clock high period	See *Two-Wire Timing Diagrams*	600		60		ns
t_{FD}	Data fall time	See *Two-Wire Timing Diagrams*		300		80	ns
t_{RD}	Data rise time	See *Two-Wire Timing Diagrams*		300			ns
		SCLK ≤ 100 kHz, see Two-Wire Timing Diagrams		1000			ns
t_{FC}	Clock fall time	See *Two-Wire Timing Diagrams*		300		40	ns
t_{RC}	Clock rise time	See *Two-Wire Timing Diagrams*		300		40	ns

Copyright © 2014–2015, Texas Instruments Incorporated

6.7 Typical Characteristics

at T_A = 25°C and V_{V+} = 3.3 V (unless otherwise noted)

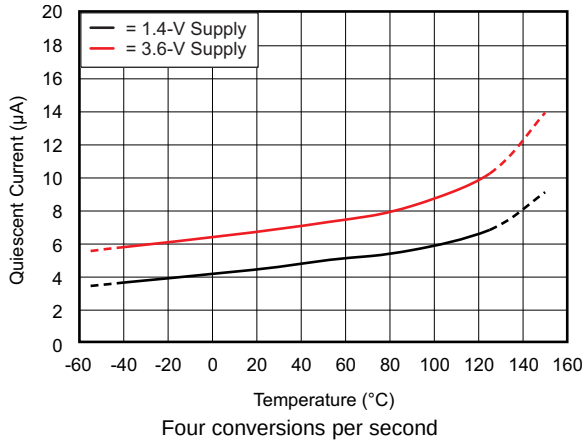


Figure 1. Average Quiescent Current vs Temperature

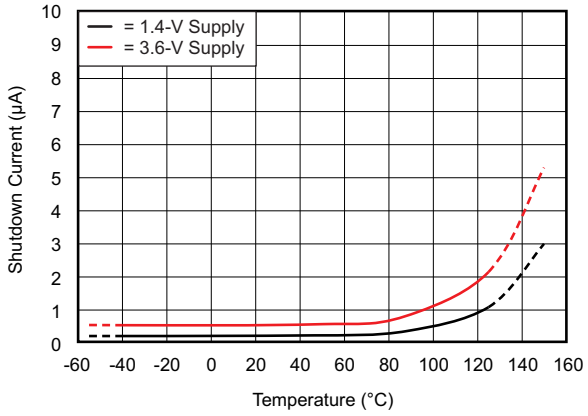


Figure 2. Shutdown Current vs Temperature

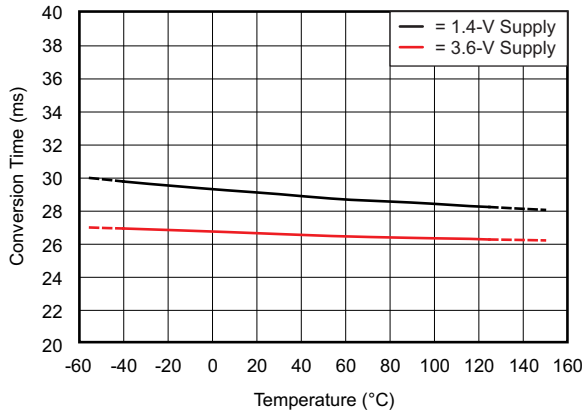


Figure 3. Conversion Time vs Temperature

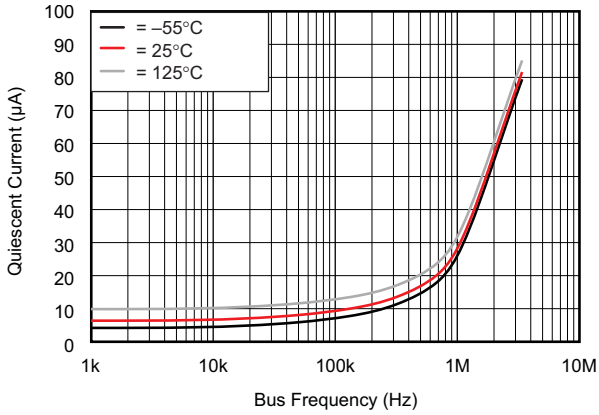


Figure 4. Quiescent Current vs Bus Frequency (Temperature at 3.3-V Supply)

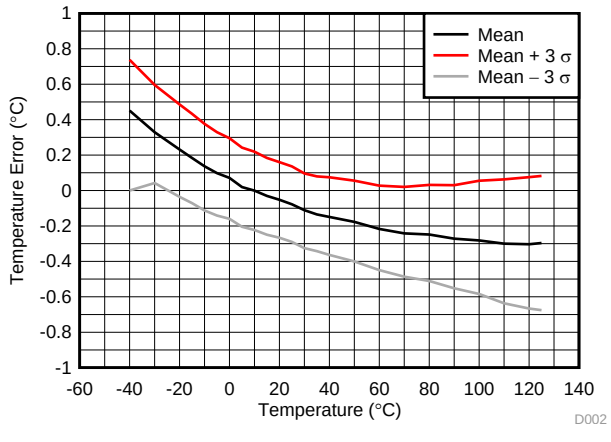


Figure 5. Temperature Error vs Temperature

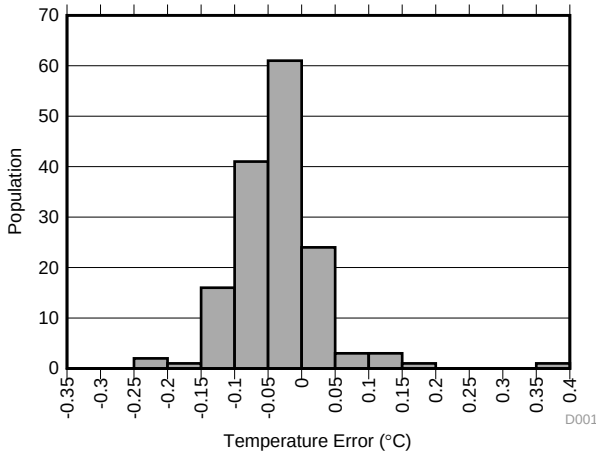


Figure 6. Temperature Error at 25°C

Copyright © 2014–2015, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TMP102-Q1 device is a digital temperature sensor that is optimal for thermal-management and thermal-protection applications. The TMP102-Q1 device is two-wire, SMBus, and I^2C interface-compatible. The device is specified over an operating temperature range of –40°C to 125°C. Figure 7 shows a block diagram of the TMP102-Q1 device.

The temperature sensor in the TMP102-Q1 device is the chip itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

An alternative version of the TMP102-Q1 device is available. The TMP112-Q1 device has highest accuracy, the same micro-package, and is pin-to-pin compatible.

Table 1. Advantages of TMP112-Q1 Versus TMP102-Q1

DEVICE	COMPATIBLE INTERFACES	PACKAGE	SUPPLY CURRENT	SUPPLY VOLTAGE (MIN)	SUPPLY VOLTAGE (MAX)	RESOLUTION	LOCAL SENSOR ACCURACY (MAX)	SPECIFIED CALIBRATION DRIFT SLOPE
TMP112-Q1	I^2C SMBus	SOT563 1.2 × 1.6 × 0.6	10 µA	1.4 V	3.6 V	12 bit 0.0625°C	0.5°C: (0°C to 65°C) 1°C: (-40°C to 125°C)	Yes
TMP102-Q1	I^2C SMBus	SOT563 1.2 × 1.6 × 0.6	10 µA	1.4 V	3.6 V	12 bit 0.0625°C	2°C: (25°C to 85°C) 3°C: (-40°C to 125°C)	No

7.2 Functional Block Diagram

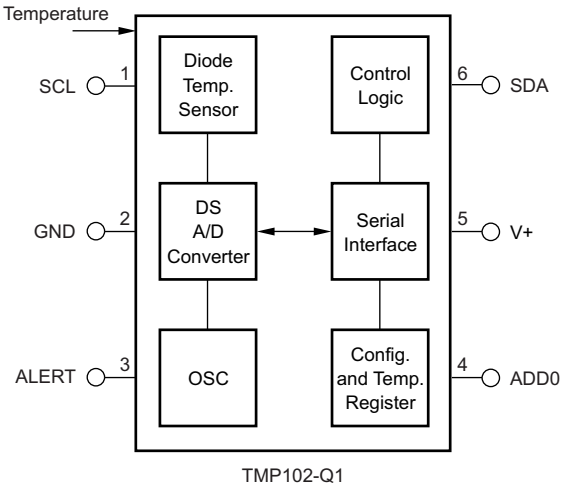


Figure 7. Internal Block Diagram

7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement is stored in the read-only temperature register. The temperature register of the TMP102-Q1 device is configured as a 12-bit, read-only register (configuration register EM bit = 0, see the *Extended Mode (EM)* section), or as a 13-bit, read-only register (configuration register EM bit = 1) that stores the output of the most recent conversion. Two bytes must be read to obtain data and are listed in Table 8 and Table 9. Byte 1 is the most significant byte (MSB), followed by byte 2, the least significant byte (LSB). The first 12 bits (13 bits in extended mode) are used to indicate temperature. The least significant byte does not have to be read if that information is not needed. The data format for temperature is summarized in Table 2 and Table 3. One LSB equals 0.0625°C. Negative numbers are represented in binary twos-complement format. Following power-up or reset, the temperature register reads 0°C until the first conversion is complete. Bit D0 of byte 2 indicates normal mode (EM bit = 0) or extended mode (EM bit = 1) , and can be used to distinguish between the two temperature register data formats. The unused bits in the temperature register always read 0.

Copyright © 2014–2015, Texas Instruments Incorporated

Feature Description (continued)

Table 2. 12-Bit Temperature Data Format(1)

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0111 1111 1111	7FF
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0	0000 0000 0000	000
–0.25	1111 1111 1100	FFC
–25	1110 0111 0000	E70
–55	1100 1001 0000	C90

(1) The resolution for the Temp ADC in Internal Temperature mode is 0.0625°C/count.

Table 2 does not list all temperatures. Use the following rules to obtain the digital data format for a given temperature or the temperature for a given digital data format.

To convert positive temperatures to a digital data format:

1. Divide the temperature by the resolution
2. Convert the result to binary code with a 12-bit, left-justified format, and MSB = 0 to denote a positive sign.

   Example: (50°C) / (0.0625°C / LSB) = 800 = 320h = 0011 0010 0000

To convert a positive digital data format to temperature:

1. Convert the 12-bit, left-justified binary temperature result, with the MSB = 0 to denote a positive sign, to a decimal number.
2. Multiply the decimal number by the resolution to obtain the positive temperature.

   Example: 0011 0010 0000 = 320h = 800 × (0.0625°C / LSB) = 50°C

To convert negative temperatures to a digital data format:

1. Divide the absolute value of the temperature by the resolution, and convert the result to binary code with a 12-bit, left-justified format.
2. Generate the twos complement of the result by complementing the binary number and adding one. Denote a negative number with MSB = 1.

   Example: (|–25°C|) / (0.0625°C / LSB) = 400 = 190h = 0001 1001 0000

   Two's complement format: 1110 0110 1111 + 1 = 1110 0111 0000

To convert a negative digital data format to temperature:

1. Generate the twos compliment of the 12-bit, left-justified binary number of the temperature result (with MSB = 1, denoting negative temperature result) by complementing the binary number and adding one. This represents the binary number of the absolute value of the temperature.
2. Convert to decimal number and multiply by the resolution to get the absolute temperature, then multiply by –1 for the negative sign.

   Example: 1110 0111 0000 has twos compliment of 0001 1001 0000 = 0001 1000 1111 + 1

   Convert to temperature: 0001 1001 0000 = 190h = 400; 400 × (0.0625°C / LSB) = 25°C = (|–25°C|); (|–25°C|) × (–1) = –25°C

Copyright © 2014–2015, Texas Instruments Incorporated

Table 3. 13-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
150	0 1001 0110 0000	0960
128	0 1000 0000 0000	0800
127.9375	0 0111 1111 1111	07FF
100	0 0110 0100 0000	0640
80	0 0101 0000 0000	0500
75	0 0100 1011 0000	04B0
50	0 0011 0010 0000	0320
25	0 0001 1001 0000	0190
0.25	0 0000 0000 0100	0004
0	0 0000 0000 0000	0000
–0.25	1 1111 1111 1100	1FFC
–25	1 1110 0111 0000	1E70
–55	1 1100 1001 0000	1C90

7.3.2 Serial Interface

The TMP102-Q1 device operates as a slave device only on the two-wire bus and SMBus. Connections to the bus are made through the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP102-Q1 device supports the transmission protocol for both fast (1 kHz to 400 kHz) and high-speed (1 kHz to 2.85 MHz) modes. All data bytes are transmitted MSB first.

7.3.3 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are called *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data-line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of the clock, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge and by pulling SDA pin low.

A data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During the data transfer the SDA pin must remain stable when SCL is high, because any change in SDA pin when SCL pin is high is interpreted as a START signal or STOP signal.

When all data have been transferred, the master generates a STOP condition indicated by pulling SDA pin from low to high, when the SCL pin is high.

Copyright © 2014–2015, Texas Instruments Incorporated

7.3.4 Serial Bus Address

To communicate with the TMP102-Q1 device, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation.

The TMP102-Q1 device features an address pin to allow up to four devices to be addressed on a single bus. Table 4 lists the pin-logic levels used to properly connect up to four devices.

Table 4. Address Pin and Slave Addresses

DEVICE TWO-WIRE ADDRESS	A0 PIN CONNECTION
1001000	Ground
1001001	V+
1001010	SDA
1001011	SCL

7.3.5 Writing and Reading Operation

Accessing a particular register on the TMP102-Q1 device is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the TMP102-Q1 device requires a value for the pointer register (see Figure 9).

When reading from the TMP102-Q1 device, the last value stored in the pointer register by a write operation determines which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the pointer register byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 10 for details of this sequence. If repeated reads from the same register are desired, continuously sending the pointer register bytes is not required because the TMP102-Q1 device remembers the pointer register value until the value is changed by the next write operation.

Register bytes are sent with the most significant byte first, followed by the least significant byte.

7.3.6 Slave Mode Operations

The TMP102-Q1 device operates either as a slave receiver or a slave transmitter. As a slave device, the TMP102-Q1 device never drives the SCL line.

7.3.6.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP102-Q1 then acknowledges reception of a valid address. The next byte transmitted by the master is the pointer register. The TMP102-Q1 then acknowledges reception of the pointer register byte. The next byte or bytes are written to the register addressed by the pointer register. The TMP102-Q1 acknowledges reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.3.6.2 Slave Transmitter Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master terminates data transfer by generating a *Not-Acknowledge* on reception of any data byte, or generating a START or STOP condition.

Copyright © 2014–2015, Texas Instruments Incorporated

7.3.7 SMBus Alert Function

The TMP102-Q1 device supports the SMBus alert function. When the TMP102-Q1 device operates in Interrupt Mode (TM = 1), the ALERT pin can be connected as an SMBus alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus alert command (0001 1001) to the bus. If the ALERT pin is active, the device acknowledges the SMBus alert command and responds by returning the slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the ALERT condition was caused by the temperature exceeding T_{HIGH} or falling below T_{LOW}. For POL = 0, the LSB is low if the temperature is greater than or equal to T_{HIGH}; this bit is high if the temperature is less than T_{LOW}. The polarity of this bit is inverted if POL = 1. See Figure 11 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears the ALERT status. The device with the lowest two-wire address wins the arbitration. If the TMP102-Q1 device wins the arbitration, its ALERT pin inactivates at the completion of the SMBus alert command. If the TMP102-Q1 device loses the arbitration, its ALERT pin remains active.

7.3.8 General Call

The TMP102-Q1 device responds to a two-wire general call address (000 0000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 0000 0110, the TMP102-Q1 device internal registers are reset to power-up values. The TMP102-Q1 device does not support the general address acquire command.

7.3.9 High-Speed (Hs) Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-Mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. The TMP102-Q1 device does not acknowledge this byte, but switches the input filters on SDA and SCL and the output filters on SDA to operate in Hs-mode, allowing transfers of up to 2.85 MHz. After the Hs-Mode master code has been issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-Mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP102-Q1 device switches the input and output filters back to fast-mode operation.

7.3.10 Time-Out Function

The TMP102-Q1 device resets the serial interface if SCL is held low for 30 ms (typ) between a start and stop condition. The TMP102-Q1 device releases the SDA line if the SCL pin is pulled low and waits for a start condition from the host controller. To avoid activating the time-out function, maintaining a communication speed of at least 1 kHz for SCL operating frequency is necessary.

7.3.11 Timing Diagrams

The TMP102-Q1 device is two-wire, SMBus, and I^2C-interface compatible. Figure 8, Figure 9, Figure 10, and Figure 11 list the various operations on the TMP102-Q1 device. Parameters for Figure 8 are defined in the *Timing Requirements* table. The bus definitions are defined as follows:

Bus Idle Both SDA and SCL lines remain high.

Start Data Transfer A change in the state of the SDA line, from high to low, when the SCL line is high, defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The TMP102-Q1 device can also be used for single byte updates. To update only the MS byte, terminate the communication by issuing a START or STOP communication on the bus.

Copyright © 2014–2015, Texas Instruments Incorporated

Acknowledge Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a *not-acknowledge* (1) on the last byte that has been transmitted by the slave.

7.3.12 Two-Wire Timing Diagrams

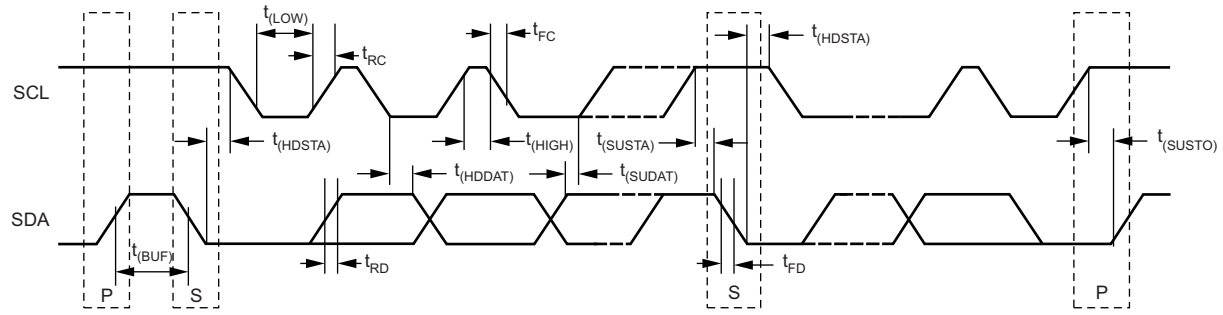
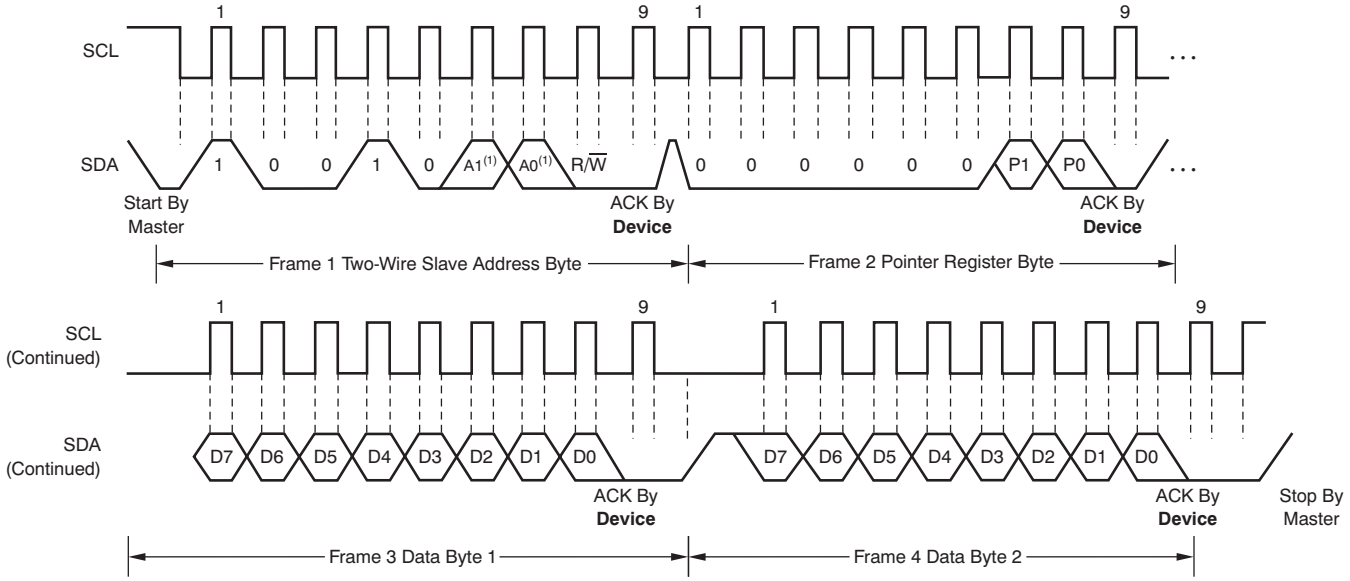


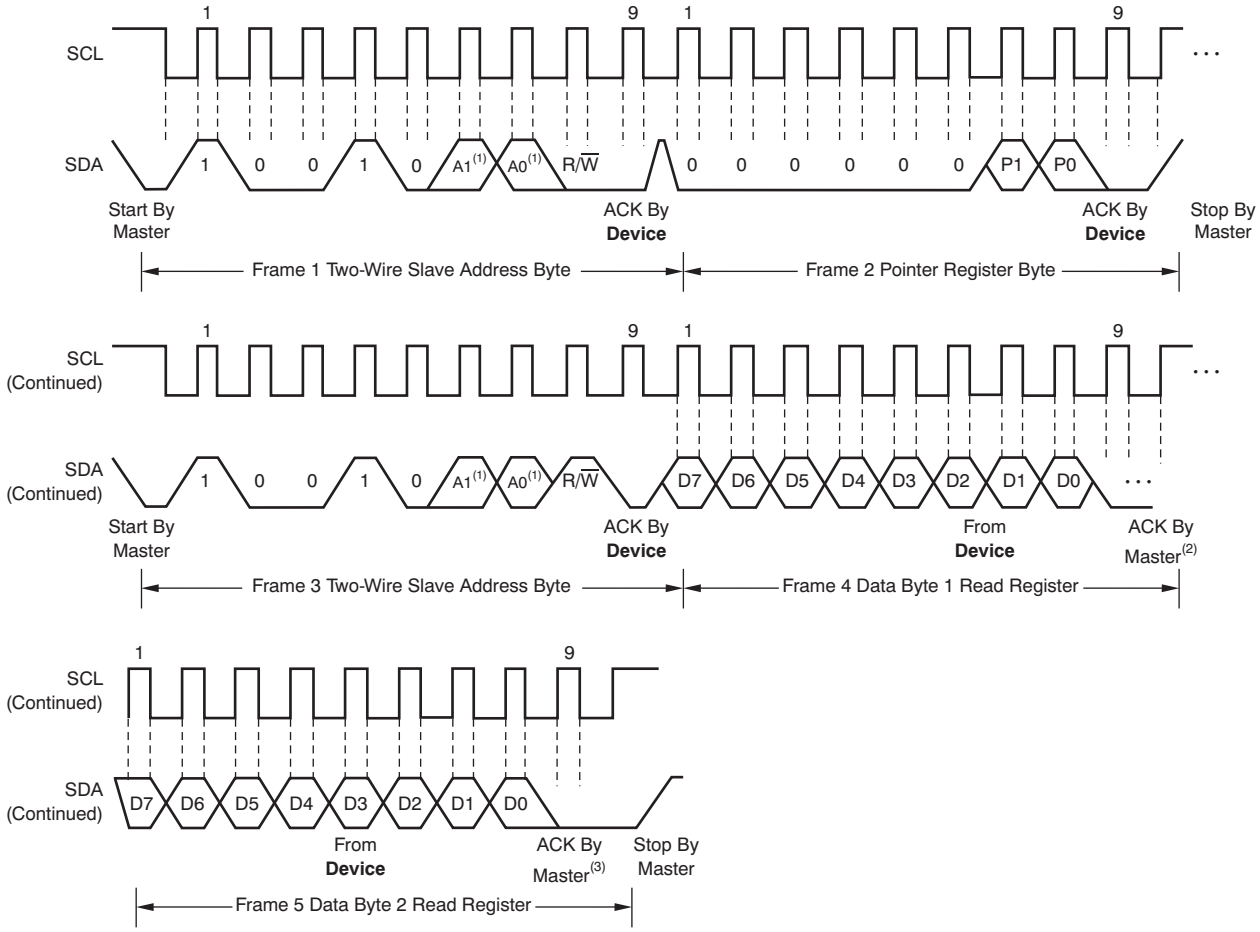
Figure 8. Two-Wire Timing Diagram



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.

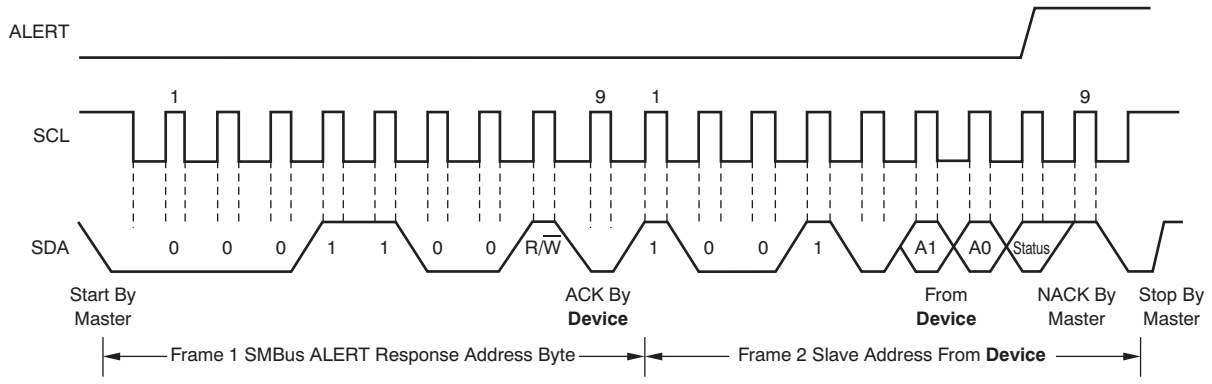
Figure 9. Two-Wire Timing Diagram for Write Word Format

Copyright © 2014–2015, Texas Instruments Incorporated



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.
(2) Master should leave SDA high to terminate a single-byte read operation.
(3) Master should leave SDA high to terminate a two-byte read operation.

Figure 10. Two-Wire Timing Diagram for Read Word Format



NOTE: (1) The value of A0 and A1 are determined by the ADD0 pin.

Figure 11. Timing Diagram for SMBus ALERT

7.4 Device Functional Modes

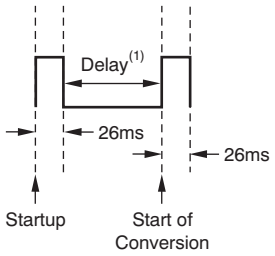
7.4.1 Continuos-Conversion Mode

The default mode of the TMP102-Q1 device is continuos conversion mode. During continuos-conversion mode, the ADC performs continuos temperature conversions and stores each results to the temperature register, overwriting the result from the previous conversion. The conversion rate bits, CR1 and CR0, configure the TMP102-Q1 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. The TMP102-Q1 device has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP102-Q1 device makes a conversion and then powers down to wait for the appropriate delay set by CR1 and CR0. Table 5 lists the settings for CR1 and CR0.

Table 5. Conversion Rate Settings

CR1	CR0	CONVERSION RATE
0	0	0.25 Hz
0	1	1 Hz
1	0	4 Hz (default)
1	1	8 Hz

After power-up or general-call reset, the TMP102-Q1 device immediately begins a conversion as shown in Figure 12. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 µA (typical at 27°C). The quiescent current during delay is 2.2 µA (typical at 27°C).



(1) The delay is set by CR1 and CR0 bits in the configuration register.

Figure 12. Conversion Start

7.4.2 Extended Mode (EM)

The Extended-Mode bit configures the device for Normal Mode operation (EM = 0) or Extended Mode operation (EM = 1). In normal mode, the temperature register, high-limit register, and low-limit register use a 12-bit data format. Normal Mode is used to make the TMP102-Q1 device compatible with the TMP75 device.

Extended mode (EM = 1) allows measurement of temperatures above 128°C by configuring the temperature register, high-limit register, and low-limit register for 13-bit data format.

7.4.3 Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 µA. Shutdown mode enables when the SD bit is 1; the device shuts down when current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.4.4 One-Shot and Conversion Ready (OS)

The TMP102-Q1 device features a one-shot temperature measurement mode. When the device is in Shutdown Mode, writing a 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, the OS bit reads 1. This feature reduces power consumption in the TMP102-Q1 device when continuous temperature monitoring is not required.

Copyright © 2014–2015, Texas Instruments Incorporated

As a result of the short conversion time, the TMP102-Q1 device achieves a higher conversion rate. A single conversion typically takes 26 ms and a read can take place in less than 20 µs. When using One-Shot Mode, 30 or more conversions per second are possible.

7.4.5 Thermostat Mode (TM)

The thermostat-mode bit indicates to the device whether to operate in comparator mode (TM = 0) or Interrupt mode (TM = 1).

7.4.5.1 Comparator Mode (TM = 0)

In Comparator mode (TM = 0), the Alert pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$register. For more information on the comparator mode, see the *High-Limit and Low-Limit Registers* section.

7.4.5.2 Interrupt Mode (TM = 1)

In Interrupt mode (TM = 1), the Alert pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The Alert pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High-Limit and Low-Limit Registers* section.

7.5 Programming

7.5.1 Pointer Register

Figure 13 shows the internal register structure of the TMP102-Q1 device. The 8-bit pointer register of the device is used to address a given data register. The pointer register uses the two least-significant bytes (LSBs) (see Table 13) to identify which of the data registers must respond to a read or write command. The power-up reset value of P1 and P0 is 00. By default, the TMP102-Q1 device reads the temperature on power up.

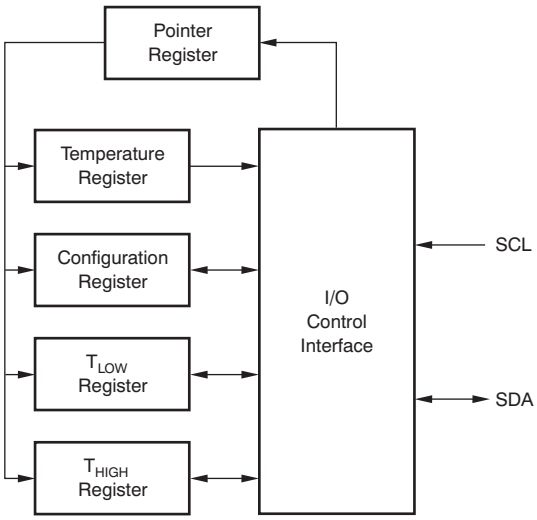


Figure 13. Internal Register Structure

Programming (continued)

Table 6 lists the pointer address of the registers available in the TMP102-Q1 device. Table 7 lists the bits of the pointer register byte. During a write command, P2 through P7 must always be 0.

Table 6. Pointer Addresses

P1	P0	REGISTER
0	0	Temperature register (read only)
0	1	Configuration register (read and write)
1	0	T_{LOW} register (read and write)
1	1	T_{HIGH} register (read and write)

Table 7. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register bits	

7.5.2 Temperature Register

The temperature register of the TMP102-Q1 device is configured as a 12-bit, read-only register (configuration register EM bit = 0, see the *Extended Mode (EM)* section), or as a 13-bit, read-only register (configuration register EM bit = 1) that stores the output of the most recent conversion. To obtain data as described in Table 8 and Table 9 read two bytes. Note that byte 1 is the most-significant byte (MSB), followed by byte 2, the least-significant byte. The first 12 bits (13 bits in extended mode) indicate temperature. The LSB does not must be read if that information is not needed.

Table 8. Byte 1 of Temperature Register(1)

D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4
(T12)	(T11)	(T10)	(T9)	(T8)	(T7)	(T6)	(T5)

(1) The 13-bit Extended-Mode configuration is shown in parentheses.

Table 9. Byte 2 of Temperature Register(1)

D7	D6	D5	D4	D3	D2	D1	D0
T3	T2	T1	T0	0	0	0	0
(T4)	(T3)	(T2)	(T1)	(T0)	(0)	(0)	(1)

(1) The 13-bit Extended-Mode configuration is shown in parenthesis.

7.5.3 Configuration Register

The configuration register is a 16-bit read-write register that stores bits which control the operational modes of the temperature sensor. Read and write operations are performed on the MSB first. Table 10 lists the format and the power-up or reset value of the configuration register. For compatibility, the first byte corresponds to the configuration register in the TMP75 device and TMP275 device (for more information see the device data sheets, SBOS288 and SBOS363, respectively). All registers are updated byte by byte.

Table 10. Configuration and Power-Up or Reset Format

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	OS	R1	R0	F1	F0	POL	TM	SD
	0	1	1	0	0	0	0	0
2	CR1	CR0	AL	EM	0	0	0	0
	1	0	1	0	0	0	0	0

Copyright © 2014–2015, Texas Instruments Incorporated

7.5.3.1 Shutdown Mode (SD)

The Shutdown-mode bit saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 µA. Shutdown mode enables when the SD bit is 1; the device shuts down when current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.5.3.2 Thermostat Mode (TM)

The thermostat-mode bit indicates to the device whether to operate in comparator mode (TM = 0) or Interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High-Limit and Low-Limit Registers* section.

7.5.3.3 Polarity (POL)

The polarity bit allows the user to adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low . When the POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is shown in Figure 14

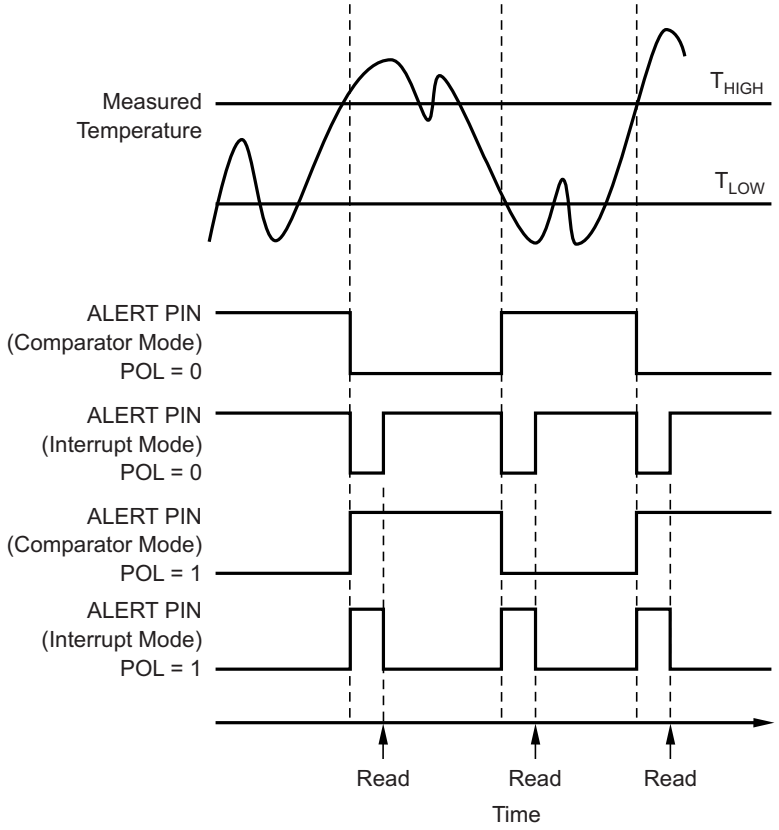


Figure 14. Output Transfer Function Diagrams

Copyright © 2014–2015, Texas Instruments Incorporated

7.5.3.4 Fault Queue (F1 and F0)

A fault condition exists when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert is programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 11 lists the number of measured faults that can be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High-Limit and Low-Limit Registers* section.

Table 11. TMP102-Q1 Fault Settings

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

7.5.3.5 Converter Resolution (R1 and R0)

The converter resolution bits, R1 and R0, are read-only bits. The TMP102-Q1 converter resolution is set at device start-up to 11 which sets the temperature register to a 12 bit-resolution.

7.5.3.6 One-Shot (OS)

When the device is in Shutdown Mode, writing a 1 to the OS bit starts a single temperature conversion. During the conversion, the OS bit reads '0'. The device returns to the shutdown state at the completion of the single conversion. For more information on the one-shot conversion mode, see the *One-Shot and Conversion Ready (OS)* section.

7.5.3.7 Extended Mode (EM)

The Extended-Mode bit configures the device for Normal Mode operation (EM = 0) or Extended Mode operation (EM = 1). In normal mode, the temperature register, high-limit register, and low-limit register use a 12-bit data format. For more information on the extended mode, see the *Extended Mode (EM)* section.

7.5.3.8 Alert (AL Bit)

The AL bit is a read-only function. Reading the AL bit provides information about the comparator mode status. The state of the POL bit inverts the polarity of data returned from the AL bit. When the POL bit equals 0, the AL bit reads as 1 until the temperature equals or exceeds $T_{(HIGH)}$ for the programmed number of consecutive faults, causing the AL bit to read as 0. The AL bit continues to read as 0 until the temperature falls below $T_{(LOW)}$ for the programmed number of consecutive faults, when it again reads as 1. The status of the TM bit does not affect the status of the AL bit.

7.5.3.9 Conversion Rate (CR)

The conversion rate bits, CR1 and CR0, configure the TMP102-Q1 device for conversion rates of 0.25 Hz, 1 Hz, 4 Hz, or 8 Hz. The default rate is 4 Hz. For more information on the conversion rate bits, see the *Continuos-Conversion Mode* section.

7.5.4 High-Limit and Low-Limit Registers

The temperature limits are stored in the $T_{(LOW)}$ and $T_{(HIGH)}$ registers in the same format as the temperature result, and their values are compared to the temperature result on every conversion. The outcome of the comparison drives the behavior of the ALERT pin, which operates as a comparator output or an interrupt, and is set by the TM bit in the configuration register.

In Comparator mode (TM = 0), the ALERT pin is active when the temperature equals or exceeds the value in T_{HIGH} and generates a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

Copyright © 2014–2015, Texas Instruments Incorporated

In Interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of fault conditions as shown in Table 11. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus alert response address. The ALERT pin is cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it becomes active again only when temperature falls below T_{LOW}. The pin remains active until cleared by a read operation of any register or a successful response to the SMBus alert response address. When the ALERT pin is cleared, the above cycle repeats, and the ALERT pin goes active when the temperature equals or exceeds T_{HIGH}. The ALERT pin is also cleared by resetting the device with the general call reset command. This action also clears the state of the internal registers in the device, returning the device to comparator mode (TM = 0).

Both operational modes are shown in Figure 14. Table 12 and Table 13 list the format for the T_{HIGH} and T_{LOW} registers. Note that the most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and T_{LOW} are: T_{HIGH} = 80°C and T_{LOW} = 75°C. The format of the data for T_{HIGH} and T_{LOW} is the same as for the temperature register.

Table 12. Bytes 1 and 2 of T_{HIGH} Register(1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	H11	H10	H9	H8	H7	H6	H5	H4
	(H12)	(H11)	(H10)	(H9)	(H8)	(H7)	(H6)	(H5)
2	H3	H2	H1	H0	0	0	0	0
	(H4)	(H3)	(H2)	(H1)	(H0)	(0)	(0)	(0)

(1) The 13-bit Extended-Mode configuration is shown in parenthesis.

Table 13. Bytes 1 and 2 of T_{LOW} Register(1)

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
1	L11	L10	L9	L8	L7	L6	L5	L4
	(L12)	(L11)	(L10)	(L9)	(L8)	(L7)	(L6)	(L5)
2	L3	L2	L1	L0	0	0	0	0
	(L4)	(L3)	(L2)	(L1)	(L0)	(0)	(0)	(0)

(1) The 13-bit Extended-Mode configuration is shown in parenthesis.

Copyright © 2014–2015, Texas Instruments Incorporated

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP102-Q1 device is used to measure the PCB temperature of the board location where the device is mounted. The programmable address options allow up to four locations on the board to be monitored on a single serial bus.

8.2 Typical Application

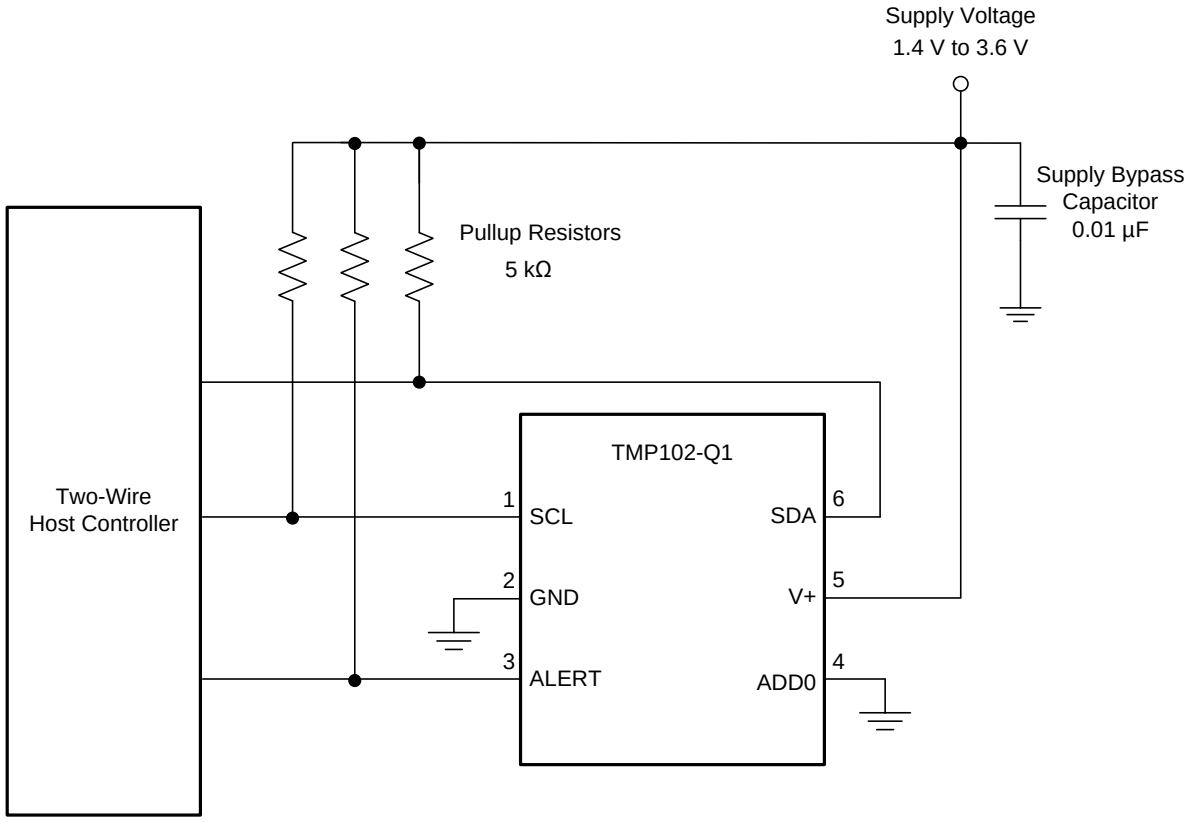


Figure 15. Typical Connections

8.2.1 Design Requirements

The TMP102-Q1 device requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistors is 5-kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ but must not exceed 3 mA of current on any of those pins. A 0.01-µF bypass capacitor on the supply is recommended as shown in Figure 15. The SCL and SDA lines can be pulled up to a supply that is equal to or higher than V+ through the pullup resistors. To configure one of four different addresses on the bus, connect the ADD0 pin to either the GND, V+, SDA, or SCL pin.

Copyright © 2014–2015, Texas Instruments Incorporated

Typical Application (continued)

8.2.2 Detailed Design Procedure

Place the TMP102-Q1 device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, care must be taken to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

The TMP102-Q1 device is a very low-power device and generates very low noise on the supply bus. Applying an RC filter to the V+ pin of the TMP102-Q1 device can further reduce any noise that the TMP102-Q1 device might propagate to other components. $R_{(F)}$ in Figure 16 must be less than 5 kΩ and $C_{(F)}$ must be greater than 10 nF.

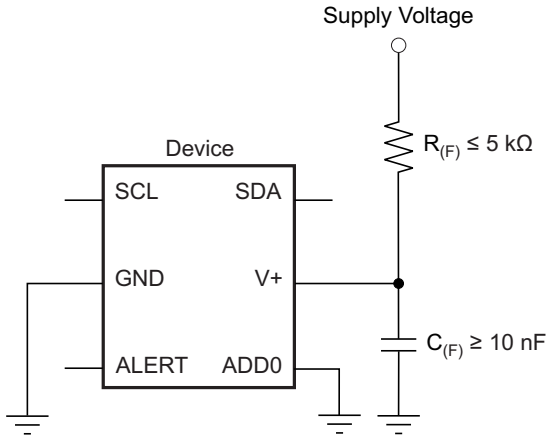


Figure 16. Noise Reduction Techniques

8.2.3 Application Curve

Figure 17 shows the step response of the TMP102-Q1 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 0.8 s. The time-constant result depends on the printed circuit board (PCB) that the TMP102-Q1 device is mounted. For this test, the TMP102-Q1 device was soldered to a two-layer PCB that measured 0.375 in × 0.437 in.

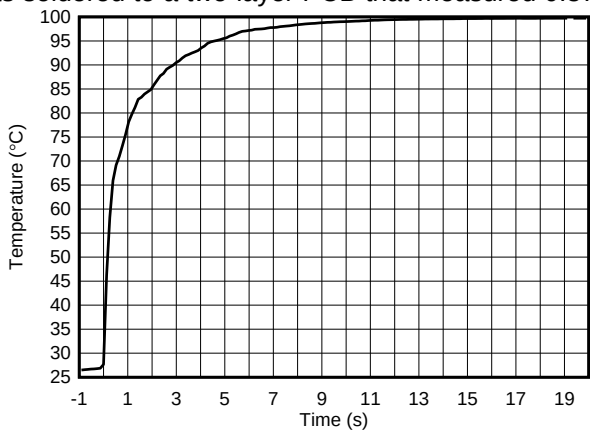


Figure 17. Temperature Step Response

Copyright © 2014–2015, Texas Instruments Incorporated

9 Power Supply Recommendations

The TMP102-Q1 device operates with power supply in the range of 1.4 to 3.6 V. The device is optimized for operation at 3.3-V supply but can measure temperature accurately in the full supply range.

A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins (SDA , SCL and ALERT) through 5-kΩ pullup resistors.

10.2 Layout Example

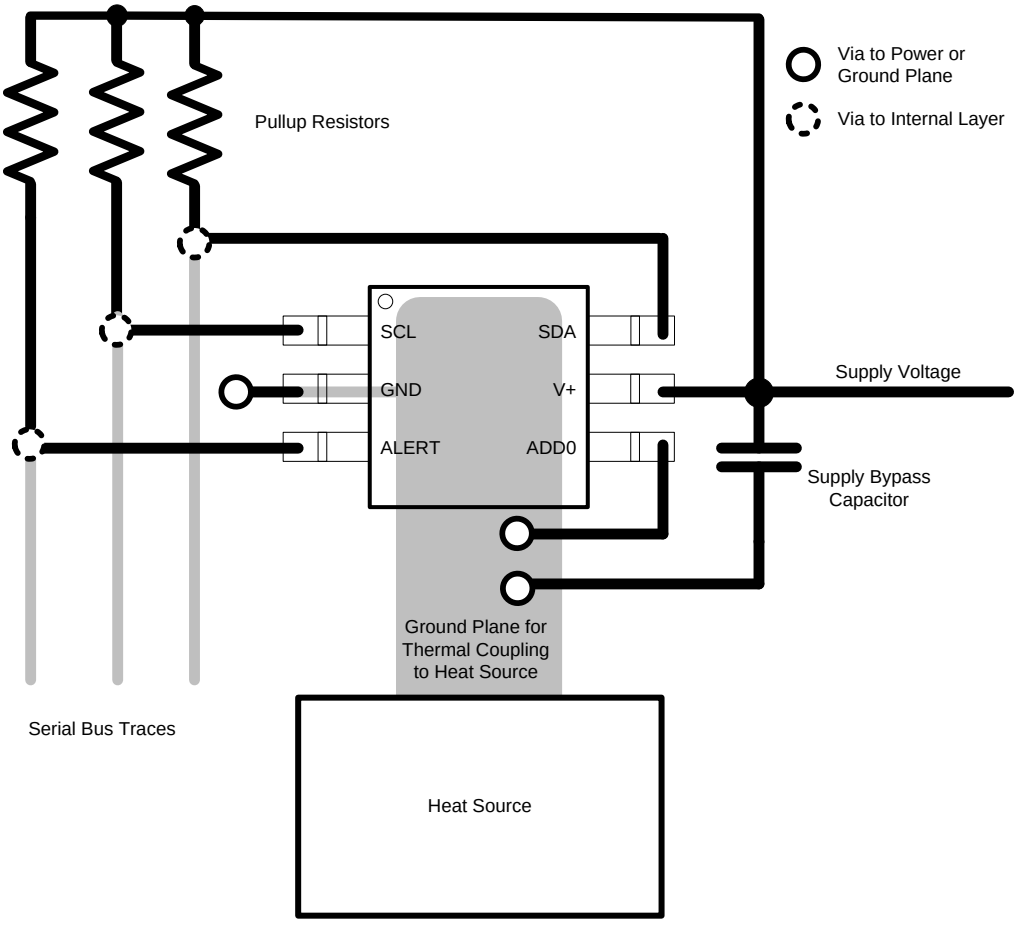


Figure 18. TMP102-Q1 Layout Example

版权 © 2014–2015, Texas Instruments Incorporated

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- 《TMP75 *具有双线接口的数字温度传感器*》，SBOS288
- 《TMP102 *采用 SOT563 封装且具有 SMBus™/两线制串行接口的低功耗数字温度传感器*》，SBOS397
  或查看 TMP102 产品文件夹，网址为 http://www.ti.com.cn/product/cn/TMP102。
- 《TMP275 *0.5°C 精度数字输出温度传感器*》，SBOS363

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
SMBus is a trademark of Intel, Inc.
All other trademarks are the property of their respective owners.

11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122
Copyright © 2016, 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP102AQDRLRQ1	ACTIVE	SOT-5X3	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SLQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMP102-Q1 :

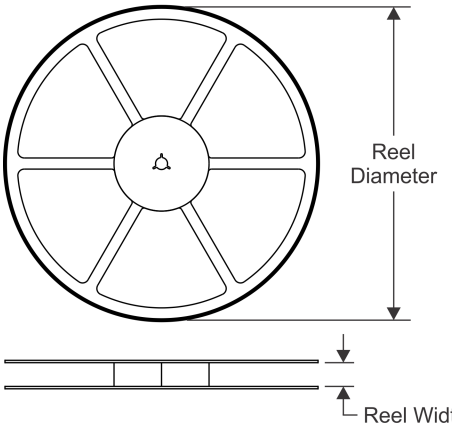
- Catalog: TMP102

NOTE: Qualified Version Definitions:

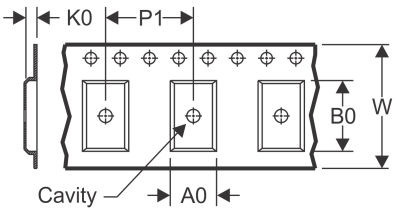
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

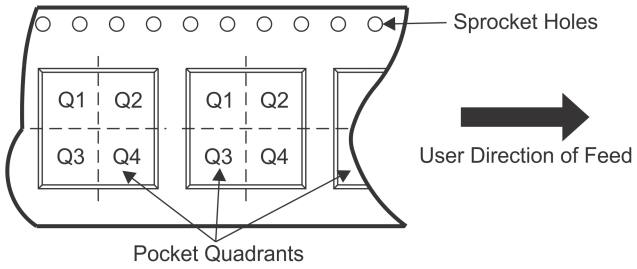


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

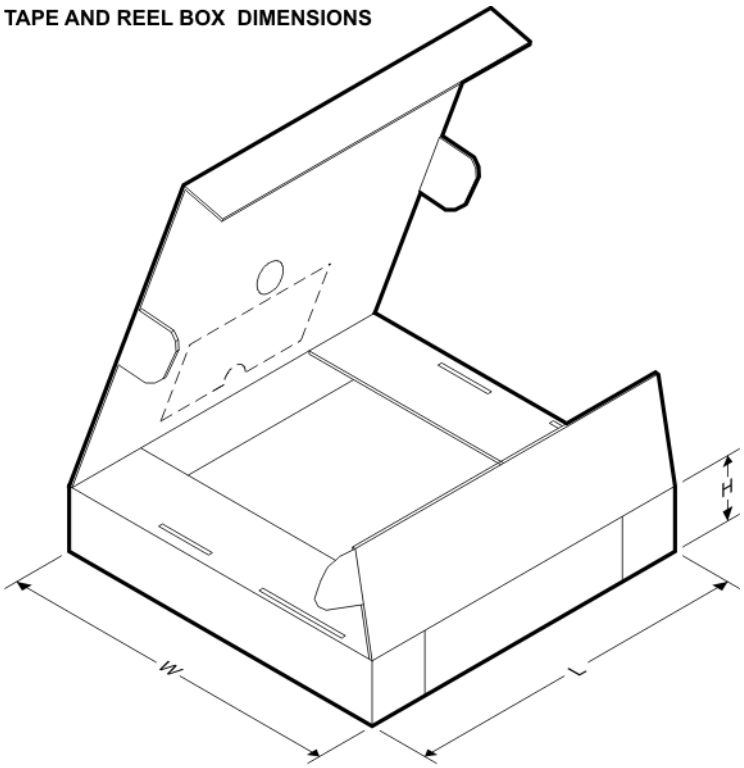
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

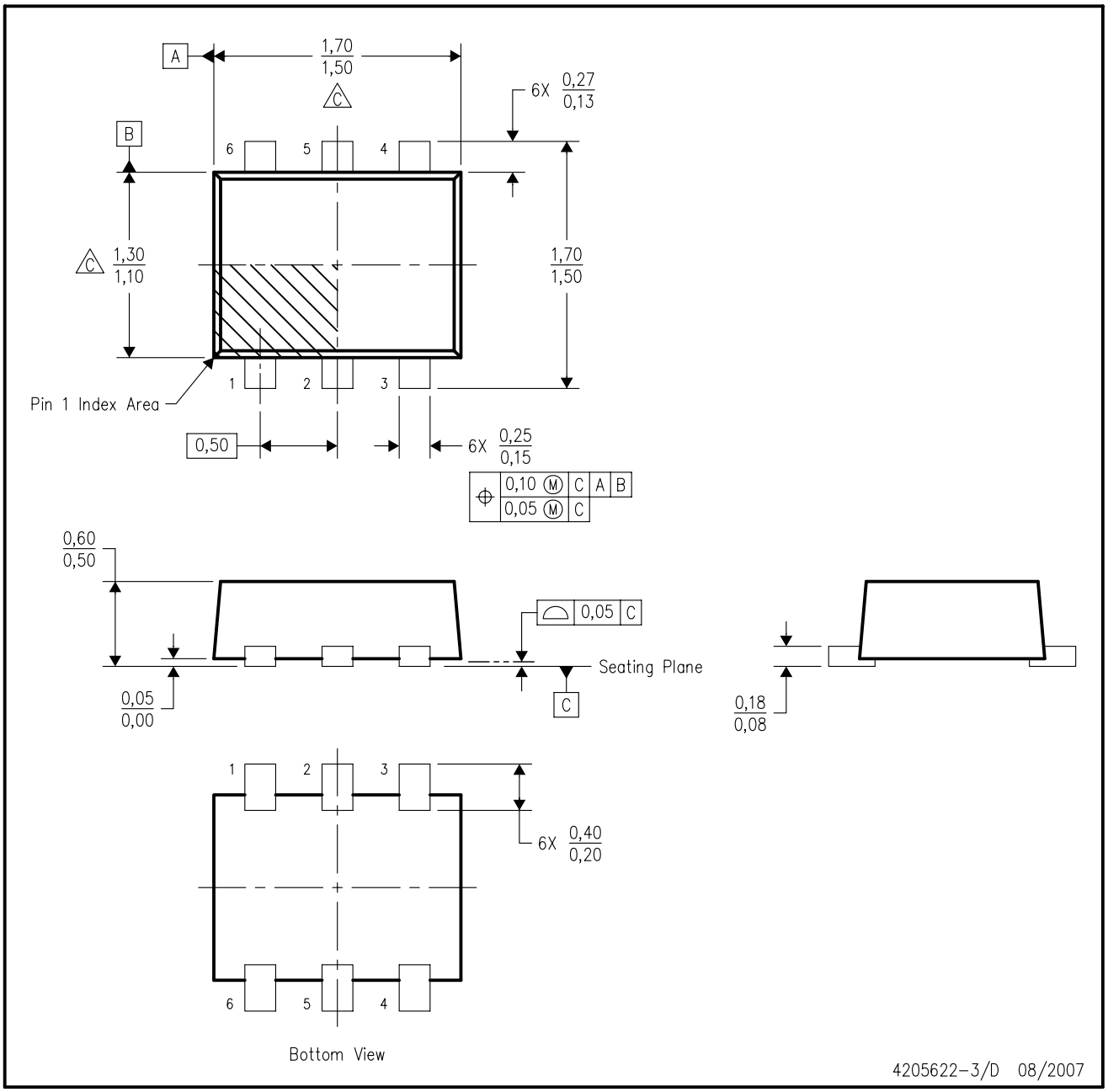
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP102AQDRLRQ1	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP102AQDRLRQ1	SOT-5X3	DRL	6	4000	223.0	270.0	35.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2017 德州仪器半导体技术（上海）有限公司