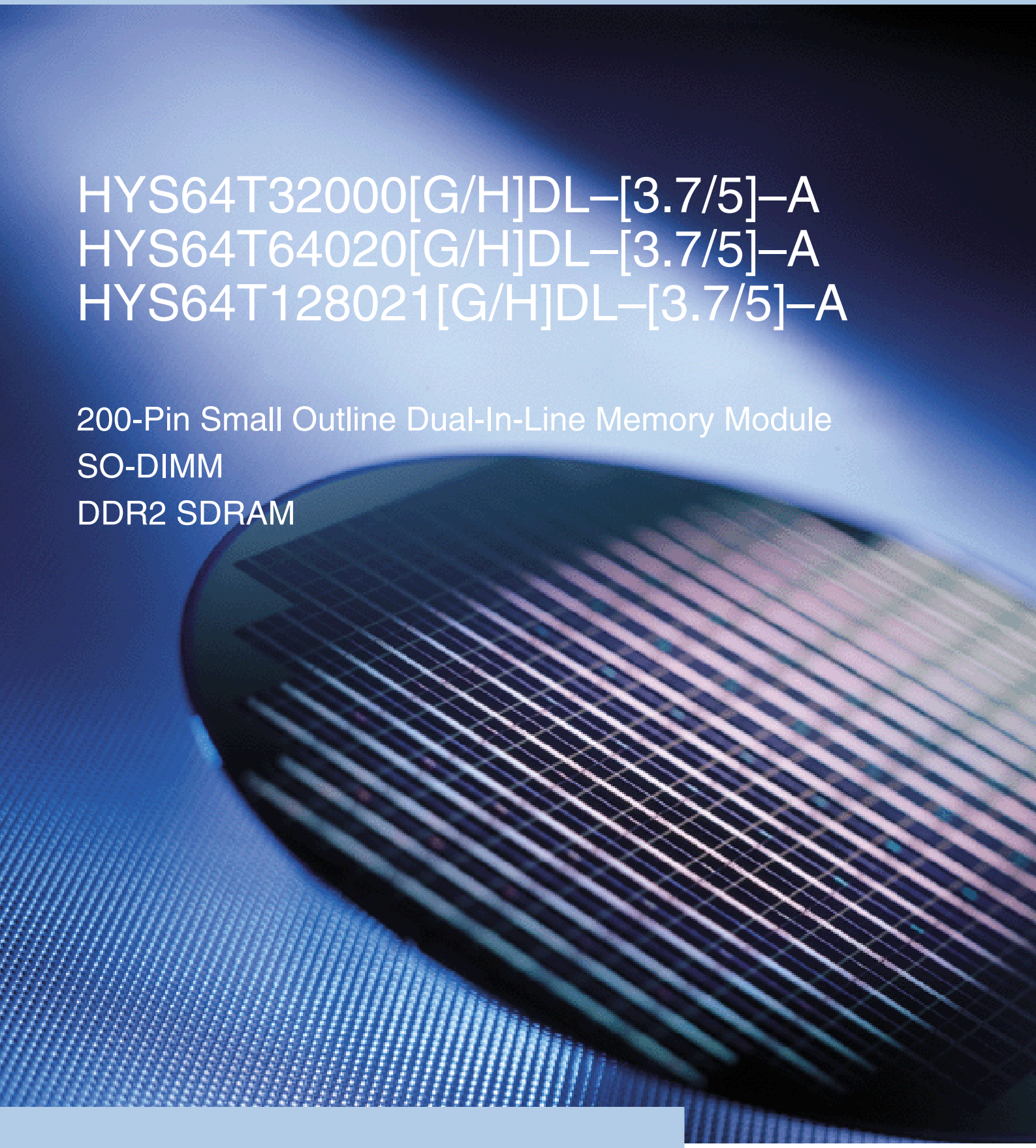
HYS64T32000[G/H]DL–[3.7/5]–A
HYS64T64020[G/H]DL–[3.7/5]–A
HYS64T128021[G/H]DL–[3.7/5]–A

200-Pin Small Outline Dual-In-Line Memory Module

SO-DIMM

DDR2 SDRAM



Memory Products

Infineon technologies

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200-Pin Small Outline Dual-In-Line Memory Module

SO-DIMM

DDR2 SDRAM

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HYS64T[32000/64020/128021][G/H]DL–[3.7/5]–A

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Page	Subjects (major changes since last revision)
all	editorial changes
all	removed HYS64T128022HDL products and all -3 products
all	added HYS64T128021[G/]DL products

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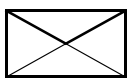

Table of Contents

1	**Overview**	6
1.1	Features	6
1.2	Description	6
1.3	Pin Configuration	8
2	**Block Diagrams**	15
3	**Electrical Characteristics**	18
4	**I_{DD} Specifications and Conditions**	19
4.1	I_{DD} Test Conditions	22
4.2	ODT (On Die Termination) Current	22
5	**Electrical Characteristics & AC Timings**	23
6	**SPD Codes**	26
7	**Package Outlines**	44
8	**Product Type Nomenclature (DDR2 DRAMs and DIMMs)**	47

1 Overview

This chapter gives an overview of the 1.8 V 200-Pin Small Outline Dual-In-Line Memory Module, 256 MByte and 512 MByte and describes its main characteristics.

1.1 Features

- 200-pin Non-ECC Unbuffered 8-Byte Dual-In-Line DDR2 SDRAM Module for Notebooks and other application where small form factors are required.
- One rank 32M × 64, two ranks 64M × 64 and 128M × 64 module organisation and 32M × 16 and 64M × 8 chip organisation
- JEDEC standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- 256 ,512 MByte and 1GByte modules built with 512Mb DDR2 SDRAMs in 60-ball FBGA (P–TFBGA–60) and 84-ball FBGA (P–TFBGA–84) chipsize packages
- Programmable CAS Latencies (3, 4 and 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs SSTL_1.8 compatible
- Off-Chip Driver Impedance Adjustment(OCD) and On-Die Termination(ODT)
- Serial Presence Detect with E^2PROM
- Low Profile Modules form factor: 67.60 mm x 30.00 mm (MO-224)
- Based on JEDEC standard reference layouts Raw Card “A”, “C” and “D”

Table 1 Performance

Product Type Speed Code			–3.7	–5	Units
Speed Grade			PC2–4200 4–4–4	PC2–3200 3–3–3	—
max. Clock Frequency	@CL5	f_{CK5}	266	200	MHz
	@CL4	f_{CK4}	266	200	MHz
	@CL3	f_{CK3}	200	200	MHz
min. RAS-CAS-Delay		t_{RCD}	15	15	ns
min. Row Precharge Time		t_{RP}	15	15	ns
min. Row Active Time		t_{RAS}	45	40	ns
min. Row Cycle Time		t_{RC}	60	55	ns

1.2 Description

The INFINEON HYS64T[32000/64020/128021][G/H]DL–[3.7/5]–A module family are low profile SO-DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as Non-ECC modules in 32M × 64 (256 MByte),64M × 64 (512 MByte) and 128M × 64 (1 GByte) organisation and density, intended for mounting into 200-pin connector sockets.

The memory array is designed with 512Mb Double-Data-Rate-Two (DDR2) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E^2PROM device using the 2-pin I^2C protocol. The first 128 bytes are programmed with configuration data and are write protected; the second 128 bytes are available to the customer.

Table 2 Ordering Information

Product Type	Compliance Code	Description	SDRAM Technology
HYS64T32000GDL–3.7–A	PC2–4200S–444–10–C0	one rank 256 MByte SO–DIMM	512 Mbit (×16)
HYS64T64020GDL–3.7–A	PC2–4200S–444–10–A0	two ranks 512 MByte SO–DIMM	512 Mbit (×16)
HYS64T128021GDL–3.7–A	PC2–4200S–444–10–D0	two ranks 1 GByte SO–DIMM	512 Mbit (× 8)
HYS64T32000GDL–5–A	PC2–3200S–333–10–C0	one rank 256 MByte SO–DIMM	512 Mbit (×16)
HYS64T64020GDL–5–A	PC2–3200S–333–10–A0	two ranks 512 MByte SO–DIMM	512 Mbit (×16)
HYS64T128021GDL–5–A	PC2–3200S–333–10–D0	two ranks 1 GByte SO–DIMM	512 Mbit (× 8)
		green Product	
HYS64T32000HDL–3.7–A	PC2–4200S–444–10–C0	one rank 256 MByte SO–DIMM	512 Mbit (×16)
HYS64T64020HDL–3.7–A	PC2–4200S–444–10–A0	two ranks 512 MByte SO–DIMM	512 Mbit (×16)
HYS64T128021HDL–3.7–A	PC2–4200S–444–10–D0	two ranks 1 GByte SO–DIMM	512 Mbit (× 8)
HYS64T32000HDL–5–A	PC2–3200S–333–10–C0	one rank 256 MByte SO–DIMM	512 Mbit (×16)
HYS64T64020HDL–5–A	PC2–3200S–333–10–A0	two ranks 512 MByte SO–DIMM	512 Mbit (×16)
HYS64T128021HDL–5–A	PC2–3200S–333–10–D0	two ranks 1 GByte SO–DIMM	512 Mbit (× 8)

Note: The Compliance Code is printed on the module label and describes the speed grade,e.g. "512MB 2R×16 PC2–3200S–33310–A" where "512MB" tells the density in megabytes, "2Rx16" means 2 ranks on module built of ×16 components, "PC2–3200S" means DDR2 SO-DIMM with 4.26 GB/s module bandwidth and "444-11" means CAS latency of 4, RCD[1] latency of 4, and RP[2] latency of 4 using Jedec SPD revision 1.0. All part numbers end with a place code, designating the silicon die revision. Example: HYS64T32000GDL–3.7–A, indicating Rev. A dice are used for DDR2 SDRAM components. For all INFINEON DDR2 module and component nomenclature see ***Chapter 8*** *of this datasheet.*

Table 3 Address Format

DIMM Density	Module Organization	Memory Ranks	# of SDRAMs	# of row/bank/column bits	Raw Card
256 MB	32M ×64	1	4	13/2/10	C
512 MB	64M ×64	2	8	13/2/10	A
1 GB	128M ×64	2	16	14/2/10	D

1) RCD: Row Column Delay

2) RP: Row Precharge

Table 4 Components on Modules[1)]

Product Type	DRAM Components	DRAM Density	DRAM Organisation
HYS64T32000GDL	HYB18T512160AC	512 Mbit	32M ×16
HYS64T64020GDL			
HYS64T32000HDL[2)]	HYB18T512160AF[2)]	512 Mbit	32M ×16
HYS64T64020HDL[2)]			
HYS64T128021GDL	HYB18T512800AC	512 Mbit	64M ×8
HYS64T128021HDL[2)]	HYB18T512800AF[2)]	512 Mbit	64M ×8

1) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.

2) Green Product

1.3 Pin Configuration

The pin configuration of the Small Outline DDR2 SDRAM DIMM is listed by function in **Table 5** (200 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**

Table 5 Pin Configuration of SO-DIMM

Pin#	Name	Pin Type	Buffer Type	Function
Clock Signals				
30	CK0	I	SSTL	**Clock Signals 2:0**
164	CK1	I	SSTL	
32	$\overline{CK0}$	I	SSTL	**Complement Clock Signals 2:0**
166	$\overline{CK1}$	I	SSTL	
79	CKE0	I	SSTL	**Clock Enable Rank 0**
80	CKE1	I	SSTL	**Clock Enable Rank 1** *Note: 2-rank module*
	NC	NC	—	*Note: 1-rank module*
Control Signals				
110	$\overline{S0}$	I	SSTL	**Chip Select Rank 0**
115	$\overline{S1}$	I	SSTL	**Chip Select Rank 1** *Note: 2-rank module*
	NC	NC	—	*Note: 1-rank module*
108	$\overline{RAS}$	I	SSTL	**Row Address Strobe**
113	$\overline{CAS}$	I	SSTL	**Column Address Strobe**
109	$\overline{WE}$	I	SSTL	**Write Enable**
Address Signals				
107	BA0	I	SSTL	**Bank Address Bus 1:0**
106	BA1	I	SSTL	
102	A0	I	SSTL	**Address Bus 4:0**
101	A1	I	SSTL	
100	A2	I	SSTL	
99	A3	I	SSTL	
98	A4	I	SSTL	

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
97	A5	I	SSTL	**Address Bus 11:5**
94	A6	I	SSTL	
92	A7	I	SSTL	
93	A8	I	SSTL	
91	A9	I	SSTL	
105	A10	I	SSTL	
	AP	I	SSTL	
90	A11	I	SSTL	
89	A12	I	SSTL	**Address Signal 12**
116	A13	I	SSTL	**Address Signal 13** *Note: 512M ×4/×8*
	NC	NC	—	*Note: Module based on 512 Mbit ×16*
Data Signals				
5	DQ0	I/O	SSTL	**Data Bus 26:0**
7	DQ1	I/O	SSTL	
17	DQ2	I/O	SSTL	
19	DQ3	I/O	SSTL	
4	DQ4	I/O	SSTL	
6	DQ5	I/O	SSTL	
14	DQ6	I/O	SSTL	
16	DQ7	I/O	SSTL	
23	DQ8	I/O	SSTL	
25	DQ9	I/O	SSTL	
35	DQ10	I/O	SSTL	
37	DQ11	I/O	SSTL	
20	DQ12	I/O	SSTL	
22	DQ13	I/O	SSTL	
36	DQ14	I/O	SSTL	
38	DQ15	I/O	SSTL	
43	DQ16	I/O	SSTL	
45	DQ17	I/O	SSTL	
55	DQ18	I/O	SSTL	
57	DQ19	I/O	SSTL	
44	DQ20	I/O	SSTL	
46	DQ21	I/O	SSTL	
56	DQ22	I/O	SSTL	
58	DQ23	I/O	SSTL	
61	DQ24	I/O	SSTL	
63	DQ25	I/O	SSTL	
73	DQ26	I/O	SSTL	

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
75	DQ27	I/O	SSTL	**Data Bus 63:27**
62	DQ28	I/O	SSTL	
64	DQ29	I/O	SSTL	
74	DQ30	I/O	SSTL	
76	DQ31	I/O	SSTL	
123	DQ32	I/O	SSTL	
125	DQ33	I/O	SSTL	
135	DQ34	I/O	SSTL	
137	DQ35	I/O	SSTL	
124	DQ36	I/O	SSTL	
126	DQ37	I/O	SSTL	
134	DQ38	I/O	SSTL	
136	DQ39	I/O	SSTL	
141	DQ40	I/O	SSTL	
143	DQ41	I/O	SSTL	
151	DQ42	I/O	SSTL	
153	DQ43	I/O	SSTL	
140	DQ44	I/O	SSTL	
142	DQ45	I/O	SSTL	
152	DQ46	I/O	SSTL	
154	DQ47	I/O	SSTL	
157	DQ48	I/O	SSTL	
159	DQ49	I/O	SSTL	
173	DQ50	I/O	SSTL	
175	DQ51	I/O	SSTL	
158	DQ52	I/O	SSTL	
160	DQ53	I/O	SSTL	
174	DQ54	I/O	SSTL	
176	DQ55	I/O	SSTL	
179	DQ56	I/O	SSTL	
181	DQ57	I/O	SSTL	
189	DQ58	I/O	SSTL	
191	DQ59	I/O	SSTL	
180	DQ60	I/O	SSTL	
182	DQ61	I/O	SSTL	
192	DQ62	I/O	SSTL	
194	DQ63	I/O	SSTL	
Data Strobe Signals				

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
13	DQS0	I/O	SSTL	**Data Strobe Bus 7:0**
31	DQS1	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
51	DQS2	I/O	SSTL	
70	DQS3	I/O	SSTL	
131	DQS4	I/O	SSTL	
148	DQS5	I/O	SSTL	
169	DQS6	I/O	SSTL	
188	DQS7	I/O	SSTL	
11	$\overline{\text{DQS0}}$	I/O	SSTL	**Complement Data Strobe Bus 7:0**
29	$\overline{\text{DQS1}}$	I/O	SSTL	*Note: See block diagram for corresponding DQ signals*
49	$\overline{\text{DQS2}}$	I/O	SSTL	
68	$\overline{\text{DQS3}}$	I/O	SSTL	
129	$\overline{\text{DQS4}}$	I/O	SSTL	
146	$\overline{\text{DQS5}}$	I/O	SSTL	
167	$\overline{\text{DQS6}}$	I/O	SSTL	
186	$\overline{\text{DQS7}}$	I/O	SSTL	
Data Mask Signals				
10	DM0	I	SSTL	**Data Mask Bus 7:0**
26	DM1	I	SSTL	
52	DM2	I	SSTL	
67	DM3	I	SSTL	
130	DM4	I	SSTL	
147	DM5	I	SSTL	
170	DM6	I	SSTL	
185	DM7	I	SSTL	
EEPROM				
197	SCL	I	CMOS	**Serial Bus Clock**
195	SDA	I/O	OD	**Serial Bus Data**
198	SA0	I	CMOS	**Slave Address Select Bus 2:0**
200	SA1	I	CMOS	
Power Supplies				
1	V_{REF}	AI	—	**I/O Reference Voltage**
199	V_{DDSPD}	PWR	—	**EEPROM Power Supply**
81,82,87,88,95,96,103,104, 111,112,117,118	V_{DD}	PWR	—	**Power Supply**
2,3,8,9,12,15,18,21,24,27,28, 33,34,39,40,41,42,47,48,53, 54,59,60,65,66,71,72,77,78, 121,122,127,128,132,133,138, 139,144,145,149,150,155,156, 161,162,165,168,171,172,177, 178,183,184,187,190,193,196	V_{SS}	GND	—	**Ground Plane**

Table 5 Pin Configuration of SO-DIMM (cont'd)

Pin#	Name	Pin Type	Buffer Type	Function
Other Pins				
114	ODT0			**On-Die Termination Control 0**
119	ODT1			**On-Die Termination Control 1**
	NC			*Note: 1 Rank modules*
50,69,83,84,85,120,163	NC	NC	—	**Not connected** *Note: Pins not connected on Infineon SO-DIMMs*

Table 6 Abbreviations for Pin Type

Abbreviation	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 7 Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

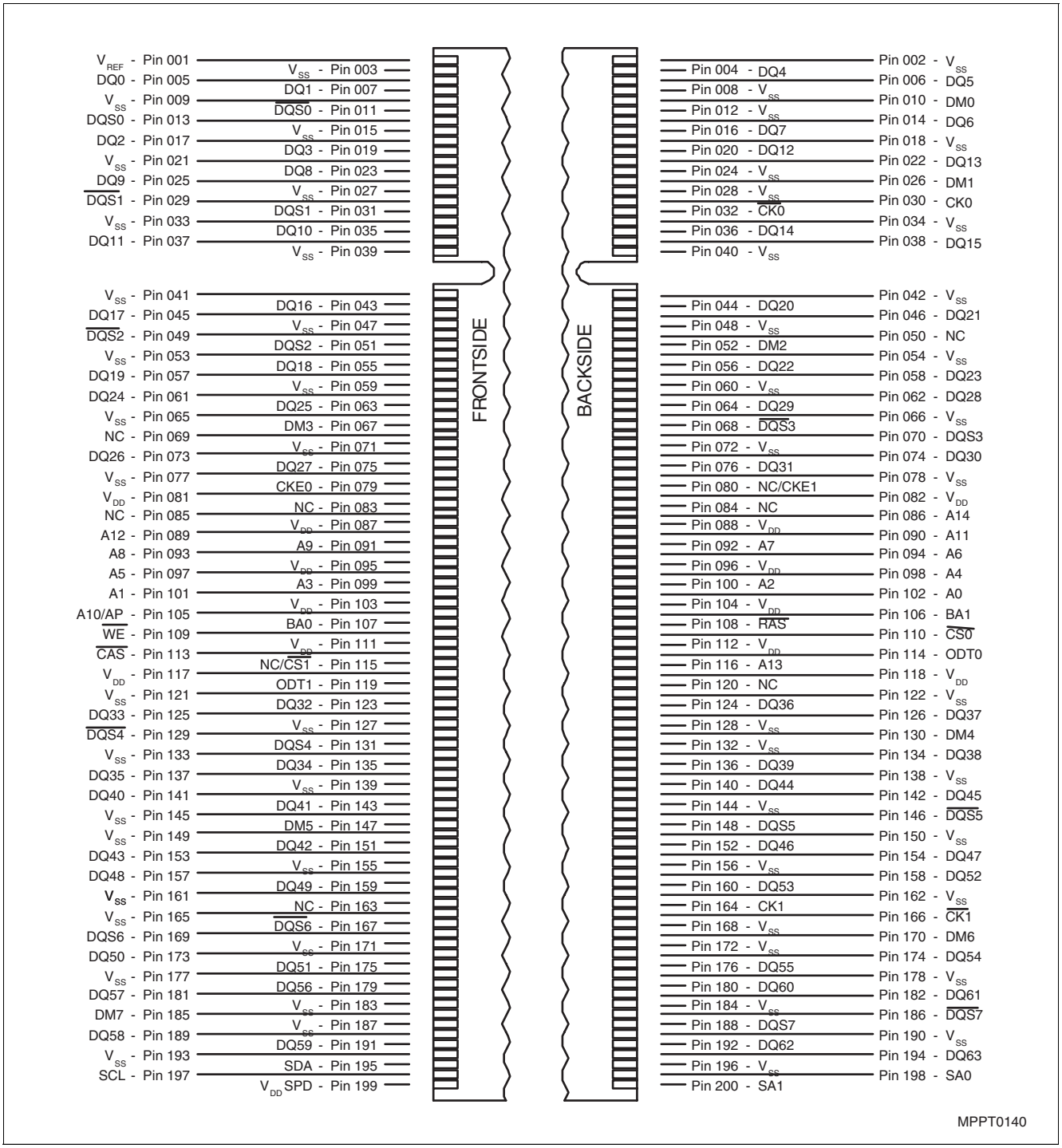

Figure 1 Pin Configuration SO-DIMM (200 Pin)

Table 8 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK[1:0], $\overline{CK}$[1:0]	I	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	I	Active High	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down Mode or the Self Refresh Mode.
$\overline{S}$[1:0]	I	Active Low	Enables the associated DDR2 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	I	Active Low	When sampled at the cross point of the rising edge of CK,and falling edge of $\overline{CK}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[1:0]	I	—	Selects internal SDRAM memory bank
ODT[1:0]	I	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR2 SDRAM mode register.
A[9:0], A10/AP, A[13:11]	I	—	During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0] inputs. If AP is low, then BA[1:0] are used to define which bank to precharge.
DQ[63:0]	I/O	—	Data Input/Output pins
DM[7:0]	I	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$. If the module is to be operated in single ended strobe mode, all $\overline{DQS}$ signals must be tied on the system board to V_{SS} through a 20 ohm to 10 Kohm resistor and DDR2 SDRAM mode registers programmed appropriately.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	—	Power supplies for core, I/O, Serial Presence Detect, and ground for the module.
SDA	I/O	—	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to V_{DDSPD} on the motherboard to act as a pull-up.
SCL	I	—	This signal is used to clock data into and out of the SPD EEPROM.
SA[1:0]	I	—	Address pins used to select the Serial Presence Detect base address.

2 Block Diagrams

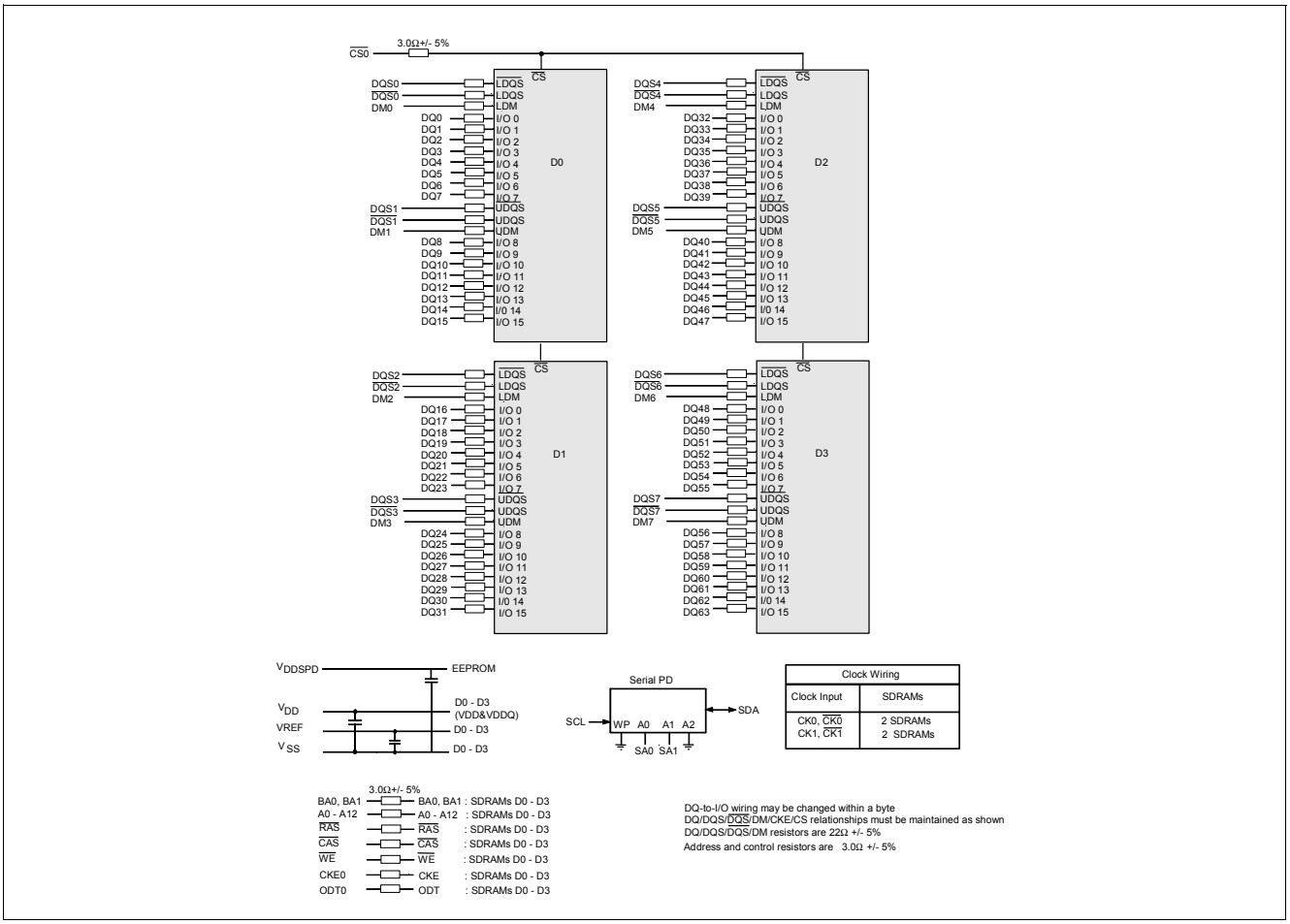

Figure 2 Block Diagram Raw Card C (32M x 64, 1 rank, x16)

Note

1. *DQ, DQS, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, S1, BAn, An, RAS, CAS, WE, ODT0, ODT1, CKEO, CKE1 resistors are 3 Ω ±5 %*

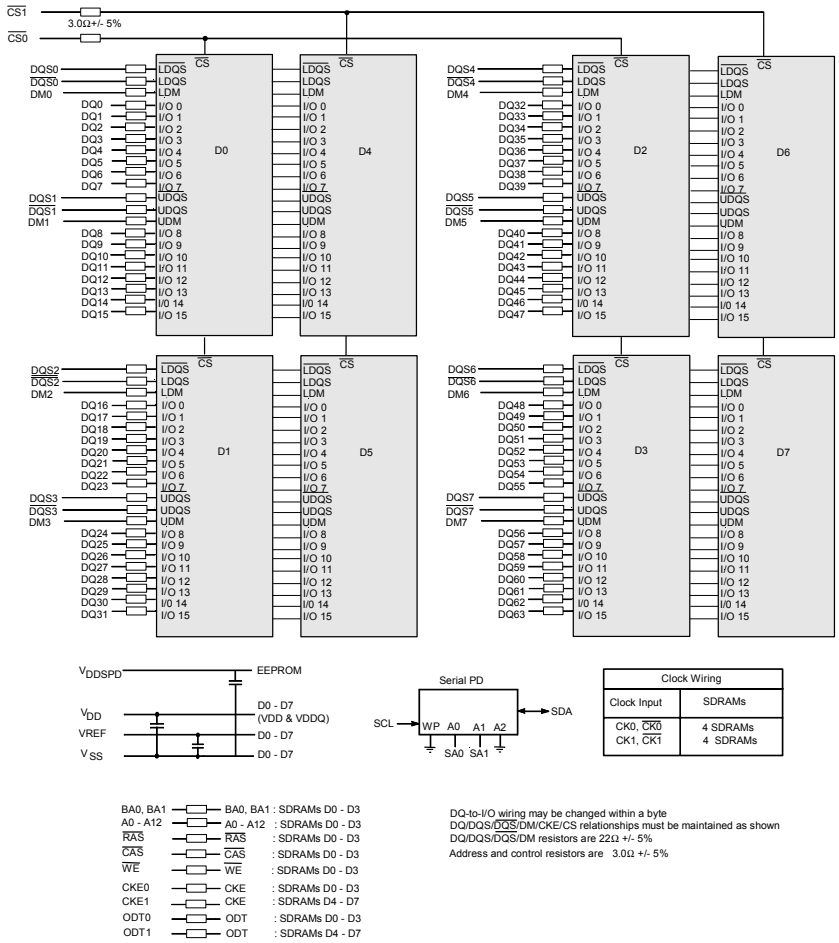

Figure 3 Block Diagram Raw Card A (64M x 64, 2 ranks, x16)

Note

1. *DQ, DQS, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, S1, BAn, An, RAS, CAS, WE, ODT0, ODT1, CKEO, CKE1 resistors are 3 Ω ±5 %*

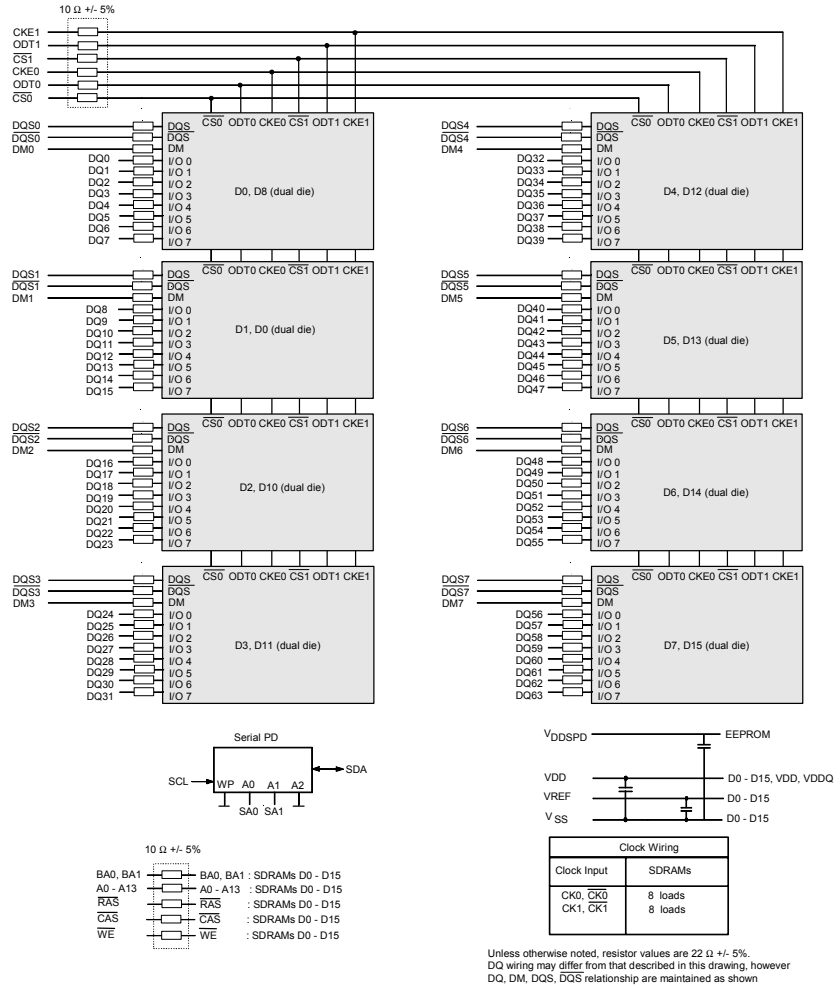

Figure 4 Block Diagram Raw Card D (128M x 64, 2 ranks, x8)

Note

1. *DQ, DQS, DQS, DM resistors are 22 Ω ±5 %*
2. *S0, S1, BAn, An, RAS, CAS, WE, ODT0, ODT1, CKE0, CKE1 resistors are 3 Ω ±5 %*

3 Electrical Characteristics

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/Test Condition
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	– 0.5	2.3	V	1)
Voltage on V_{DD} relative to V_{SS}	V_{DD}	– 1.0	2.3	V	1)
Voltage on $V_{DD\,Q}$ relative to V_{SS}	V_{DDQ}	– 0.5	2.3		1)
Barometric Pressure (operating & storage)		+69	+105	kPa	1)
Storage Humidity (without condensation)	H_{STG}	5	95	%	1)

1) *Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

Table 10 Operating Temperature Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+65	°C	
DRAM Component Case Temperature Range	T_{CASE}	0	+95	°C	1)2)3)4)
Storage temperature	T_{STG}	– 55	+100	°C	
Barometric Pressure (operating & storage)		+69	+105	kPa	5)
Operating Humidity (relative)	H_{OPR}	10	90	%	

1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2

2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported

3) Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9 µs.

4) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.

5) Up to 3000 m.

Table 11 Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Nom.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 × V_{DDQ}	0.5 × V_{DDQ}	0.51 × V_{DDQ}	V	2)
SPD Supply Voltage	V_{DDSPD}	1.7	—	3.6	V	
DC Input Logic High	$V_{IH\,(DC)}$	V_{REF} + 0.125	—	V_{DDQ} +0.3	V	
DC Input Logic Low	$V_{IL\,(DC)}$	– 0.30	—	V_{REF} –0.125	V	
In / Output Leakage Current	I_L	– 5	—	5	µA	3)

1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}

2) Peak to peak AC noise on V_{REF} may not exceed ± 2% V_{REF} (DC). V_{REF} is also expected to track noise variations in V_{DDQ}.

3) For any pin on the DIMM connector under test input of 0 V ≤ V_{IN} ≤ V_{DDQ} + 0.3 V.

4 I_{DD} Specifications and Conditions

Table 12 I_{DD} Measurement Conditions[1)2)]

Parameter	Symbol
Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, CKE is HIGH, CS is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD0}
Operating Current 1 One bank Active - Read - Precharge; I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CKmin.}$, $t_{RC} = t_{RCmin.}$, $t_{RAS} = t_{RASmin.}$, $t_{RCD} = t_{RCDmin.}$,AL = 0, CL = $CL_{min.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	I_{DD1}
Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2P}
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD2N}
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CKmin.}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	I_{DD2Q}
Active Power-Down Current All banks open; $t_{CK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “0” (Fast Power-down Exit);	$I_{DD3P(0)}$
Active Power-Down Current All banks open; $_{tCK} = t_{CKmin.}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to “1” (Slow Power-down Exit);	$I_{DD3P(1)}$
Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD3N}
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; I_{OUT} = 0 mA.	I_{DD4R}
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{min.}$; $t_{CK} = t_{CKmin.}$; $t_{RAS} = t_{RASmax.}$, $t_{RP} = t_{RPmin.}$; CKE is HIGH, $\overline{CS}$ is high between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	I_{DD4W}
Burst Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{RFCmin.}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5B}
Distributed Refresh Current $t_{CK} = t_{CKmin.}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	I_{DD5D}

Table 12 I_{DD} Measurement Conditions[1)2)] (cont'd)

Parameter	Symbol
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. RESET = Low. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max.	I_{DD6}
All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. I_{out} = 0 mA.	I_{DD7}

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V

2) For details and notes see the relevant INFINEON component data sheet

Table 13 I_{DD} Specification HYS64T[32000/64020][G/H]DL

Product Type	HYS64T32000GDL-5-A	HYS64T32000HDL-5-A	HYS64T64020GDL-5-A	HYS64T64020HDL-5-A	HYS64T32000GDL-3.7-A	HYS64T32000HDL-3.7-A	HYS64T64020GDL-3.7-A	HYS64T64020HDL-3.7-A	Unit	Notes
Organization	**256 MB**	**256 MB**	**512 MB**	**512 MB**	**256 MB**	**256 MB**	**512 MB**	**512 MB**		
	×64	**×64**	**×64**	**×64**	**×64**	**×64**	**×64**	**×64**		
	1 Rank	**1 Rank**	**2 Ranks**	**2 Ranks**	**1 Rank**	**1 Rank**	**2 Ranks**	**2 Ranks**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	280	280	300	300	320	320	340	340	mA	1)2)
I_{DD1}	300	300	320	320	360	360	380	380	mA	1)2)
I_{DD2P}	20	20	30	30	20	20	30	30	mA	1)3)
I_{DD2N}	130	130	260	260	160	160	320	320	mA	1)3)
I_{DD2Q}	100	100	200	200	120	120	240	240	mA	1)3)
$I_{DD3P(MRS=0)}$	50	50	100	100	60	60	130	130	mA	1)3)
$I_{DD3P(MRS=1)}$	20	20	40	40	20	20	40	40	mA	1)3)
I_{DD3N}	140	140	280	280	160	160	320	320	mA	1)3)
I_{DD4R}	340	340	360	360	400	400	420	420	mA	1)2)
I_{DD4W}	360	360	380	380	440	440	460	460	mA	1)2)
I_{DD5B}	480	480	500	500	520	520	540	540	mA	1)2)
I_{DD5D}	20	20	50	50	20	20	50	50	mA	1)3)
I_{DD6}	20	20	30	30	20	20	30	30	mA	1)4)
I_{DD7}	840	840	860	860	880	880	900	900	mA	1)2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in IDD2P Precharge Power-Down Standby Current mode

3) Both ranks are in the same IDD current mode

4) standard

Table 14 I_{DD} Specification HYS64T128021[G/H]DL

Product Type	HYS64T128021GDL-5-A	HYS64T128021HDL-5-A	HYS64T128021GDL-3.7-A	HYS64T128021HDL-3.7-A	Unit	Notes
Organization	**1 GB**	**1 GB**	**1 GB**	**1 GB**		
	×64	**×64**	**×64**	**×64**		
	2 Ranks	**2 Ranks**	**2 Ranks**	**2 Ranks**		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**		
I_{DD0}	472	472	552	552	mA	1)2)
I_{DD1}	512	512	632	632	mA	1)2)
I_{DD2P}	64	64	64	64	mA	1)3)
I_{DD2N}	512	512	640	640	mA	1)3)
I_{DD2Q}	400	400	480	480	mA	1)3)
$I_{DD3P(MRS=0)}$	208	208	256	256	mA	1)3)
$I_{DD3P(MRS=1)}$	80	80	80	80	mA	1)3)
I_{DD3N}	560	560	640	640	mA	1)3)
I_{DD4R}	592	592	752	752	mA	1)2)
I_{DD4W}	632	632	792	792	mA	1)2)
I_{DD5B}	976	976	1060	1060	mA	1)2)
I_{DD5D}	96	96	96	96	mA	1)3)
I_{DD6}	64	64	64	64	mA	1)4)
I_{DD7}	1072	1072	1312	1312	mA	1)2)

1) Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R} and I_{DD7} are defined with the outputs disabled

2) The other rank is in IDD2P Precharge Power-Down Standby Current mode

3) Both ranks are in the same IDD current mode

4) standard

4.1 I_{DD} Test Conditions

For testing the IDD parameters, the timing parameters as in **Table 15** are used.

Table 15 I_{DD} Measurement Test Condition

Parameter	Symbol	-3.7	-5	Unit
		PC2-4200-4-4-4	PC2-3200-3-3-3	
CAS Latency	CL_{min}	4	3	t_{CK}
Clock Cycle Time	t_{CKmin}	3.75	5	ns
Active to Read or Write delay	t_{RCDmin}	15	15	ns
Active to Active / Auto-Refresh command period	t_{RCmin}	60	55	ns
Active bank A to Active bank B command delay	t_{RRDmin}	10	10	ns
Active to Precharge Command	t_{RASmin}	45	40	ns
	t_{RASmax}	70000	70000	ns
Precharge Command Period	t_{RPmin}	15	15	ns
Auto-Refresh to Active / Auto-Refresh command period	t_{RFCmin}	105	105	ns
Average periodic Refresh interval	t_{REFI}	7.8	7.8	µs

4.2 ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-state or driving “0” or “1”, as long a ODT is enabled during a given period of time.

Table 16 ODT current per terminated pin

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODTO}	5	6	7.5	mA/DQ	A6 = 0, A2 = 1
		2.5	3	3.75	mA/DQ	A6 = 1, A2 = 0
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6 = 0, A2 = 1
		5	6	7.5	mA/DQ	A6 = 1, A2 = 0

Note: For power consumption calculations the ODT duty cycle has to be taken into account

5 Electrical Characteristics & AC Timings

Table 17 AC Timing - Absolute Specificatioins –5/–3.7

Parameter	Symbol	–3.7		–5		Unit	Notes
		PC2-4200S		PC2-3200S			
		Min.	Max.	Min.	Max.		
DQ output access time from CK/$\overline{CK}$	t_{AC}	-500	+500	–600	+600	ps	1)
DQS output access time from CK/$\overline{CK}$	t_{DQSCK}	–450	+450	–500	+500	ps	1)
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	1)
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	1)
Clock Half Period	t_{HP}	min. (t_{CL}, t_{CH})		min. (t_{CL}, t_{CH})		t_{CK}	1)
Clock cycle time	t_{CK}	5000	8000	5000	8000	ps	1)2)
		3750	8000	5000	8000	ps	1)3)
Address and control input setup time	t_{IS}	600	—	600	—	ps	1)
Address and control input hold time	t_{IH}	600	—	600	—	ps	1)
DQ and DM input hold time	t_{DH}	350	—	400	—	ps	1)
DQ and DM input setup time	t_{DS}	350	—	400	—	ps	1)
Control and Addr. input pulse width (each input)	t_{IPW}	0.6	—	0.6	—	t_{CK}	1)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	0.35	—	t_{CK}	1)
Data-out high-impedance time from CK/$\overline{CK}$	t_{HZ}	—	t_{ACmax}	—	t_{ACmax}	ps	1)
DQ low-impedance from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2\times t_{ACmin}$	t_{ACmax}	$2\times t_{ACmin}$	t_{ACmax}	ps	1)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	t_{ACmin}	t_{ACmax}	t_{ACmin}	t_{ACmax}	ps	1)
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	—	350	ps	1)
Data hold skew factor	t_{QHS}	—	400	—	450	ps	1)
Data Output hold time from DQS	t_{QH}	$t_{HP}-t_{QHS}$	—	$t_{HP}-t_{QHS}$	—	t_{CK}	1)
Write command to 1st DQS latching transition	t_{DQSS}	WL - 0.25	WL + 0.25	WL – 0.25	WL + 0.25	t_{CK}	1)
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	0.35	—	t_{CK}	1)
DQS falling edge to CLK setup time (write cycle)	t_{DSS}	0.2	—	0.2	—	t_{CK}	1)
DQS falling edge hold time from CLK (write cycle)	t_{DSH}	0.2	—	0.2	—	t_{CK}	1)
Mode register set command cycle time	t_{MRD}	2	—	2	—	t_{CK}	1)
Write preamble	t_{WPRE}	0.25	—	0.25	—	t_{CK}	1)
Write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}	1)
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}	1)
Read postamble	t_{RPST}	0.40	0.60	0.40	0.60	t_{CK}	1)
Active to Precharge command	t_{RAS}	45	70000	40	70000	ns	1)

Table 17 AC Timing - Absolute Specificatioins –5/–3.7

Parameter	Symbol	–3.7		–5		Unit	Notes
		PC2-4200S		PC2-3200S			
		Min.	Max.	Min.	Max.		
Active to Active/Auto-refresh command period	t_{RC}	60	—	55	—	ns	1)
Auto-refresh to Active/Auto-refresh command period	t_{RFC}	105	—	105	—	ns	1)
Active to Read or Write delay (with and without Auto-Precharge) delay	t_{RCD}	15	—	15	—	ns	1)
Precharge command period	t_{RP}	15	—	15	—	ns	1)
Active bank A to Active bank B command	t_{RRD}	10	—	10	—	ns	1)
$\overline{CAS}$ A to $\overline{CAS}$ B Command Period	t_{CCD}	2	—	2	—	t_{CK}	1)
Write recovery time	t_{WR}	15	—	15	—	ns	1)
Auto precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	WR + t_{RP}	—	t_{CK}	1)
Internal write to read command delay	t_{WTR}	7.5	—	10	—	ns	1)
Internal read to precharge command delay	t_{RTP}	7.5	—	7.5	—	ns	1)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	2	—	t_{CK}	1)
Exit active power-down mode to read command (slew exit, lower power)	t_{XARDS}	6 – AL	—	6 – AL	—	t_{CK}	1)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	2	—	t_{CK}	1)
Exit Self-Refresh to read command	t_{XSRD}	200	—	200	—	t_{CK}	1)
Exit Self-Refresh to non-read command	t_{XSNR}	t_{RFC} + 10	—	t_{RFC} + 10	—	ns	1)
CKE minimum high and low pulse width	t_{CKE}	3	—	3	—	t_{CK}	1)
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	1)
Minimum time clocks remain ON after CKE asynchronously drops low	t_{DELAY}	t_{IS} + t_{CK} + t_{IH}	—	t_{IS} + t_{CK}+ t_{IH}	—	ns	1)
Average Periodic Refresh Interval	t_{REFI}	—	7.8	—	7.8	µs	1)4)
		—	3.9	—	3.9		1)5)

1) For details and notes see the relevant INFINEON component datasheet
2) CL = 3
3) CL = 4 & 5
4) 0 °C ≤ T_{CASE} ≤ 85 °C
5) 85 °C < T_{CASE} ≤ 95 °C

Table 18 ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

Symbol	Parameter / Condition	Min.	Max.	Unit
t_{AOND}	ODT turn-on delay	2	2	t_{CK}
t_{AON}	ODT turn-on	$t_{AC(min)}$	$t_{AC(max)}$ + 1 ns	ns
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC(min)}$ + 2 ns	2 t_{CK} + $t_{AC(max)}$ + 1 ns	ns
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}
t_{AOF}	ODT turn-off	$t_{AC(min)}$	$t_{AC(max)}$ + 0.6 ns	ns
t_{AOFPD}	ODT turn-off delay (Power-Down Modes)	$t_{AC(min)}$ + 2 ns	2.5 t_{CK} + $t_{AC(max)}$ + 1 ns	ns
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}

6 SPD Codes

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		**HYS64T64020GDL–3.7–A**	**HYS64T64020HDL–3.7–A**	**HYS64T32000GDL–3.7–A**	**HYS64T32000HDL–3.7–A**
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	60	60
6	Data Width	40	40	40	40
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	3D	3D
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	00	00	00	00
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	10	10	10	10
14	Error Checking SDRAM Width	00	00	00	00

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		HYS64T64020GDL–3.7–A	HYS64T64020HDL–3.7–A	HYS64T32000GDL–3.7–A	HYS64T32000HDL–3.7–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
15	Not used	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	Not used	00	00	00	00
20	DIMM Type Information	04	04	04	04
21	DIMM Attributes	00	00	00	00
22	Component Attributes	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	3D	3D
24	t_{AC} SDRAM @ CL_{max} - 1 [ns]	50	50	50	50
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} - 2 [ns]	60	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.min}$ [ns]	28	28	28	28
29	$t_{RCD.min}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	40	40	40	40
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25	25	25
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37	37	37
34	$t_{DS.min}$ [ns]	10	10	10	10
35	$t_{DH.min}$ [ns]	22	22	22	22

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		HYS64T64020GDL–3.7–A	HYS64T64020HDL–3.7–A	HYS64T32000GDL–3.7–A	HYS64T32000HDL–3.7–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
36	$t_{WR.min}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E	1E	1E
38	$t_{RTP.min}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E	1E	1E
45	$t_{QHS.max}$ [ns]	28	28	28	28
46	PLL Relock Time	00	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	53	53	53	53
48	Psi(T-A) DRAM	72	72	72	72
49	ΔT_0 (DT0)	52	52	52	52
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2B	2B	2B	2B
51	ΔT_{2P} (DT2P)	1D	1D	1D	1D
52	ΔT_{3N} (DT3N)	1D	1D	1D	1D
53	$\Delta T_{3P.fast}$ (DT3P fast)	23	23	23	23
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	16	16	16
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} S Sign (DT4R4W)	36	36	36	36
56	ΔT_{5B} (DT5B)	1C	1C	1C	1C
57	ΔT_7 (DT7)	30	30	30	30
58	Psi(ca) PLL	00	00	00	00
59	Psi(ca) REG	00	00	00	00

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		**HYS64T64020GDL–3.7–A**	**HYS64T64020HDL–3.7–A**	**HYS64T32000GDL–3.7–A**	**HYS64T32000HDL–3.7–A**
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
60	ΔT_{PLL} (DTPLL)	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	11	11	11	11
63	Checksum of Bytes 0-62	BC	BC	BB	BB
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36
74	Product Type, Char 2	34	34	34	34
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	36	33	33
77	Product Type, Char 5	34	34	32	32
78	Product Type, Char 6	30	30	30	30

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		HYS64T64020GDL–3.7–A	HYS64T64020HDL–3.7–A	HYS64T32000GDL–3.7–A	HYS64T32000HDL–3.7–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
79	Product Type, Char 7	32	32	30	30
80	Product Type, Char 8	30	30	30	30
81	Product Type, Char 9	47	48	47	48
82	Product Type, Char 10	44	44	44	44
83	Product Type, Char 11	4C	4C	4C	4C
84	Product Type, Char 12	33	33	33	33
85	Product Type, Char 13	2E	2E	2E	2E
86	Product Type, Char 14	37	37	37	37
87	Product Type, Char 15	41	41	41	41
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Manufacturing Date Week	xx	xx	xx	xx

Table 19 SPD Codes for HYS 64T[32000/64020] PC2–4200S

Product Type		HYS64T64020GDL–3.7–A	HYS64T64020HDL–3.7–A	HYS64T32000GDL–3.7–A	HYS64T32000HDL–3.7–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**	**PC2–4200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
96	Module Serial Number (1)	xx	xx	xx	xx
97	Module Serial Number (2)	xx	xx	xx	xx
98	Module Serial Number (3)	xx	xx	xx	xx
99	Module Serial Number (4)	xx	xx	xx	xx
100 - 127	Not used	00	00	00	00
128-255	BLANK	FF	FF	FF	FF

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0D	0D	0D	0D
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	60	60
6	Data Width	40	40	40	40
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	50	50	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	60	60	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	00	00
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	10	10	10	10
14	Error Checking SDRAM Width	00	00	00	00
15	Not used	00	00	00	00

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	Not used	00	00	00	00
20	DIMM Type Information	04	04	04	04
21	DIMM Attributes	00	00	00	00
22	Component Attributes	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	50	50	50	50
24	t_{AC} SDRAM @ CL_{max} - 1 [ns]	60	60	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} - 2 [ns]	60	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.min}$ [ns]	28	28	28	28
29	$t_{RCD.min}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	40	40	40	40
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	35	35	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	47	47	47	47
34	$t_{DS.min}$ [ns]	15	15	15	15
35	$t_{DH.min}$ [ns]	27	27	27	27
36	$t_{WR.min}$ [ns]	3C	3C	3C	3C

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
37	$t_{WTR.min}$ [ns]	28	28	28	28
38	$t_{RTP.min}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80	80
44	$t_{DQSQ.max}$ [ns]	23	23	23	23
45	$t_{QHS.max}$ [ns]	2D	2D	2D	2D
46	PLL Relock Time	00	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51	51
48	Psi(T-A) DRAM	72	72	72	72
49	ΔT_0 (DT0)	42	42	42	42
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	23	23	23	23
51	ΔT_{2P} (DT2P)	1D	1D	1D	1D
52	ΔT_{3N} (DT3N)	19	19	19	19
53	$\Delta T_{3P.fast}$ (DT3P fast)	1C	1C	1C	1C
54	$\Delta T_{3P.slow}$ (DT3P slow)	16	16	16	16
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} S Sign (DT4R4W)	2E	2E	2E	2E
56	ΔT_{5B} (DT5B)	1A	1A	1A	1A
57	ΔT_7 (DT7)	2D	2D	2D	2D
58	Psi(ca) PLL	00	00	00	00
59	Psi(ca) REG	00	00	00	00
60	ΔT_{PLL} (DTPLL)	00	00	00	00

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	11	11	11	11
63	Checksum of Bytes 0-62	0E	0E	0D	0D
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36
74	Product Type, Char 2	34	34	34	34
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	36	36	33	33
77	Product Type, Char 5	34	34	32	32
78	Product Type, Char 6	30	30	30	30
79	Product Type, Char 7	32	32	30	30
80	Product Type, Char 8	30	30	30	30

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
81	Product Type, Char 9	47	48	47	48
82	Product Type, Char 10	44	44	44	44
83	Product Type, Char 11	4C	4C	4C	4C
84	Product Type, Char 12	35	35	35	35
85	Product Type, Char 13	41	41	41	41
86	Product Type, Char 14	20	20	20	20
87	Product Type, Char 15	20	20	20	20
88	Product Type, Char 16	20	20	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	1x	1x	1x	1x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Manufacturing Date Week	xx	xx	xx	xx
96	Module Serial Number (1)	xx	xx	xx	xx

Table 20 SPD Codes for HYS 64T[32000/64020] PC2-3200S

Product Type		HYS64T64020GDL–5–A	HYS64T64020HDL–5–A	HYS64T32000GDL–5–A	HYS64T32000HDL–5–A
Organization		**512 MB**	**512 MB**	**256 MB**	**256 MB**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×16)	**2 Ranks (×16)**	**1 Rank (×16)**	**1 Rank (×16)**
Label Code		**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**	**PC2–3200S–333**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
97	Module Serial Number (2)	xx	xx	xx	xx
98	Module Serial Number (3)	xx	xx	xx	xx
99	Module Serial Number (4)	xx	xx	xx	xx
100 - 127	Not used	00	00	00	00
128-255	BLANK	FF	FF	FF	FF

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		HYS64T128021HDL–3.7–A	HYS64T128021GDL–3.7–A	HYS64T128021HDL–5–A	HYS64T128021GDL–5–A
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
0	Programmed SPD Bytes in EEPROM	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E
4	Number of Column Addresses	0A	0A	0A	0A
5	DIMM Rank and Stacking Information	61	61	61	61
6	Data Width	40	40	40	40
7	Not used	00	00	00	00
8	Interface Voltage Level	05	05	05	05
9	t_{CK} @ CL_{max} (Byte 18) [ns]	3D	3D	50	50
10	t_{AC} SDRAM @ CL_{max} (Byte 18) [ns]	50	50	60	60
11	Error Correction Support (non-ECC, ECC)	00	00	00	00
12	Refresh Rate and Type	82	82	82	82
13	Primary SDRAM Width	08	08	08	08
14	Error Checking SDRAM Width	00	00	00	00
15	Not used	00	00	00	00

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		HYS64T128021HDL–3.7–A	HYS64T128021GDL–3.7–A	HYS64T128021HDL–5–A	HYS64T128021GDL–5–A
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
16	Burst Length Supported	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04
18	Supported CAS Latencies	38	38	38	38
19	Not used	00	00	00	00
20	DIMM Type Information	04	04	04	04
21	DIMM Attributes	00	00	00	00
22	Component Attributes	01	01	01	01
23	t_{CK} @ CL_{max} -1 (Byte 18) [ns]	3D	3D	50	50
24	t_{AC} SDRAM @ CL_{max} - 1 [ns]	50	50	60	60
25	t_{CK} @ CL_{max} -2 (Byte 18) [ns]	50	50	50	50
26	t_{AC} SDRAM @ CL_{max} - 2 [ns]	60	60	60	60
27	$t_{RP.min}$ [ns]	3C	3C	3C	3C
28	$t_{RRD.min}$ [ns]	1E	1E	1E	1E
29	$t_{RCD.min}$ [ns]	3C	3C	3C	3C
30	$t_{RAS.min}$ [ns]	2D	2D	2D	2D
31	Module Density per Rank	80	80	80	80
32	$t_{AS.min}$ and $t_{CS.min}$ [ns]	25	25	35	35
33	$t_{AH.min}$ and $t_{CH.min}$ [ns]	37	37	47	47
34	$t_{DS.min}$ [ns]	10	10	15	15
35	$t_{DH.min}$ [ns]	22	22	27	27

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		HYS64T128021HDL–3.7–A	HYS64T128021GDL–3.7–A	HYS64T128021HDL–5–A	HYS64T128021GDL–5–A
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
36	$t_{WR.min}$ [ns]	3C	3C	3C	3C
37	$t_{WTR.min}$ [ns]	1E	1E	28	28
38	$t_{RTP.min}$ [ns]	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00
40	t_{RC} and t_{RFC} Extension	00	00	00	00
41	$t_{RC.min}$ [ns]	3C	3C	3C	3C
42	$t_{RFC.min}$ [ns]	69	69	69	69
43	$t_{CK.max}$ [ns]	80	80	80	80
44	$t_{DQSQ.max}$ [ns]	1E	1E	23	23
45	$t_{QHS.max}$ [ns]	28	28	2D	2D
46	PLL Relock Time	00	00	00	00
47	$T_{CASE.max}$ Delta / ΔT_{4R4W} Delta	51	51	51	51
48	Psi(T-A) DRAM	78	78	78	78
49	ΔT_0 (DT0)	3E	3E	32	32
50	ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} ((DT2Q, RDIMM)	2E	2E	24	24
51	ΔT_{2P} (DT2P)	1E	1E	1E	1E
52	ΔT_{3N} (DT3N)	1E	1E	1B	1B
53	$\Delta T_{3P.fast}$ (DT3P fast)	24	24	1E	1E
54	$\Delta T_{3P.slow}$ (DT3P slow)	17	17	17	17
55	ΔT_{4R} (DT4R) / ΔT_{4R4W} S Sign (DT4R4W)	34	34	28	28
56	ΔT_{5B} (DT5B)	1E	1E	1B	1B
57	ΔT_7 (DT7)	20	20	1E	1E
58	Psi(ca) PLL	00	00	00	00
59	Psi(ca) REG	00	00	00	00

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		HYS64T128021HDL–3.7–A	HYS64T128021GDL–3.7–A	HYS64T128021HDL–5–A	HYS64T128021GDL–5–A
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
60	ΔT_{PLL} (DTPLL)	00	00	00	00
61	ΔT_{REG} (DTREG) / Toggle Rate	00	00	00	00
62	SPD Revision	11	11	11	11
63	Checksum of Bytes 0-62	D2	D2	26	26
64	JEDEC ID Code of Infineon (1)	C1	C1	C1	C1
65	JEDEC ID Code of Infineon (2)	00	00	00	00
66	JEDEC ID Code of Infineon (3)	00	00	00	00
67	JEDEC ID Code of Infineon (4)	00	00	00	00
68	JEDEC ID Code of Infineon (5)	00	00	00	00
69	JEDEC ID Code of Infineon (6)	00	00	00	00
70	JEDEC ID Code of Infineon (7)	00	00	00	00
71	JEDEC ID Code of Infineon (8)	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx
73	Product Type, Char 1	36	36	36	36
74	Product Type, Char 2	34	34	34	34
75	Product Type, Char 3	54	54	54	54
76	Product Type, Char 4	31	31	31	31
77	Product Type, Char 5	32	32	32	32
78	Product Type, Char 6	38	38	38	38

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		HYS64T128021HDL–3.7–A	HYS64T128021GDL–3.7–A	HYS64T128021HDL–5–A	HYS64T128021GDL–5–A
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
79	Product Type, Char 7	30	30	30	30
80	Product Type, Char 8	32	32	32	32
81	Product Type, Char 9	31	31	31	31
82	Product Type, Char 10	48	47	48	47
83	Product Type, Char 11	44	44	44	44
84	Product Type, Char 12	4C	4C	4C	4C
85	Product Type, Char 13	33	33	35	35
86	Product Type, Char 14	2E	2E	41	41
87	Product Type, Char 15	37	37	20	20
88	Product Type, Char 16	41	41	20	20
89	Product Type, Char 17	20	20	20	20
90	Product Type, Char 18	20	20	20	20
91	Module Revision Code	0x	0x	0x	0x
92	Test Program Revision Code	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx
95	Module Manufacturing Date Week	xx	xx	xx	xx
96	Module Serial Number (1)	xx	xx	xx	xx
97	Module Serial Number (2)	xx	xx	xx	xx
98	Module Serial Number (3)	xx	xx	xx	xx

Table 21 SPD Codes for HYS64T128021[G/H]DL

Product Type		**HYS64T128021HDL–3.7–A**	**HYS64T128021GDL–3.7–A**	**HYS64T128021HDL–5–A**	**HYS64T128021GDL–5–A**
Organization		**1 GByte**	**1 GByte**	**1 GByte**	**1 GByte**
		×64	**×64**	**×64**	**×64**
		2 Ranks (×8)	**2 Ranks (×8)**	**2 Ranks (×8)**	**2 Ranks (×8)**
Label Code		**PC2–4200S–444**	**PC2–4200S–444**	**PC2–3200S–444**	**PC2–3200S–444**
JEDEC SPD Revision		**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**	**Rev. 1.1**
Byte#	**Description**	**HEX**	**HEX**	**HEX**	**HEX**
99	Module Serial Number (4)	xx	xx	xx	xx
100 - 127	Not used	00	00	00	00
128- 255	BLANK	FF	FF	FF	FF

7 Package Outlines

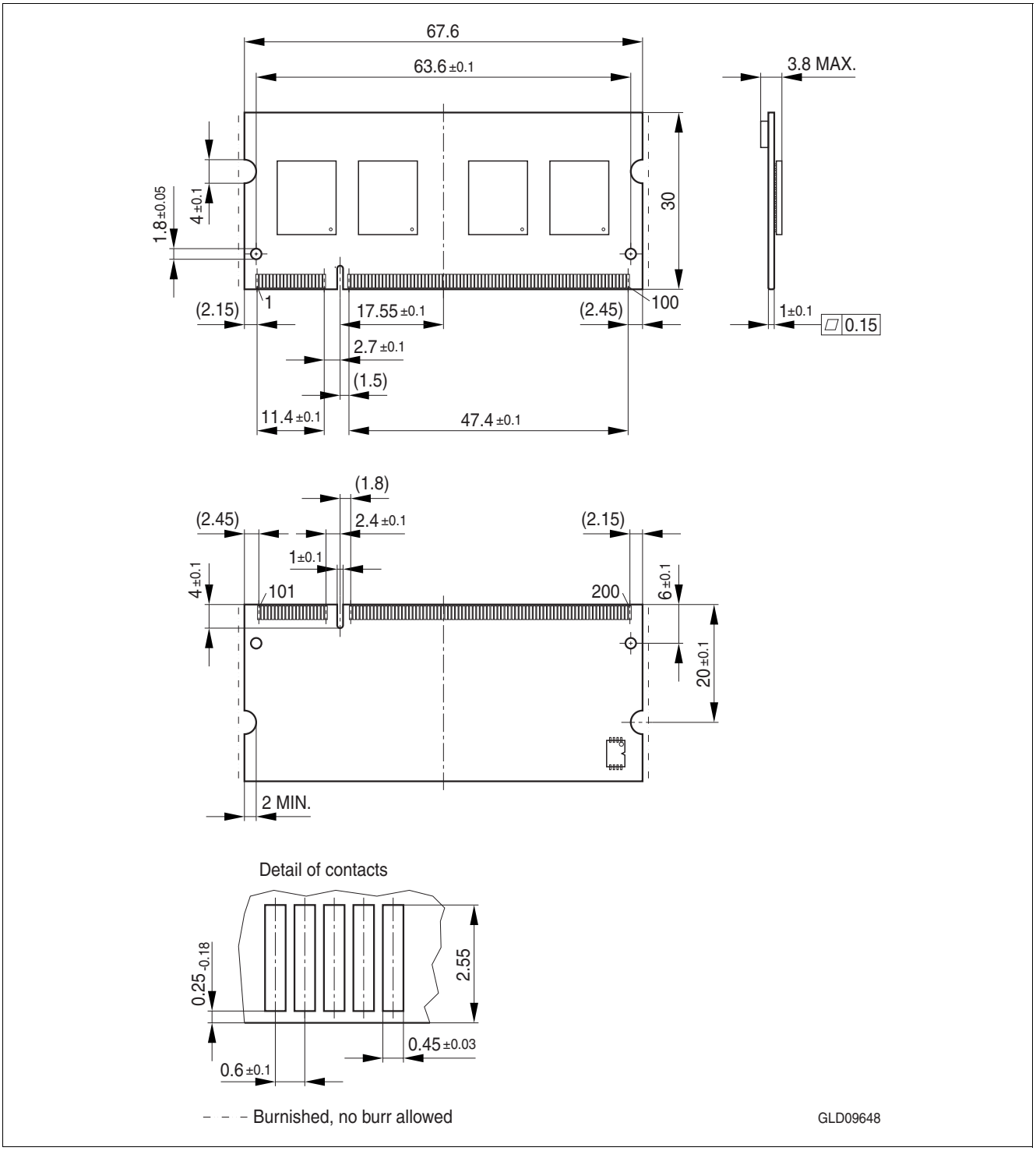

Figure 5 Package Outline L-DIM-200-30

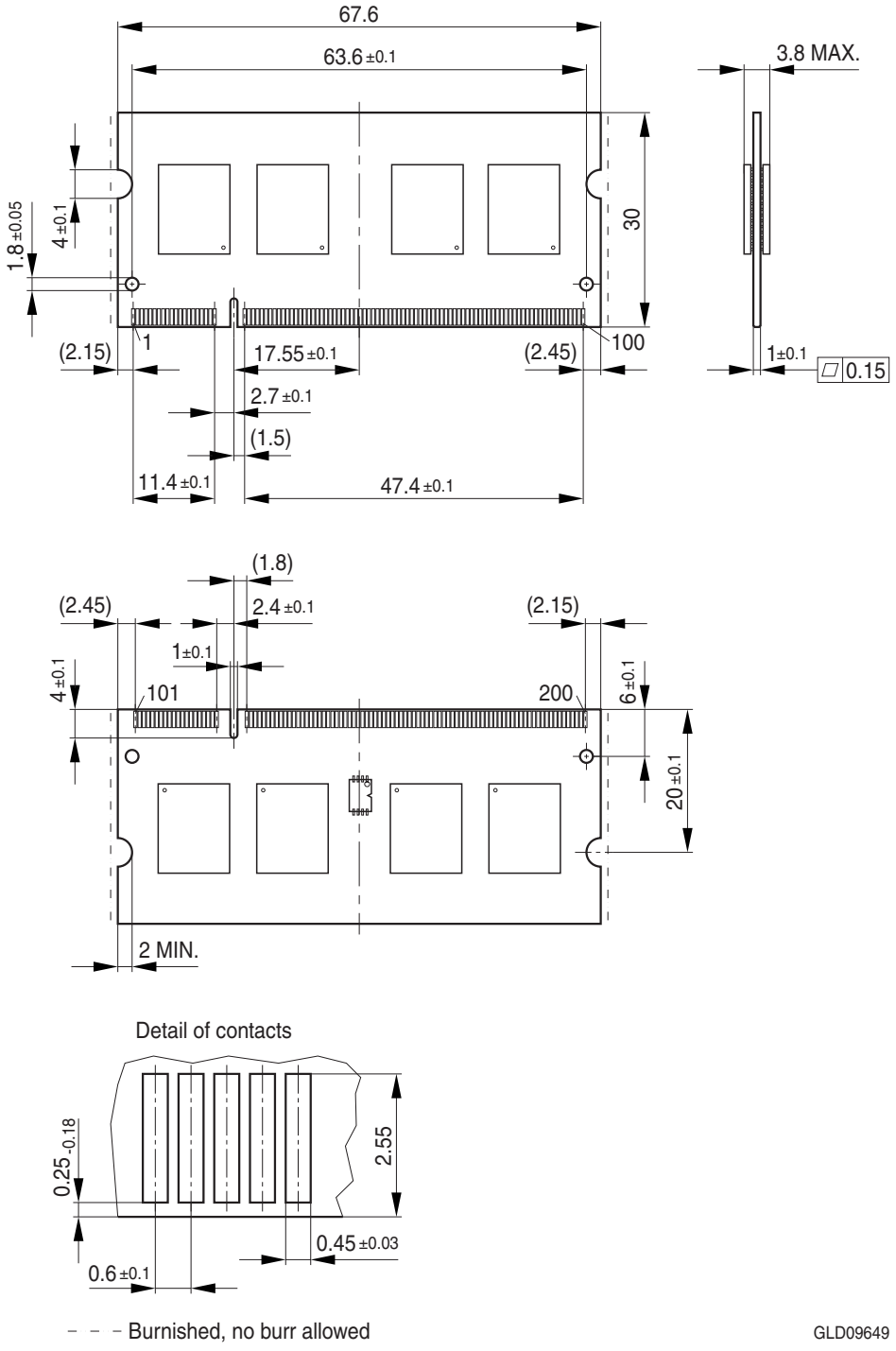

Figure 6 Package Outline L-DIM-200-31

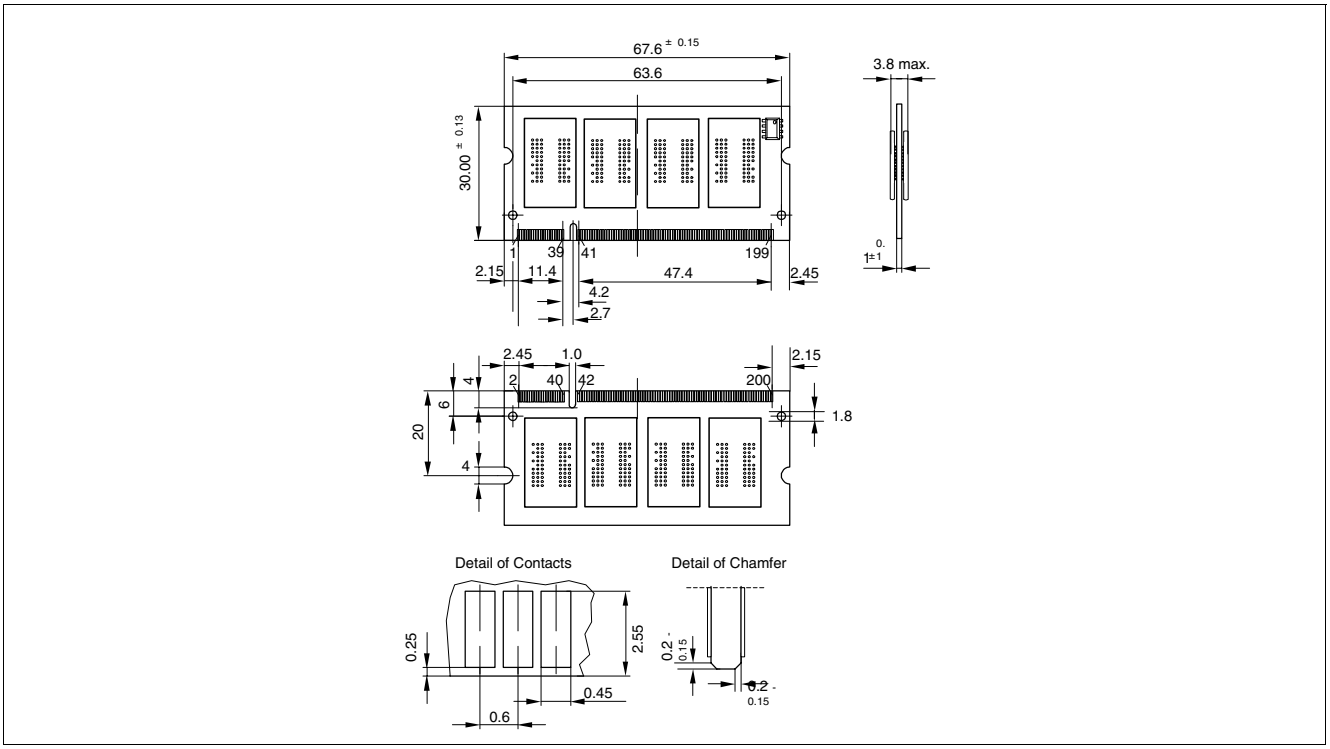

Figure 7 Package Outline L-DIM-200-33

8 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Infineon's nomenclature uses simple coding combined with some propriatory coding. Table 22 provides examples for module and component product type number as well as the field number. The detailed field description together with possible values and coding explanation is listed for modules in Table 23 and for components in Table 24.

Table 22 Nomenclature Fields and Examples

Example for	Field Number										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Micro-DIMM	HYS	64	T	64	0	2	0	K	M	–5	–A
DDR2 DRAM	HYB	18	T	512	16		0	A	C	–5	

Table 23 DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	INFINEON Modul Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density[1)]	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
5	Raw Card Generation	0 .. 9	look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	look up table
8	Package, Lead-Free Status	A .. Z	look up table
9	Module Type	S	**S**O-DIMM
		M	**M**icro-DIMM
		R	**R**egistered
		U	**U**nbuffered
10	Speed Grade	–3.7	PC2–4200 4–4–4
		–5	PC2–3200 3–3–3
11	Die Revision	–A	First
		–B	Second

1) Multiplying "Memory Density per I/O" with "Module Data Width" and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column "Coding".

Table 24 DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	INFINEON Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL1.8
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	–3.7	DDR2-533
		–5	DDR2-400
11	N/A for Components		

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