19-1701; Rev 2; 2/01

MAXIM

2.125Gbps, 3.3V Quad-Port Bypass with Repeater

General Description

The MAX3752 quad-port bypass IC is designed for use in the Fibre Channel Arbitrated Loop topology. This device consists of four serially connected port bypass circuits (PBCs) and a repeater that provides clock and data recovery (CDR).

The quad-port bypass circuit allows connection of up to four Fibre Channel L-Ports, which can each be enabled or bypassed by controlling the PBC select inputs. Additional quad PBCs can be cascaded for applications requiring more than four L-Ports. To reduce the external parts count, all signal inputs and outputs have internal termination resistors.

The MAX3752 complies with Fibre Channel jitter tolerance requirements and can recover data signals with up to 0.7 unit intervals (UIs) of high-frequency jitter. When the repeater is not needed, it can be disabled to reduce power consumption. A fully integrated phase-locked loop (PLL) provides a frequency lock indication and does not need an external reference clock.

Applications

2.125Gbps Fibre Channel

Fibre Channel Data Storage Systems

Storage Area Networks

Fibre Channel Hubs

Typical Operating Circuit appears at end of data sheet.

Features

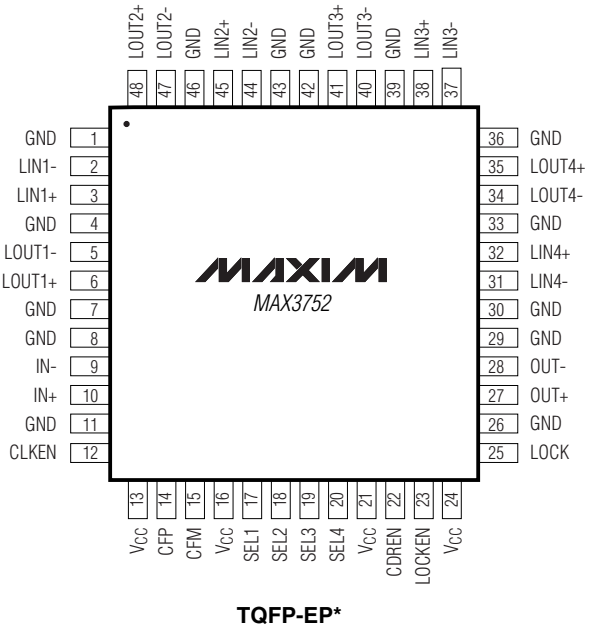
- **Four High-Speed Data Ports**
- **Meets Fibre Channel Jitter Tolerance Requirements**
- **Large Output Signal Swing (>1000mVp-p)**
- **+3.0V to +3.6V Single-Supply Voltage**
- **On-Chip Termination Resistors Compatible with 75Ω Transmission Lines at All Ports**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3752CCM	0°C to +70°C	48 TQFP-EP*

**EP = Exposed pad*

Pin Configuration



TQFP-EP*

** Exposed pad is connected to ground.*

For price, delivery, and to place orders, please contact Maxim Distribution at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.....-0.5V to +5.0V
Current into OUT+, OUT-, LOUT1+, LOUT1-, LOUT2+, LOUT2-, LOUT3+, LOUT3-, LOUT4+, LOUT4- .....0 to 22mA
Voltage at OUT+, OUT-, LOUT1+, LOUT1-, LOUT2+, LOUT2-, LOUT3+, LOUT3-, LOUT4+, LOUT4-..... .....(V_{CC} - 1.65V) to (V_{CC} + 0.5V)
Voltage at IN+, IN-, LIN1+, LIN1-, LIN2+, LIN2-,LIN3+, LIN3-, LIN4+, LIN4-.....-0.5V to (V_{CC} + 0.5V)
Voltage at CLKEN, CFP, CFM, SEL1, SEL2, SEL3, SEL4, CDREN, LOCKEN.....-0.5V to (V_{CC} + 0.5V)
Voltage at LOCK.....-0.5V to (V_{CC} + 0.5V)
Current at LOCK .....-10mA to +1mA
Continuous Power Dissipation (T_A = +70°C)
TQFP-EP (derate 27.0mW/°C above +70°C) 2W
Operating Junction Temperature Range.....-55°C to +150°C
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-50°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C. Typical values are at +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Note 1)	CDR disabled (CLKEN, CDREN, LOCKEN = GND)		195		mA
			193	269	
	CDR enabled (CLKEN, CDREN, LOCKEN = V_{CC})		225		
			255	353	
Input Swing (Differential)	IN±, LINn±	200		2200	mV_{p-p}
Input Common-Mode Voltage			V_{CC} - 0.45		V
Output Voltage Swing (Differential)	150Ω load (OUT±, LOUTn±)	1000	1400	1600	mV_{p-p}
Input Resistance (Differential)	(IN±, LINn±)	132	150	181	Ω
Output Resistance (Differential)	(OUT±, LOUTn±)	132	150	181	Ω
TTL Input Voltage (Low)				0.8	V
TTL Input Voltage (High)		2			V
TTL Input Current	0 ≤ TTL input voltage ≤ V_{CC}	-50		50	µA
Lock Output Voltage (Low)	I_{OL} = +1mA, LOCKEN = HIGH		0.4	0.7	V
Lock Output Voltage (High)	I_{OH} = -100µA, LOCKEN = HIGH	2.4	V_{CC} - 0.4		V
Voltage at CFP, CFM			V_{CC} - 1.03		V

AC ELECTRICAL CHARACTERISTICS—MAX3752 Operating at 2.125Gbps

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +70°C. Typical values are at +3.3V, C_F = 0.22µF, T_A = +25°C, unless otherwise noted.) (Notes 2–7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Rate			2.125 ± 100ppm		Gbps
Output Edge Speed	20% to 80%	75	115	160	ps
Random Jitter at OUT±	Pattern = K28.7+, CDR disabled		1.5		ps_{RMS}
	Pattern = K28.7+, CDR enabled		2.3		
	Pattern = CRPAT, CDR enabled (Note 8)		3.6		
Deterministic Jitter at OUT±	Pattern = K28.5, CDR disabled		39	82	ps_{p-p}
	Pattern = K28.5, CDR enabled		27	47	
	Pattern = FC-RPAT, CDR enabled (Note 8, jitter applied)		52	80	
Total Jitter at OUT±	Pattern = CRPAT, CDR enabled		72		ps_{p-p}
	Pattern = CRPAT, CDR enabled (Note 8, jitter applied)		100		
Jitter Tolerance (BER = 10^{-12})	f = 85kHz sine wave (Notes 8, 9)	1.5	>4.22		UI_{p-p}
	f = 1.27MHz sine wave (Notes 8, 9)	0.1	>0.85		
	f = 10MHz sine wave (Notes 8, 9)	0.1	>0.47		
Deterministic Jitter Tolerance		0.38			UI_{p-p}
Total High-Frequency Jitter Tolerance	BER = 10^{-12} (Note 10)	0.7			UI_{p-p}
CDR Lock Time	Pattern = CJTPAT		4.4		ms
Propagation Delay	IN± to OUT± (ports bypassed, CDR enabled)			10	ns
	LINn± to LOUT(n+1)± (port normal mode)			2	
	SEL(n) rising edge to data valid at LOUT(n+1)± or OUT± (port normal mode)		8		
	SEL(n) falling edge to data valid at LOUT(n+1)± or OUT± (port bypass mode)		8		

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AC ELECTRICAL CHARACTERISTICS (continued)

Note 1: Includes output currents.
Note 2: AC characteristics are guaranteed by design and characterization.
Note 3: K28.7+ Pattern: 0011 1110 00.
Note 4: Fibre Channel Random Pattern in hex (FC-RPAT): 3EB0 5C67 85D3 172C A856 D84B B6A6 65.
Note 5: Compliant Random Pattern in hex (CRPAT):

Pattern Sequence	Repetitions
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
86 BA 6C64 75 D0 E8 DC A8 B4 79 49 EA A6 65	16
72 31 9A 95 AB	1
C1 6A AA 9A A6	1

Note 6: K28.5 Pattern: 0011 1110 1011 0000 0101.
Note 7: Compliant Jitter Tolerance Pattern in Hex (CJTPAT):

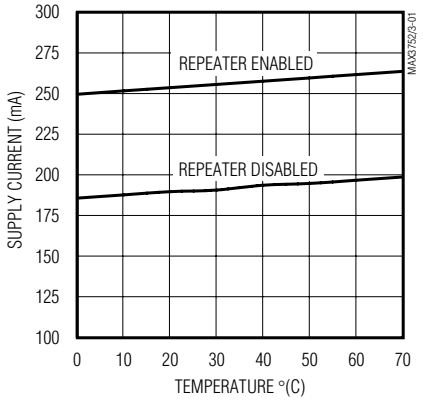
Pattern Sequence	Repetitions
3E AA 2A AA AA	6
3E AA A6 A5 A9	1
87 1E 38 71 E3	41
87 1E 38 70 BC 78 F4 AA AA AA	1
AA AA AA AA AA	12
AA A1 55 55 E3 87 1E 38 71 E1	1
AB 9C 96 86 E6	1
C1 6A AA 9A A6	1

Note 8: Parameter measured with 0.38UI deterministic and 0.22UI random jitter (BER = 10^{-12}) applied to the input.
Note 9: Jitter tolerance measurement exceeds the capability of the test equipment used.
Note 10: Parameter measured with 0.1UI sinusoidal jitter at 10MHz plus 0.38UI deterministic jitter applied to the input.

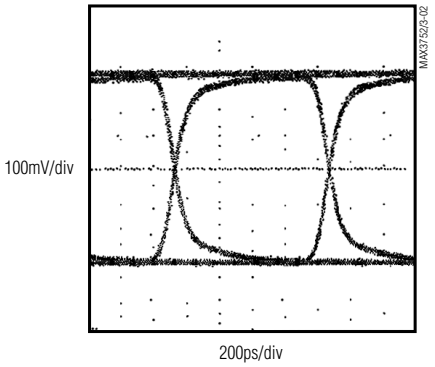
Typical Operating Characteristics

(T_A = +25°C and V_{CC} = +3.3V, unless otherwise noted.)

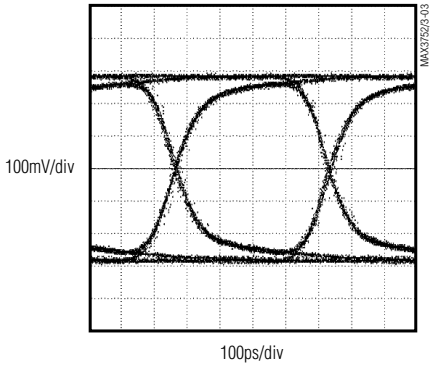
SUPPLY CURRENT vs. TEMPERATURE



DATA OUTPUT EYE DIAGRAM (1.0625Gbps CJTPAT)



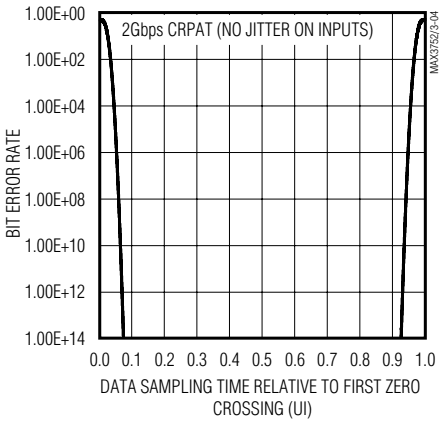
DATA OUTPUT EYE DIAGRAM (2.125Gbps CJTPAT)



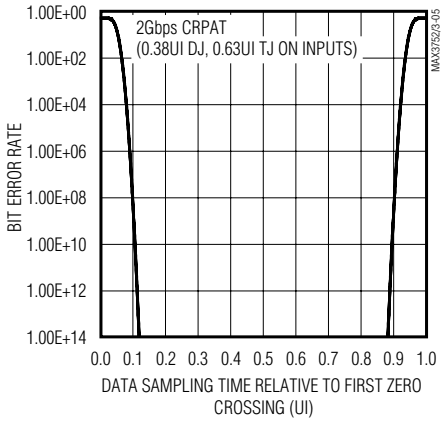
Typical Operating Characteristics (continued)

(T_A = +25°C and V_{CC} = +3.3V, unless otherwise noted.)

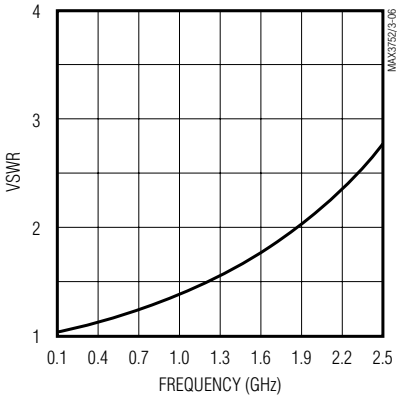
OUTPUT JITTER—BATHTUB PLOT



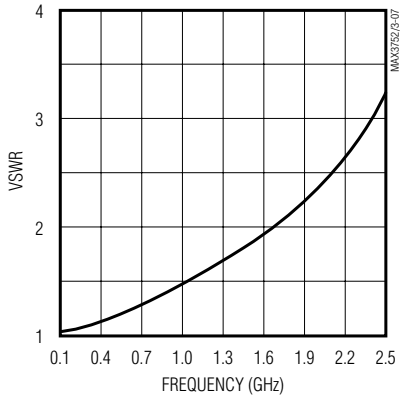
OUTPUT JITTER—BATHTUB PLOT



INPUT VSWR vs. FREQUENCY (BY SIMULATION)



OUTPUT VSWR vs. FREQUENCY (BY SIMULATION)



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Pin Description

PIN	NAME	FUNCTION
1, 4, 7, 8, 11, 26, 29, 30, 33, 36, 39, 42, 43, 46	GND	Electrical Ground
2	LIN1-	Inverted Data Input for L-Port 1
3	LIN1+	Noninverted Data Input for L-Port 1
5	LOUT1-	Inverted Data Output for L-Port 1
6	LOUT1+	Noninverted Data Output for L-Port 1
9	IN-	Inverted Data Input
10	IN+	Noninverted Data Input
12	CLKEN	Clock Enable. A TTL high level enables clock output at L-Port 1.
13,16, 21, 24	V_{CC}	Positive Supply Voltage
14	CFP	CDR Filter Capacitor Positive Connection
15	CFM	CDR Filter Capacitor Negative Connection
17	SEL1	Select 1. A TTL low on SEL1 selects data from IN±. TTL high on SEL1 selects data from LIN1±.
18	SEL2	Select 2. A TTL low on SEL2 selects data from the previous port bypass circuit. A TTL high on SEL2 selects data from LIN2±.
19	SEL3	Select 3. A TTL low on SEL3 selects data from the previous port bypass circuit. A TTL high on SEL3 selects data from LIN3±.
20	SEL4	Select 4. A TTL low on SEL4 selects data from the previous port bypass circuit. A TTL high on SEL4 selects data from LIN4±.
22	CDREN	CDR Enable Input (TTL). A high input enables the CDR for data recovery. A low input disables the CDR (no data recovery).
23	LOCKEN	Lock Enable Input (TTL). A high input enables the LOCK output. A low input disables the LOCK output.
25	LOCK	CDR Lock Output. Enabled by LOCKEN. A high output indicates the CDR PLL is locked. When LOCKEN is low, LOCK is high.
27	OUT+	Noninverted Data Output
28	OUT-	Inverted Data Output
31	LIN4-	Inverted Data Input for L-Port 4
32	LIN4+	Noninverted Data Input for L-Port 4
34	LOUT4-	Inverted Data Output for L-Port 4
35	LOUT4+	Noninverted Data Output for L-Port 4
37	LIN3-	Inverted Data Input for L-Port 3
38	LIN3+	Noninverted Data Input for L-Port 3
40	LOUT3-	Inverted Data Output for L-Port 3
41	LOUT3+	Noninverted Data Output for L-Port 3
44	LIN2-	Inverted Data Input for L-Port 2
45	LIN2+	Noninverted Data Input for L-Port 2
47	LOUT2-	Inverted Data Output for L-Port 2
48	LOUT2+	Noninverted Data Output for L-Port 2
EP	Exposed Pad	Ground. The exposed pad must be soldered to the circuit board for proper thermal performance.

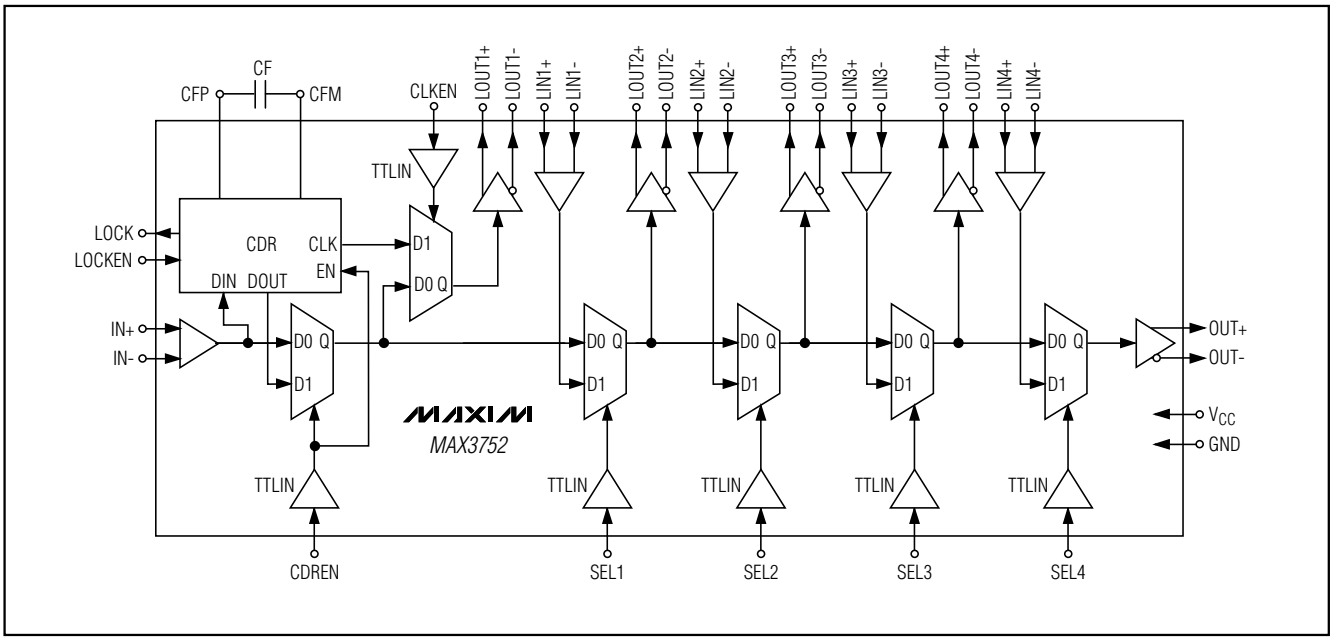


Figure 1. Functional Diagram

Detailed Description

The MAX3752 quad PBC consists of an input buffer, a clock/data recovery circuit (for optional data recovery), four serially connected port bypass circuits, and an output buffer (Figure 1). The circuit design is optimized for both high-speed (2Gbps) and low-voltage (+3.3V) operation.

Input Buffer

The input buffer provides line termination and level conversion. It accepts a differential input voltage of 200mV to 2200mV at the IN+ and IN- pins. Internal resistors terminate each input to 75Ω (150Ω total between the two inputs), eliminating the need for external termination resistors in most applications (see *Applications Information* for a suggested interface to 50Ω systems).

Clock and Data Recovery

The purpose of the clock and data recovery (CDR) is to improve jitter transfer performance by attenuating jitter that may be present in the input data. The CDR can recover data signals that are corrupted by up to 0.7UI of high-frequency jitter (BER = 10^{-12}). When data recovery is not needed, the CDR may be disabled in order to save power.

The input buffer drives the CDR circuit, as well as one input of a 2:1 multiplexer. A TTL high on the CDR enable pin (CDREN) enables the CDR and connects the CDR data output to the port bypass circuits. The recovered clock signal is available for test purposes at LOUT1 (the output of the first port bypass circuit) when the clock enable input (CLKEN) is set to a TTL high level. A TTL low on CDREN disables the CDR and connects the input buffer output directly to the port bypass circuits.

Port Bypass Circuits

The output of the 2:1 input multiplexer drives a cascaded series of four PBCs. Each PBC consists of a differential output buffer, a differential input buffer, and a 2:1 multiplexer. The multiplexer select input (SELn) controls which multiplexer input is connected to the multiplexer output. A TTL low on the multiplexer select pin causes the data signal from the previous stage to be connected to the multiplexer output (port bypass mode). A TTL high on the multiplexer select pin causes the data signal from the input buffer to be connected to the multiplexer output (port enable mode). The output of the last PBC drives the output buffer.

Output Buffer

The output signal of the last PBC drives the differential high-power output buffer. The output buffer drives the output port (OUT±). Internal resistors terminate each output to 75Ω (150Ω total between the two outputs), eliminating the need for external termination resistors in most applications (see *Applications Information* for a suggested interface to 50Ω systems). The output buffer produces a differential output voltage of 1000mV to 1600mV when driving a differential 150Ω load.

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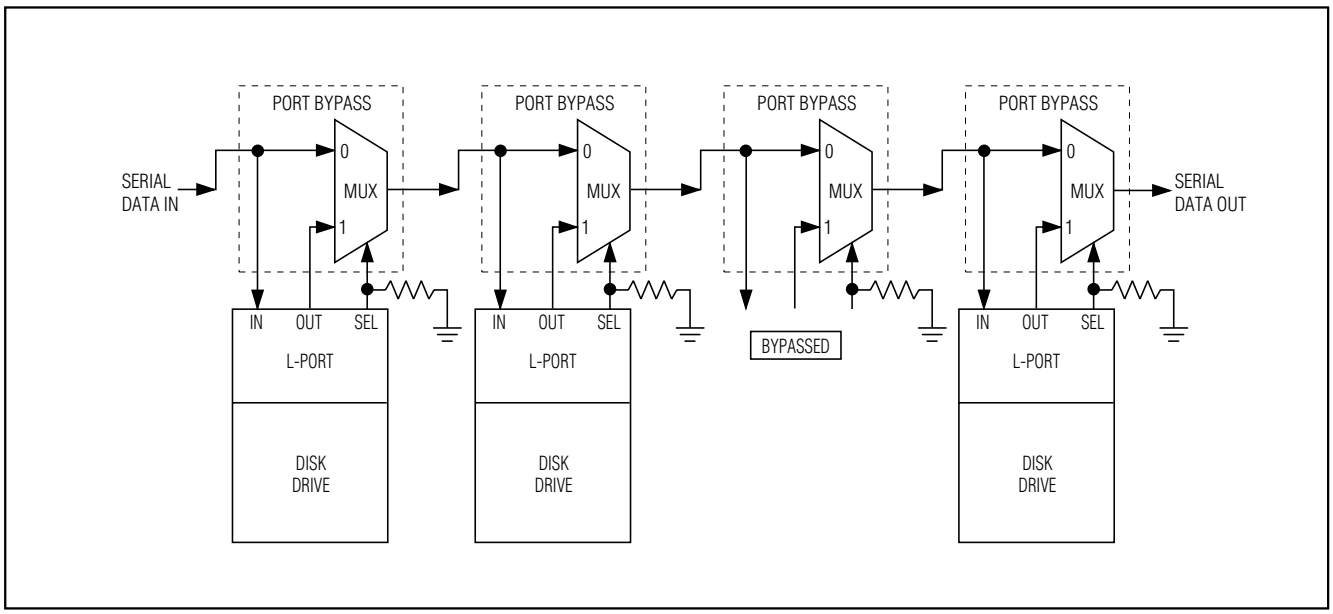


Figure 2. Disk Array Implemented with Port Bypass Circuits

Applications Information

The MAX3752 quad-port bypass circuit is designed for hard disk array applications of the Fibre Channel Arbitrated Loop network protocol.

A drive array is a collection of hard disk drives (called physical drives) that are connected together. The total storage capacity of the array of physical drives can be divided into one or more subsets (called logical drives) that may be spread over all of the physical drives in the array. For example, a computer accessing the drive array might "see" it as two logical drives (D: and E:, for example) that each have a storage capacity of 20GB, even though the actual array is made up of eight physical 5GB drives.

In applications where data storage reliability is critical, it may be desirable to create a disk array where the data is stored redundantly on more than one physical drive. This type of system is generally called a redundant array of inexpensive disks (RAIDs). If a physical drive fails, it may be replaced and the lost data can be restored.

Drive arrays are also useful in applications that require fast access to stored data. The data may be distributed over physical drives connected in a parallel arrangement, enabling access to data concurrently from multiple drives in the array. This makes it possible to achieve I/O rates much greater than what is feasible with nonarrayed drives.

The Fibre Channel Arbitrated Loop protocol enables multiple physical drives to be connected in a loop topology. Each physical drive is connected to the Fibre Channel loop through an L-Port that may be individually addressed and controlled to create the array of logical drives. Data is transmitted over the loop as an encoded serial bit stream. Using the Fibre Channel Arbitrated Loop protocol, the configuration of the disk array can be rearranged under software control to achieve desired objectives (such as data reliability or fast access).

The port bypass circuit allows any L-Port to be enabled (connected to the network) or bypassed (disconnected from the network) while the network is operating. This enables hot swapping of physical drives (inserting or removing physical drives while the network is operating) so that drives may be replaced with minimal disruption to the disk array system. Figure 2 shows the disk array.

Input/Output Structures

Figures 3 and 4 show models for the MAX3752 inputs and outputs.

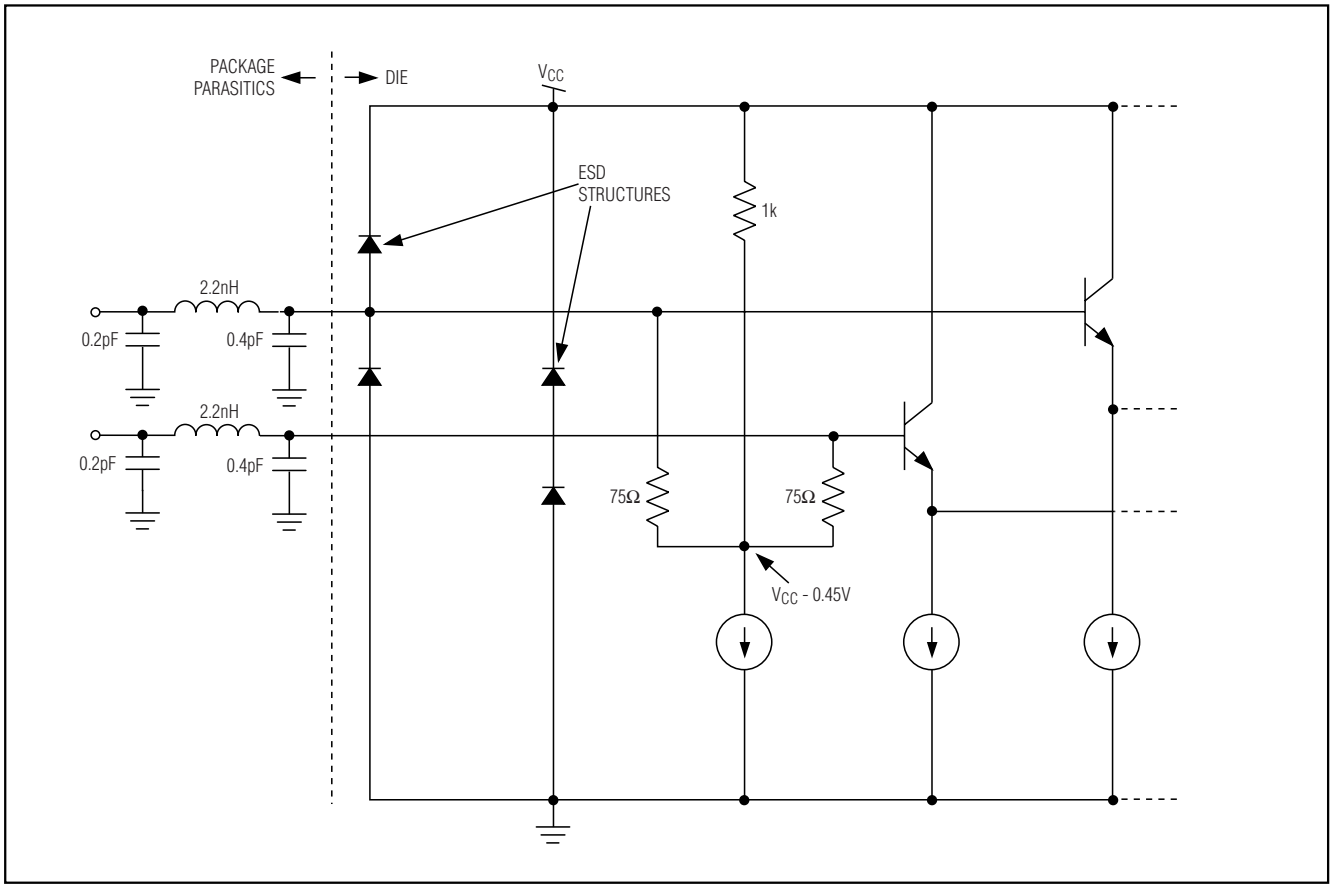


Figure 3. MAX3752 Input Structure

Cascading Port Bypass Circuits

Two or more MAX3752 quad PBCs can be cascaded by directly connecting the OUT+ and OUT- pins of one quad PBC to the IN+ and IN- pins of the next quad PBC. See *Typical Operating Circuit.*

Interfacing to 50Ω Systems

Figure 5 shows examples of resistive impedance transforming networks that can be used to interface between the 75Ω input/output structure of the MAX3752 and 50Ω systems. The characteristics of the two examples shown can be derived by referring to Figures 3, 4, and 5. The top configuration in Figure 5 is useful in designs where the parallel 300Ω resistors can be placed very close to the input/output pins of the IC. In this case, the 50Ω transmission lines should connect directly to the IC.

The bottom configuration in Figure 5 provides a better impedance match than the top configuration for designs where 75Ω transmission lines are connected between the input/output pins of the IC and the resistive impedance transforming networks.

Neither of the two configurations in Figure 5 provides 100% efficient voltage coupling. In the top configuration, the input voltage (V_{IN}) is the same as the source voltage (V_{SRC}), but the output/load voltage (V_{OUT} = V_{LOAD} for this case) is reduced by a factor of 0.67 because the output is loaded with an equivalent of 75Ω. (The data sheet specification for output voltage swing is based on a 150Ω load.) In the bottom configuration, V_{IN} is attenuated by a factor of 0.64 from V_{SRC}, and V_{LOAD} is attenuated by a factor of 0.43 from V_{OUT}.

For example, a source voltage of 625mV will result in an input voltage of 625mV for the top configuration, but only 400mV for the bottom configuration. Also, a typical output voltage swing of 1400mV into a differential 150Ω load will cause the corresponding load voltage to be

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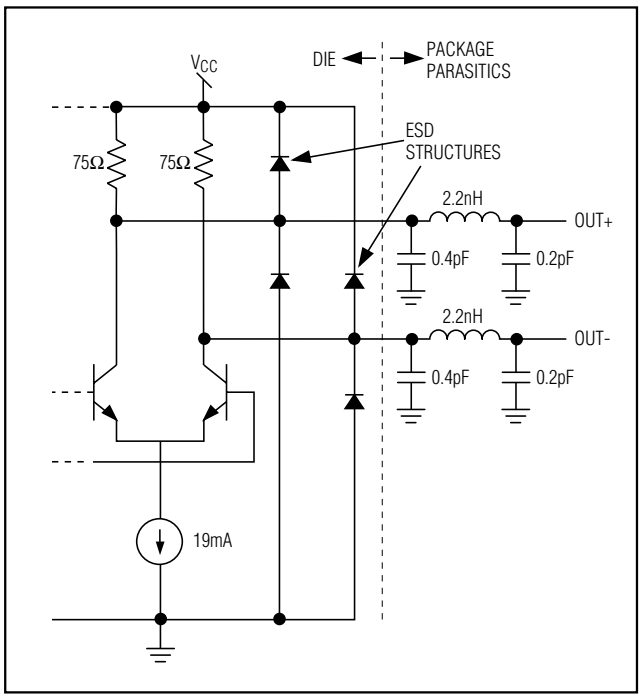


Figure 4. MAX3752 Output Structure

940mV for the top configuration and 600mV for the bottom configuration.

Layout Considerations

For best performance, carefully lay out the PC board using high-frequency techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled impedance transmission lines to interface with the MAX3752 high-speed inputs and outputs. Power-supply decoupling capacitors should be placed very close to V_{CC} pins. Isolate the input signals from the output signals as much as possible.

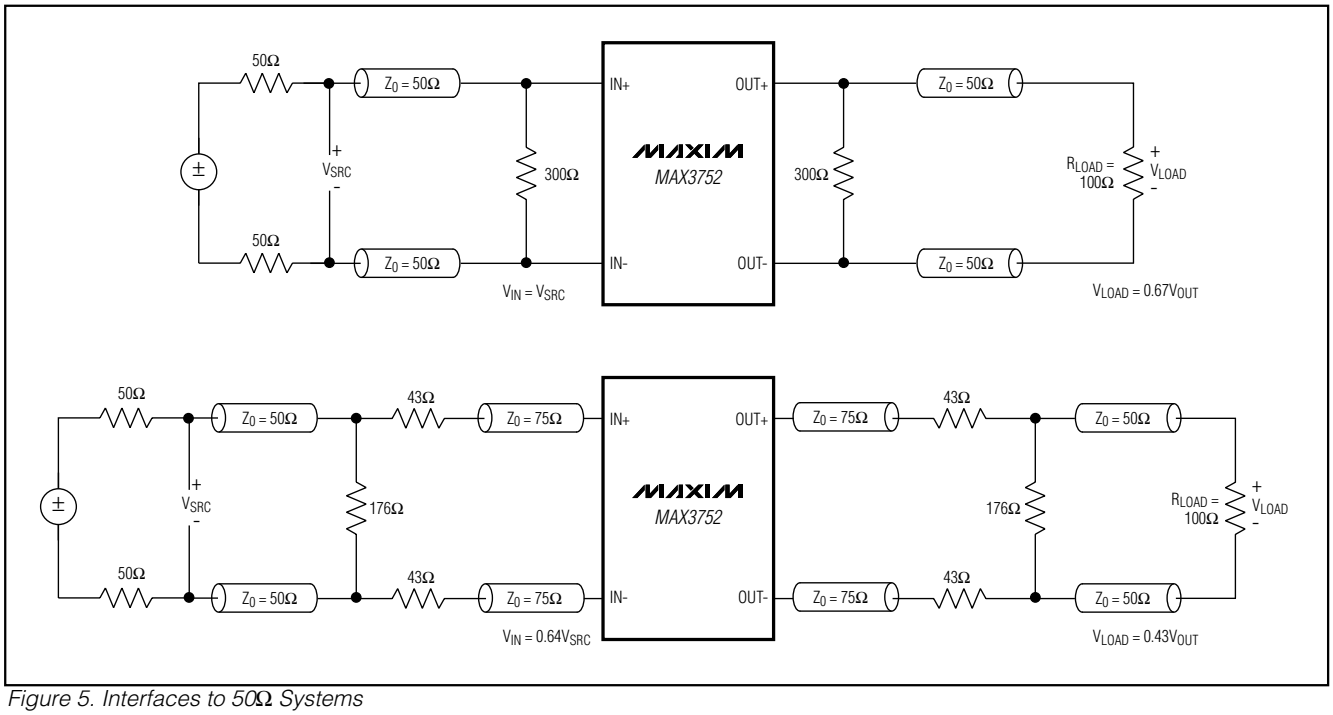
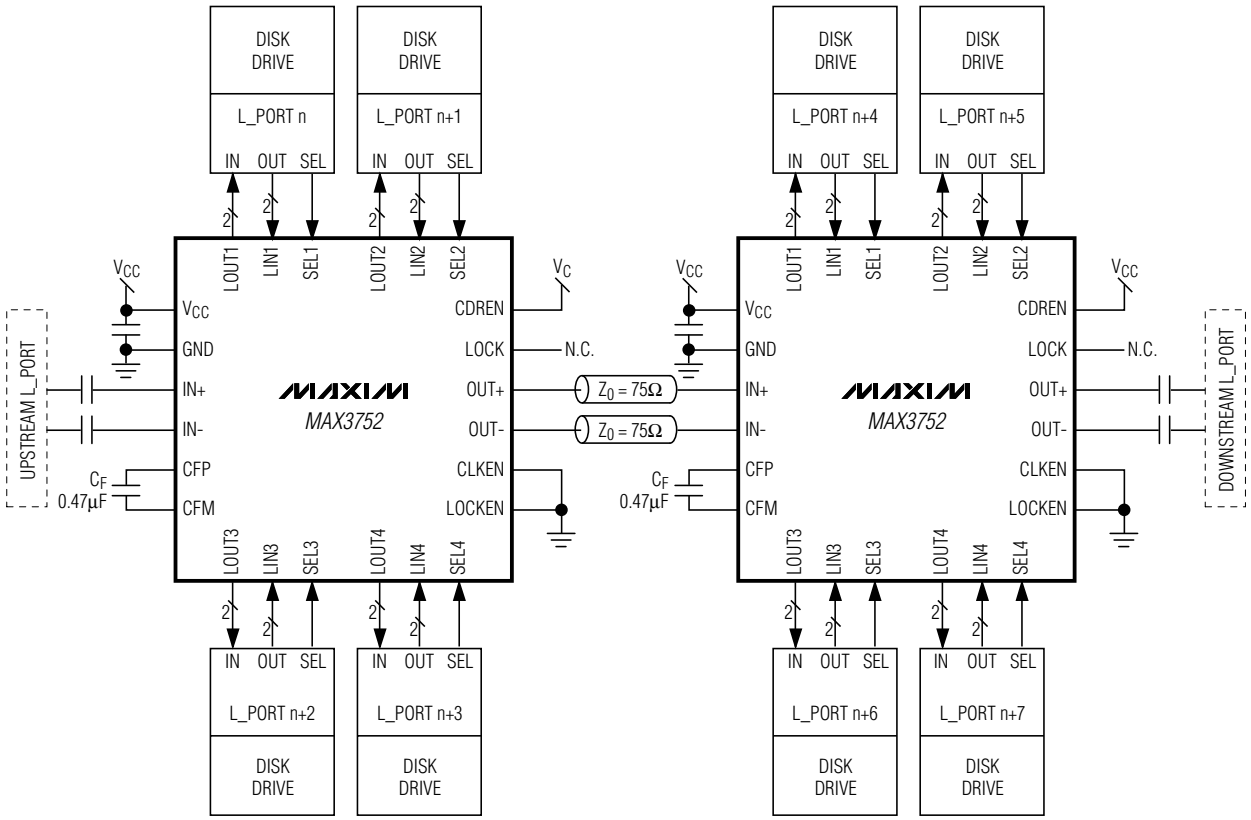


Figure 5. Interfaces to 50Ω Systems

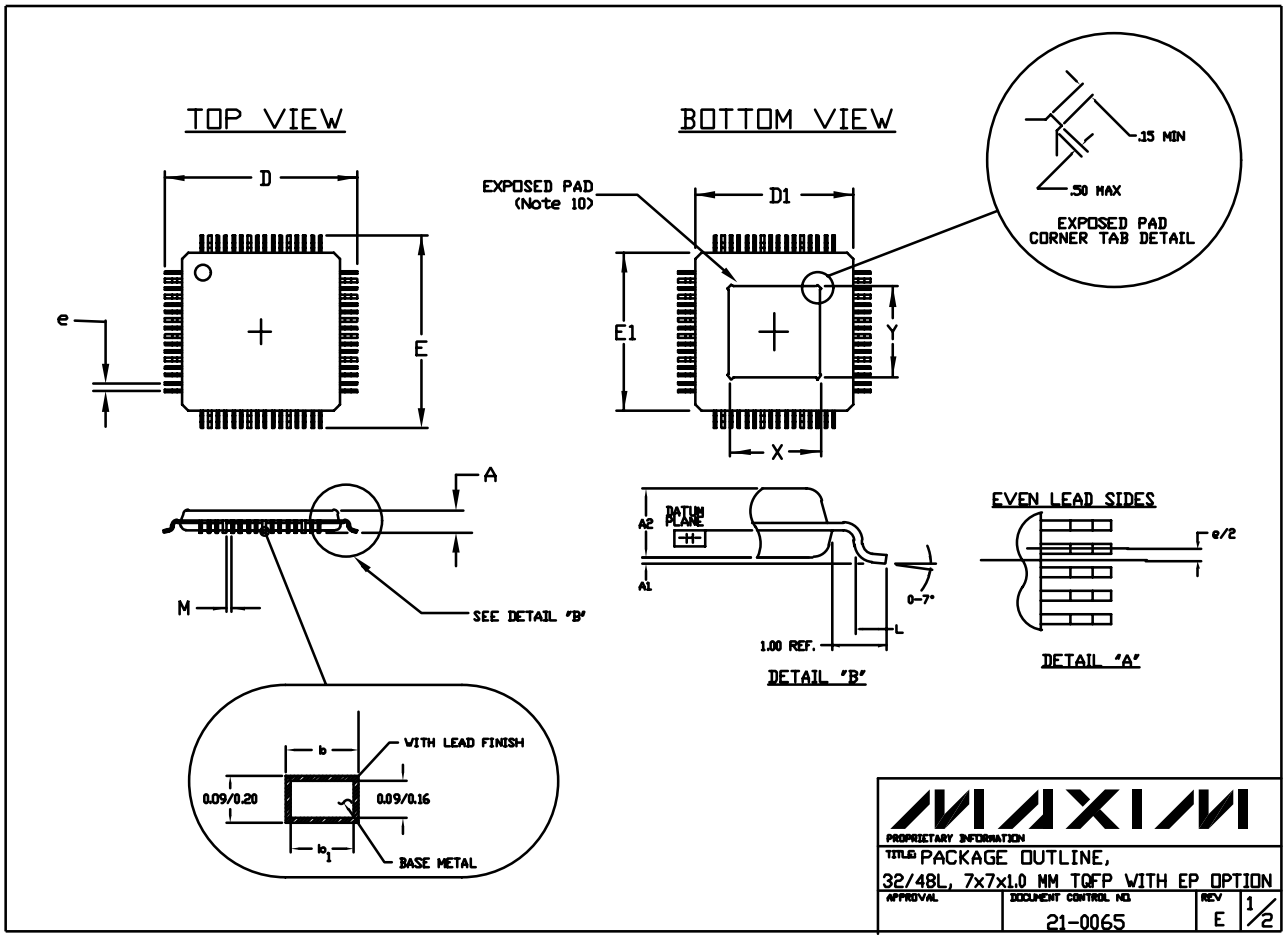
Typical Operating Circuit



NOTE: ALL HIGH-SPEED INPUTS AND OUTPUTS (IN±, OUT±, LIN±, AND LOUT±) SHOULD BE CONNECTED USING CONTROLLED IMPEDANCE TRANSMISSION LINES. AC-COUPLING MAY ALSO BE REQUIRED. ALL CAPACITORS ARE 0.1µF UNLESS OTHERWISE INDICATED.

2.125Gbps, 3.3V Quad-Port Bypass with Repeater

Package Information



48L, TQFP.EPS

Package Information (continued)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	1.20
A_1	0.05	0.10	0.15	0.05	0.10	0.15
A_2	0.95	1.00	1.05	0.95	1.00	1.05
D		9.00 BSC.			9.00 BSC.	
D_1		7.00 BSC.			7.00 BSC.	
E		9.00 BSC.			9.00 BSC.	
E_1		7.00 BSC.			7.00 BSC.	
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15	—	—	0.14	—	—
N		32			48	
e		0.80 BSC.			0.50 BSC.	
b	0.30	0.37	0.45	0.17	0.22	0.27
b1	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD (Note 10)

MAXIM — PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.0 MM TQFP WITH EP OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0065	E	2/2

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