TPS3701 用于过压和欠压检测且具有内部基准电压的 36V 窗口比较器

1 特性

- 宽电源电压范围：1.8V 至 36V
- 可调节阀值：低至 400mV
- 针对过压和欠压检测的开漏输出
- 低静态电流：7μA（典型值）
- 高阈值精度：
  - 0.75%（整个温度范围内）
  - 0.25%（典型值）
- 内部滞后：5.5mV（典型值）
- 温度范围：-40°C 至 125°C
- 封装：
  - 小外形尺寸晶体管 (SOT)-6 封装

2 应用

- 工业控制系统
- 嵌入式计算模块
- 数字信号处理器 (DSP)、微控制器和微处理器
- 笔记本和台式计算机
- 便携式和电池供电类产品
- 现场可编程门阵列 (FPGA) 和专用集成电路 (ASIC) 系统

3 说明

TPS3701 宽电源电压窗口比较器工作电压范围为 1.8V 至 36V。 此器件具有两个内部基准电压为 400mV 的精密比较器和两个额定电压为 25V 的开漏输出（OUTA 和 OUTB），分别用于过压和欠压检测。TPS3701 可用作窗口比较器或两个独立的电压监视器；用外部电阻器设置监视电压。

当 INA 引脚的电压降至负向阈值以下时，OUTA 被驱动为低电平；当 INA 引脚的电压升至正向阈值以上时，OUTA 被驱动为高电平。 当 INB 引脚的电压升至正向阈值以上时，OUTB 被驱动为低电平；而 INB 引脚的电压降至负向阈值以下时，OUTB 被驱动为高电平。 TPS3701 的两个比较器均内置有滞后特性，可抑制噪声，避免触发错误，从而确保运行输出稳定。

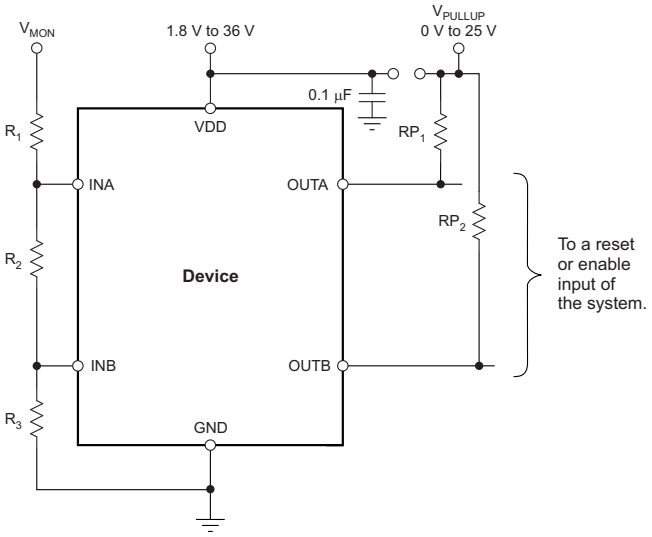
TPS3701 采用 SOT-6 封装，额定工作结温范围为 –40°C 至 125°C。

器件信息(1)

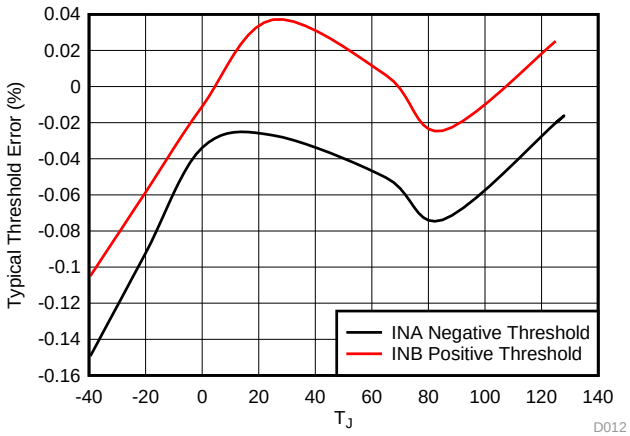
部件号	封装	封装尺寸（标称值）
TPS3701	SOT (6)	2.90mm x 1.60mm

(1) 要了解所有可用封装，请见数据表末尾的封装选项附录。

典型应用



典型误差与结温之间的关系



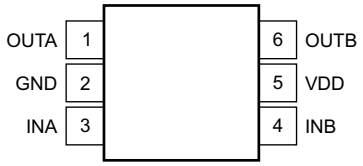
目录

4 修订历史记录

日期	修订版本	注释
2014 年 11 月	*	最初发布版本

5 Pin Configuration and Functions

DDC Package
SOT-6
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
INA	3	I	Comparator A input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage $V_{IT–(INA)}$, OUTA is driven low.
INB	4	I	Comparator B input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage $V_{IT+(INB)}$, OUTB is driven low.
OUTA	1	O	INA comparator open-drain output. OUTA is driven low when the voltage at this comparator is less than $V_{IT–(INA)}$. The output goes high when the sense voltage rises above $V_{IT+(INA)}$.
OUTB	6	O	INB comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+(INB)}$. The output goes high when the sense voltage falls below $V_{IT–(INB)}$.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating junction temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	V_{DD}	–0.3	+40	V
	V_{OUTA}, V_{OUTB}	–0.3	+28	V
	V_{INA}, V_{INB}	–0.3	+7	V
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	+125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	+2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	+500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{INA}, V_{INB}	Input pin voltage	0		1.7	V
V_{OUTA}, V_{OUTB}	Output pin voltage	0		25	V
I_{OUTA}, I_{OUTB}	Output pin current	0		10	mA
T_J	Junction temperature	–40	+25	+125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS3701 DDC (SOT) 6 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	50.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V ≤ V_{DD} < 36 V, and pullup resistors $RP_{1,2}$ = 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		36	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} ≤ 0.2 V			0.8	V
$V_{IT–(INA)}$	INA pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{IT+(INA)}$	INA pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	400	405.5	413	mV
$V_{HYS(INA)}$	INA pin hysteresis voltage ($HYS = V_{IT+(INA)} – V_{IT–(INA)}$)		2	5.5	12	mV
$V_{IT–(INB)}$	INB pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	387	394.5	400	mV
$V_{IT+(INB)}$	INB pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{HYS(INB)}$	INB pin hysteresis voltage ($HYS = V_{IT+(INB)} – V_{IT–(INB)}$)		2	5.2	12	mV
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, I_{OUT} = 3 mA		130	250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA		150	250	mV
I_{IN}	Input current (at INA, INB pins)	V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 6.5 V	–25	+1	+25	nA
		V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 0.1 V	–15	+1	+15	nA
$I_{D(leak)}$	Open-drain output leakage current	V_{DD} = 1.8 V and 36 V, V_{OUT} = 25 V		10	300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V – 36 V		8	11	µA
UVLO	Undervoltage lockout(2)	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. If less than $V_{(POR)}$, the output is undetermined.
(2) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined if less than $V_{(POR)}$.

6.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		9.9		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		28.1		µs
$t_{d(start)}$(2)	Startup delay	V_{DD} = 5 V		155		µs
t_r	Output rise time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.1 to 0.9) × V_{DD}		2.7		µs
t_f	Output fall time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.9 to 0.1) × V_{DD}		0.12		µs

(1) High-to-low and low-to-high refers to the transition at the input pins (INA and INB).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs (typ) before the output state reflects the input condition.

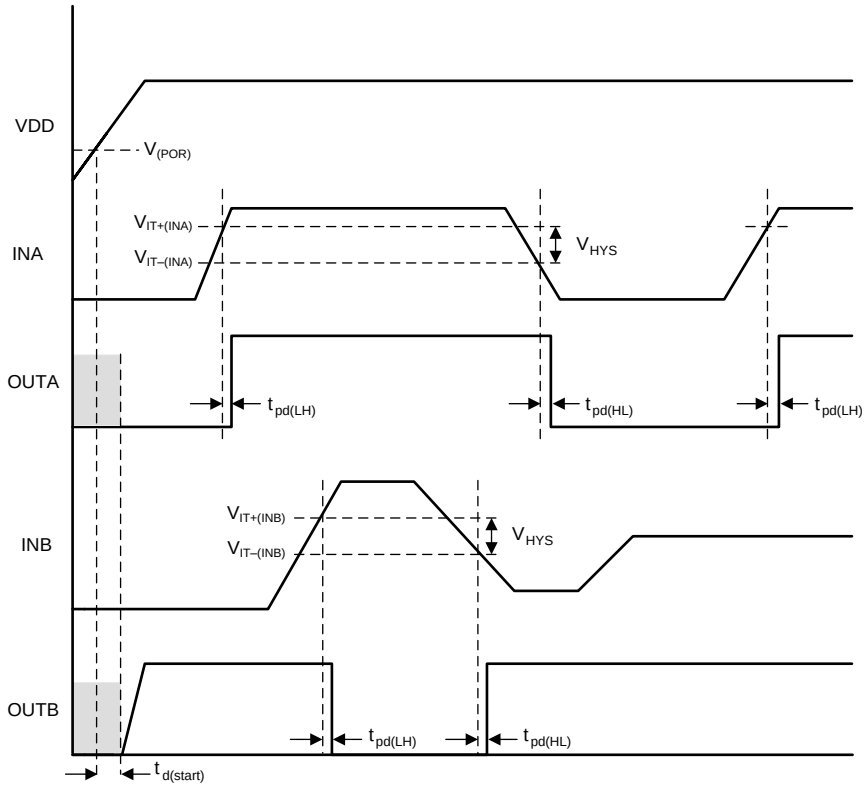


图 1. Timing Diagram

6.7 Typical Characteristics

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

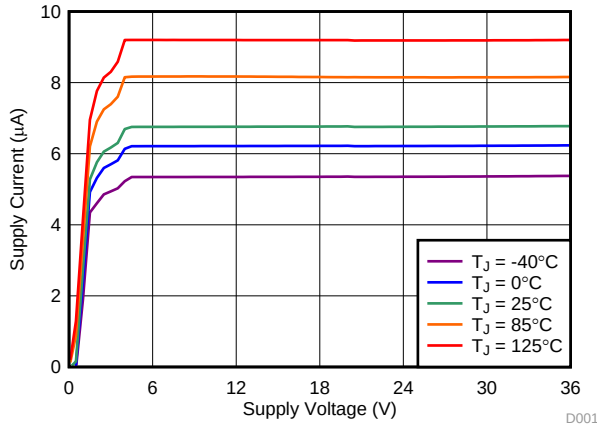
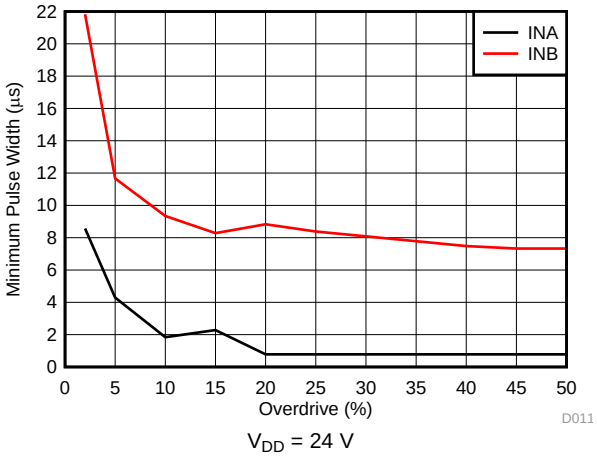


图 2. Supply Current vs Supply Voltage



V_{DD} = 24 V

图 3. Minimum Pulse Duration vs Threshold Overdrive Voltage (1)

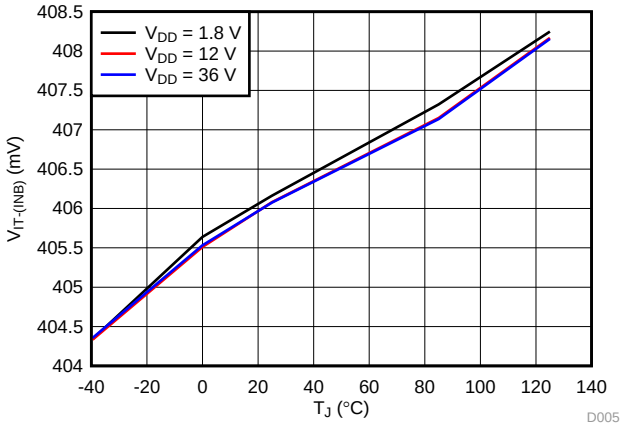


图 4. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) vs Temperature

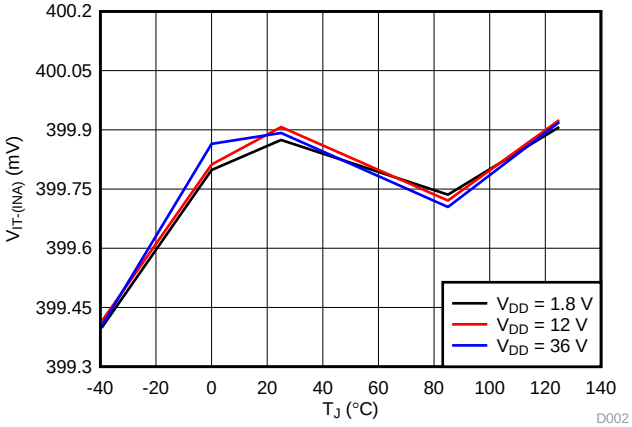


图 5. INA Negative Input Threshold Voltage ($V_{IT-(INA)}$) vs Temperature

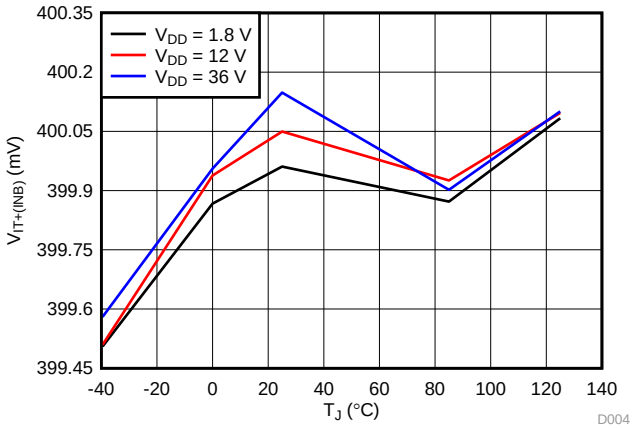


图 6. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) vs Temperature

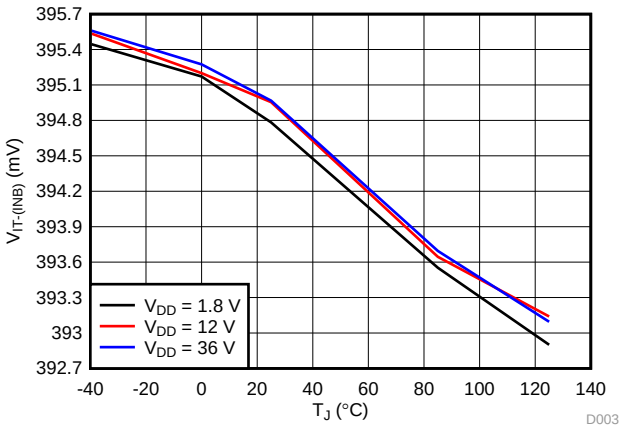


图 7. INB Negative Input Threshold Voltage ($V_{IT-(INB)}$) vs Temperature

(1) Minimum pulse duration required to trigger output high-to-low transition. INA = negative spike below V_{IT-} and INB = positive spike above V_{IT+}.

Typical Characteristics (接下页)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

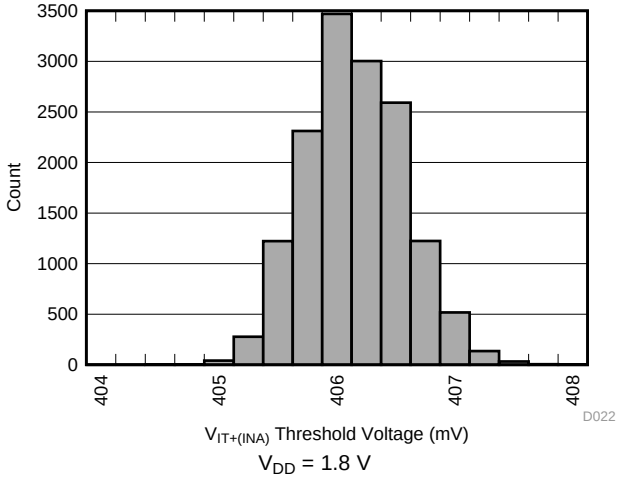


图 8. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) Distribution

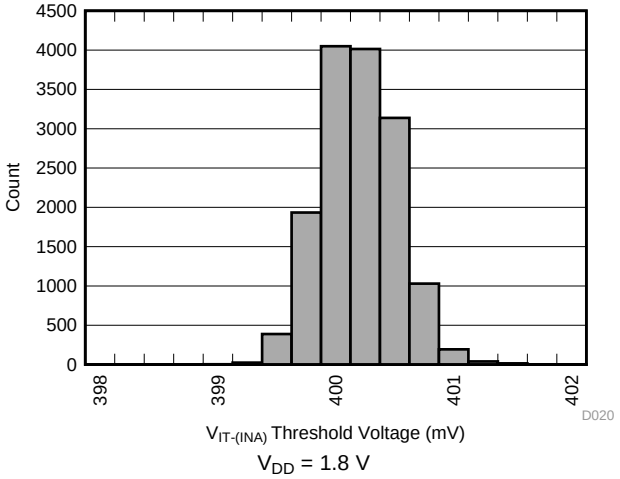


图 9. INA Negative Input Threshold Voltage ($V_{IT–(INA)}$) Distribution

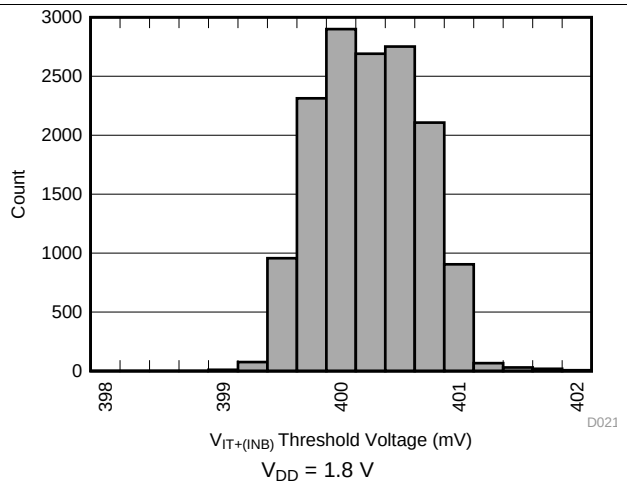


图 10. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) Distribution

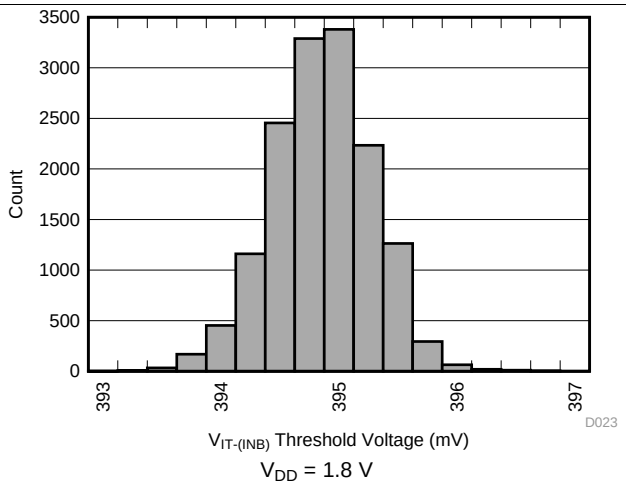


图 11. INB Negative Input Threshold Voltage ($V_{IT–(INB)}$) Distribution

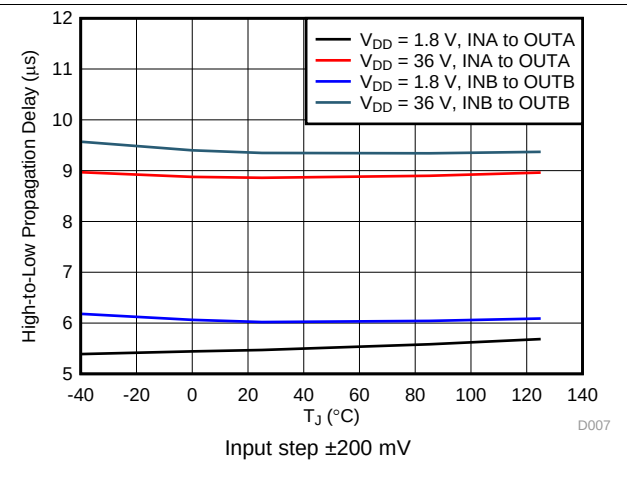


图 12. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

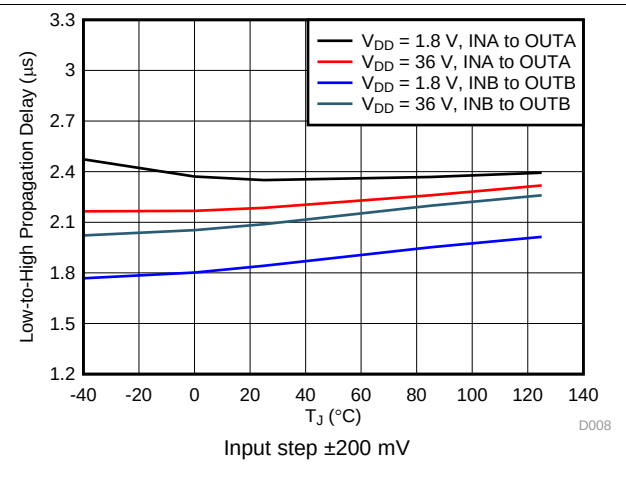
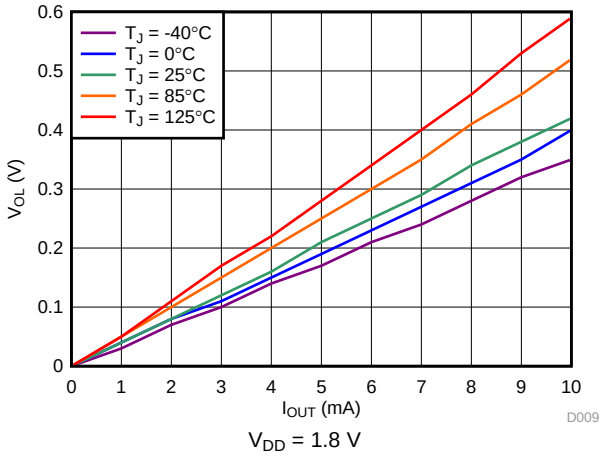


图 13. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

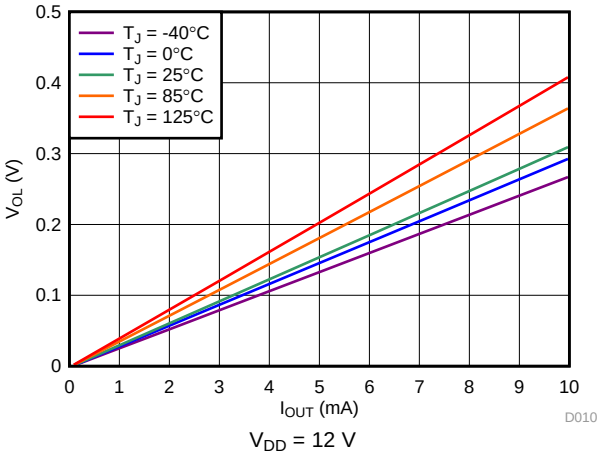
Typical Characteristics (接下页)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.



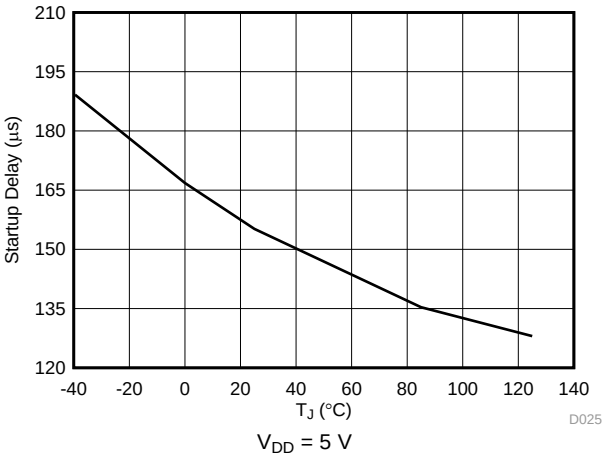
V_{DD} = 1.8 V

图 14. Output Voltage Low vs Output Sink Current



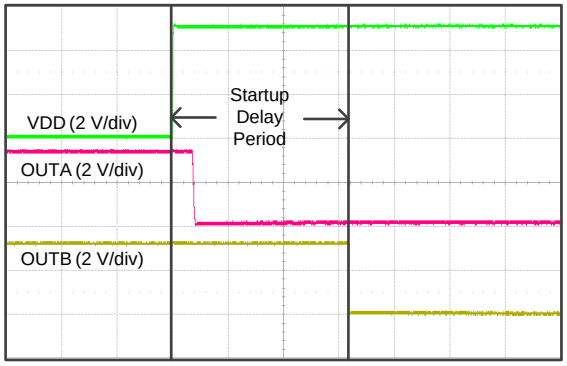
V_{DD} = 12 V

图 15. Output Voltage Low vs Output Sink Current



V_{DD} = 5 V

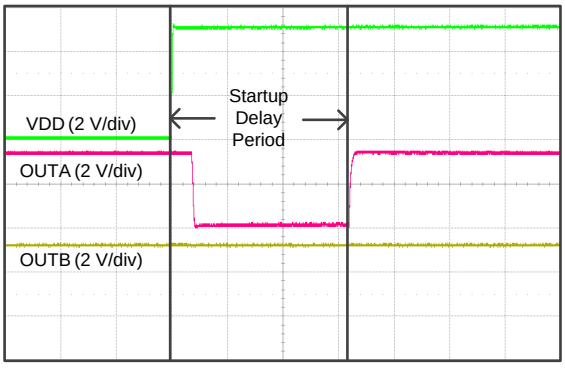
图 16. Startup Delay vs Temperature



Time (50 µs/div)

V_{DD} = 5 V, V_{INA} = 390 mV, V_{INB} = 410 mV, V_{PULLUP} = 3.3 V

图 17. Startup Delay



Time (50 µs/div)

V_{DD} = 5 V, V_{INA} = 410 mV, V_{INB} = 390 mV, V_{PULLUP} = 3.3 V

图 18. Startup Delay

7 Detailed Description

7.1 Overview

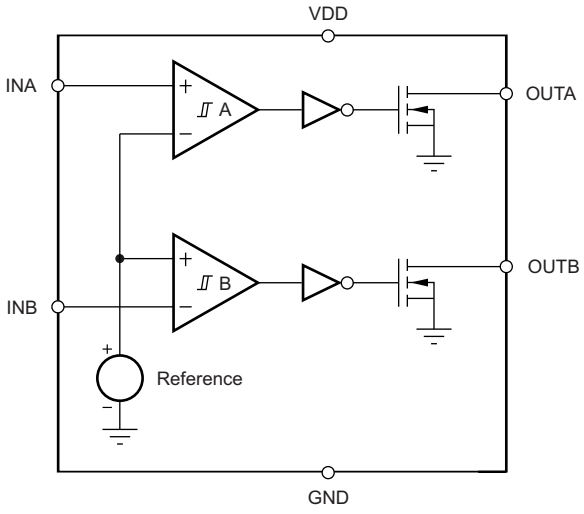
The TPS3701 combines two comparators (referred to as A and B) and a precision reference for over- and undervoltage detection. The TPS3701 features a wide supply voltage range (1.8 V to 36 V) and high-accuracy window threshold voltages of 400 mV (0.75% over temperature) with built-in hysteresis. The outputs are rated to 25 V and can sink up to 10 mA.

Set each input pin (INA, INB) to monitor any voltage above 0.4 V by using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. To form a window comparator, use the two input pins and three resistors (see the *Window Comparator Considerations* section). In this configuration, the TPS3701 is designed to assert the output signals when the monitored voltage is within the window band. Each input can also be used independently. The relationship between the inputs and the outputs is shown in 表 1. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

表 1. Truth Table

CONDITION	OUTPUT	STATUS
INA > $V_{IT+(INA)}$	OUTA high	Output A high impedance
INA < $V_{IT–(INA)}$	OUTA low	Output A asserted
INB > $V_{IT+(INB)}$	OUTB low	Output B asserted
INB < $V_{IT–(INB)}$	OUTB high	Output B asserted

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inputs (INA, INB)

The TPS3701 combines two comparators with a precision reference voltage. Each comparator has one external input; the other input is connected to the internal reference. The rising threshold on INB and the falling threshold on INA are designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy when used as a window comparator. Both comparators also have built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator inputs swings from ground to 1.7 V (7.0 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications in order to reduce sensitivity to transient voltage changes on the monitored signal.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA voltage drops below $V_{IT-(INA)}$. When the voltage exceeds $V_{IT+(INA)}$, OUTA goes to a high-impedance state; see 图 1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB exceeds $V_{IT+(INB)}$. When the voltage drops below $V_{IT-(INB)}$ OUTB goes to a high-impedance state; see 图 1. Together, these two comparators form a window-detection function as described in the *Window Comparator Considerations* section.

7.3.2 Outputs (OUTA, OUTB)

In a typical TPS3701 application, the outputs are connected to a reset or enable input of the processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the outputs are connected to the enable input of a voltage regulator [such as a dc-dc converter or low-dropout regulator (LDO)].

The TPS3701 provides two open-drain outputs (OUTA and OUTB); use pullup resistors to hold these lines high when the output goes to a high-impedance state. Connect pullup resistors to the proper voltage rails to enable the outputs to be connected to other devices at correct interface voltage levels. The TPS3701 outputs can be pulled up to 25 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table. Use wired-OR logic to merge OUTA and OUTB into one logic signal.

表 1 and the *Inputs (INA, INB)* section describe how the outputs are asserted or high impedance. See 图 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUTA and OUTB signals correspond to the voltage on INA and INB as listed in 表 1.

7.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA and INB.

7.4.3 Power On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3701 is used as a precision dual-voltage supervisor in several different configurations. The monitored voltage (V_{MON}), VDD voltage, and output pullup voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

8.1.1 Window Comparator Considerations

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in 图 19 and 图 20. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA and INB monitor for undervoltage and overvoltage conditions, respectively.

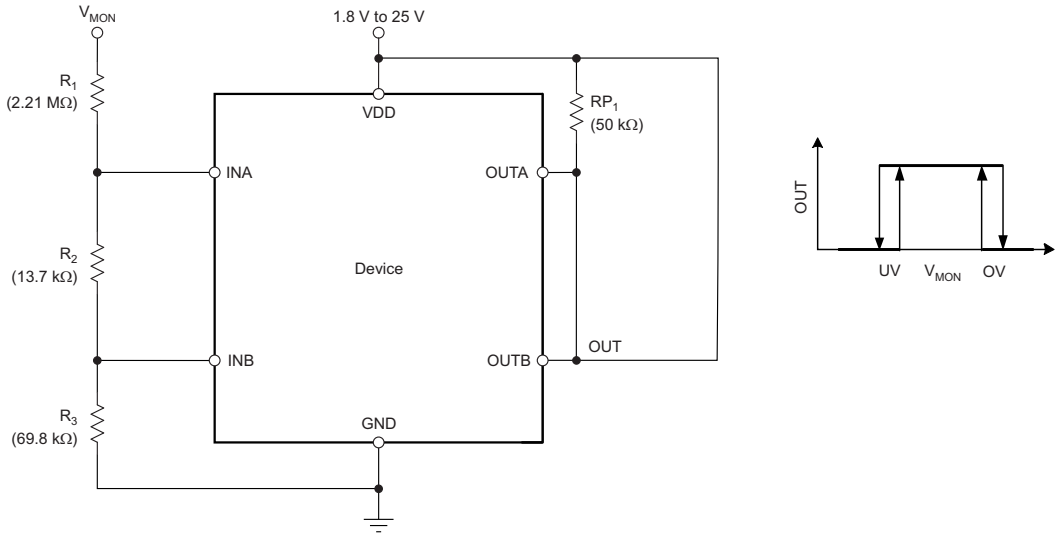


图 19. Window Comparator Block Diagram

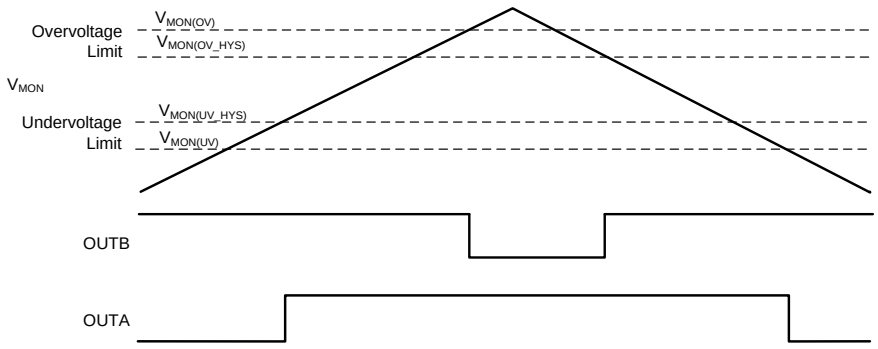


图 20. Window Comparator Timing Diagram

Application Information (接下页)

The TPS3701 flags the overvoltage or undervoltage condition with the greatest accuracy. The highest accuracy threshold voltages are $V_{IT-(INA)}$ and $V_{IT+(INB)}$, and correspond with the falling undervoltage flag, and the rising overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage is within the valid window (both OUTA and OUTB are in a high-impedance state), and correspond to the $V_{MON(UV)}$ and $V_{MON(OV)}$ trigger voltages, respectively. If the monitored voltage is outside of the valid window (V_{MON} is less than the undervoltage limit, $V_{MON(UV)}$, or greater than overvoltage limit, $V_{MON(OV)}$), then the input threshold voltages to re-enter the valid window are $V_{IT+(INA)}$ or $V_{IT-(INB)}$, and correspond with the $V_{MON(UV\_HYS)}$ and $V_{MON(OV\_HYS)}$ monitored voltages, respectively.

The resistor divider values and target threshold voltage can be calculated by using 公式 1 through 公式 4:

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose an R_{TOTAL} value so that the current through the divider is approximately 100 times higher than the input current at the INA and INB pins. Resistors with high values minimize current consumption; however, the input bias current degrades accuracy if the current through the resistors is too low. See application report *SLVA450, Optimizing Resistor Dividers at a Comparator Input*, for details on sizing input resistors.

R_3 is determined by 公式 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} \quad (2)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected.

R_2 is determined by either 公式 3 or 公式 4:

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV\_HYS)}} \bullet V_{IT+(INA)} \right) - R_3 \quad (3)$$

where

- $V_{MON(UV\_HYS)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises.

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA)} \right) - R_3 \quad (4)$$

where

- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected.

8.1.2 Input and Output Configurations

图 21 to 图 24 show examples of the various input and output configurations.

Application Information (接下页)

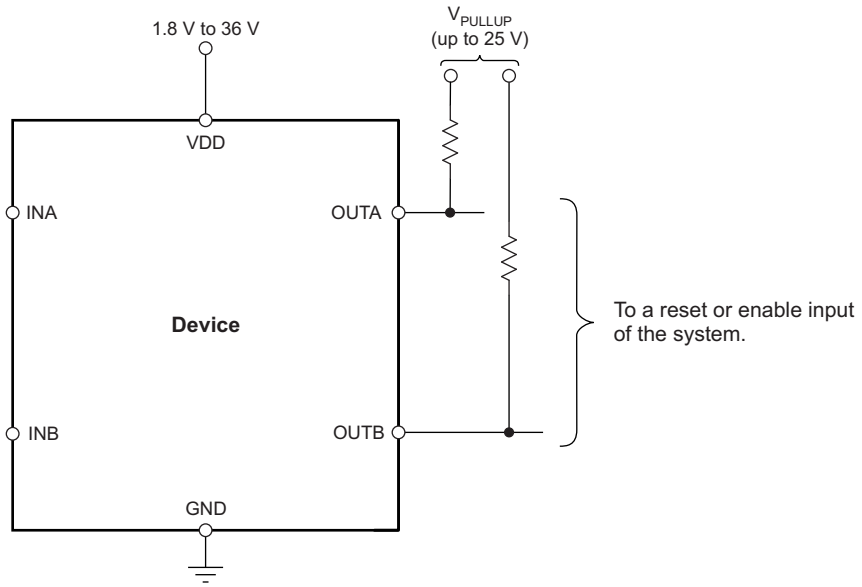


图 21. Interfacing to Voltages Other than V_{DD}

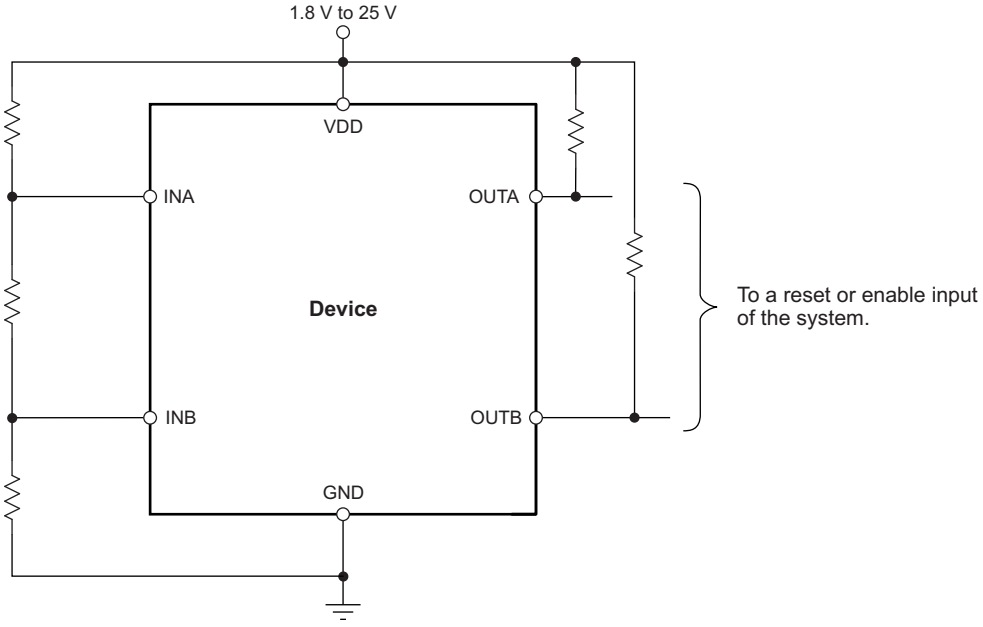
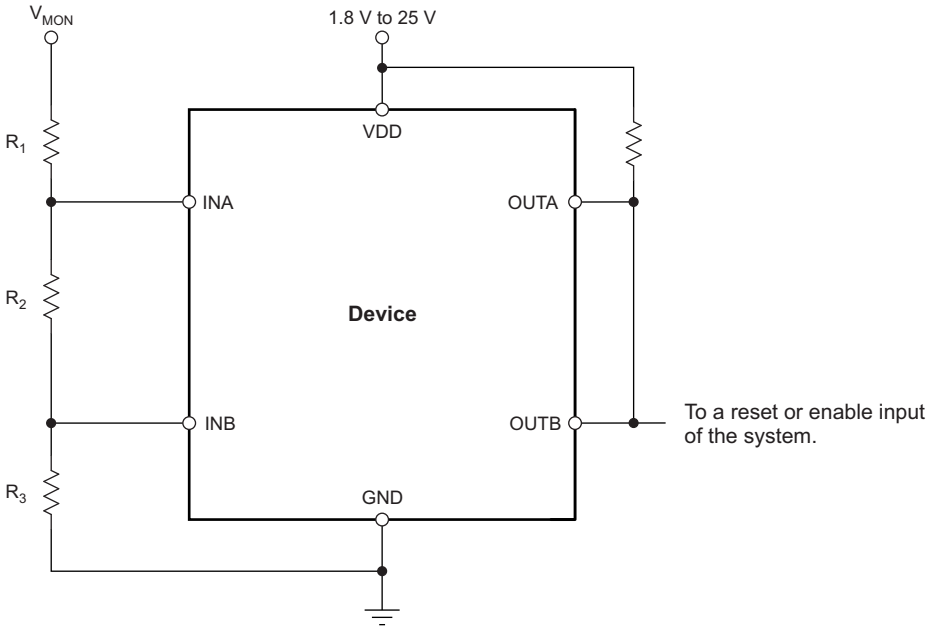


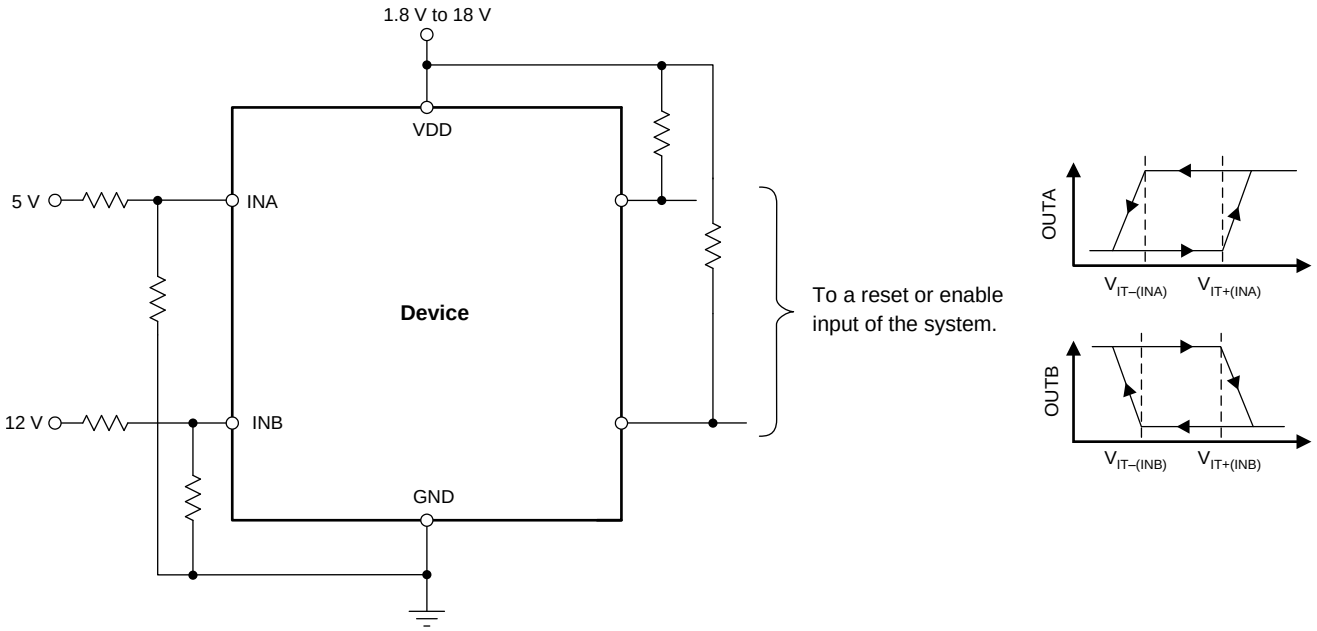
图 22. Monitoring the Same Voltage as V_{DD}

Application Information (接下页)



NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

图 23. Monitoring a Voltage Other than V_{DD}



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

图 24. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

8.1.3 Immunity to Input Pin Voltage Transients

The TPS3701 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and amplitude; see 图 3, *Minimum Pulse Duration vs Threshold Overdrive Voltage*.

8.2 Typical Application

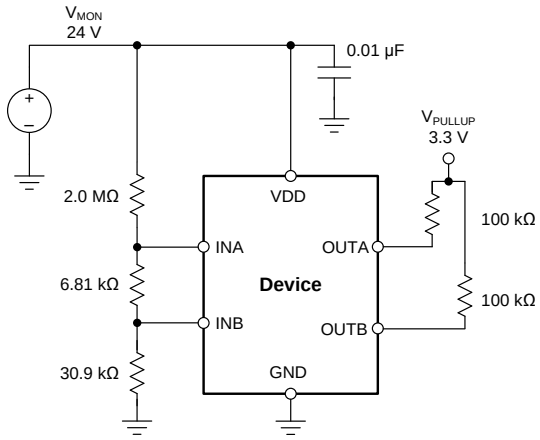


图 25. 24-V, 10% Window Comparator

8.2.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, rising ($V_{MON(OV)}$) and falling ($V_{MON(UV)}$) threshold ±10% nominal (26.4 V and 21.6 V, respectively)	$V_{MON(OV)}$ = 26.4 V ±2.7%, $V_{MON(UV)}$ = 21.6 V ±2.7%
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 µA	24 µA

8.2.2 Detailed Design Procedure

1. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification by using 公式 1. For this example, the current flow through the resistor network was chosen to be 13 µA; a lower current can be selected, however, care should be taken to avoid leakage currents that are artifacts of the manufacturing process. Leakage currents significantly impact the accuracy if they are greater than 1% of the resistor network current.

$$R_{TOTAL} = \frac{V_{MON(OV)}}{I} = \frac{26.4\ V}{13\ \mu A} = 2.03\ M\Omega \quad (5)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected as V_{MON} rises.
- I is the current flowing through the resistor network.

2. After R_{TOTAL} is determined, R_3 can be calculated using 公式 6. Select the nearest 1% resistor value for R_3. In this case, 30.9 kΩ is the closest value.

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} = \frac{2.03\ M\Omega}{26.4\ V} \bullet 0.4\ V = 30.7\ k\Omega \quad (6)$$

3. Use 公式 7 to calculate R2. Select the nearest 1% resistor value for R_2. In this case, 6.81 kΩ is the closest value.

$$R_2 = \frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA+)} - R_3 = \frac{2.03\ M\Omega}{21.6\ V} \bullet 0.4\ V - 30.9\ k\Omega = 6.69\ k\Omega \quad (7)$$

4. Use 公式 8 to calculate R1. Select the nearest 1% resistor value for R_1. In this case, 2 MΩ is the closest value.

$$R_1 = R_{TOTAL} - R_2 - R_3 = 2.03\ M\Omega - 6.81\ k\Omega - 30.9\ k\Omega = 1.99\ M\Omega \quad (8)$$

5. The worst-case tolerance can be calculated by referring to Equation 13 in application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*. An example of the rising threshold error, $V_{MON(OV)}$, is given in 公式 9:

$$\%\ ACC = \%\ TOL(V_{IT+(INB)}) + 2 \bullet \left(1 - \frac{V_{IT+(INB)}}{V_{MON(OV)}}\right) \bullet \%\ TOL_R = 0.75\ \% + 2 \bullet \left(1 - \frac{0.4}{26.4}\right) \bullet 1\% = 2.72\ \% \quad (9)$$

where

- % TOL($V_{IT+(INB)}$) is the tolerance of the INB positive threshold.
- % ACC is the total tolerance of the $V_{MON(OV)}$ voltage.
- % TOL_R is the tolerance of the resistors selected.

6. When the outputs switch to the high-Z state, the rise time of the OUTA or OUTB node depends on the pullup resistance and the capacitance on the node. Choose pullup resistors that satisfy the downstream timing requirements; 100-kΩ resistors are a good choice for low-capacitive loads.

8.2.3 Application Curves

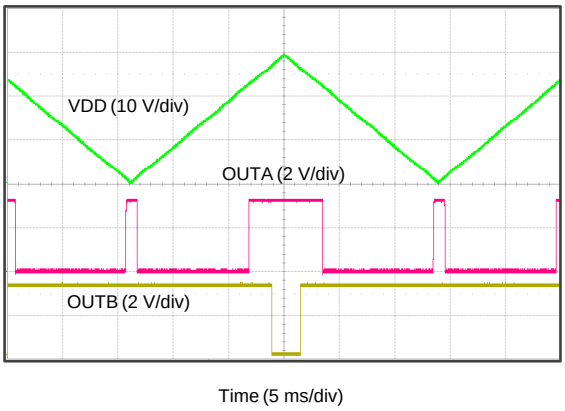


图 26. 24-V Window Monitor Output Response

9 Power Supply Recommendations

The TPS3701 has a 40-V absolute maximum rating on the VDD pin, with a recommended operating condition of 36 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100-Ω resistor and 0.01-µF capacitor is required in these cases, as shown in 图 27.

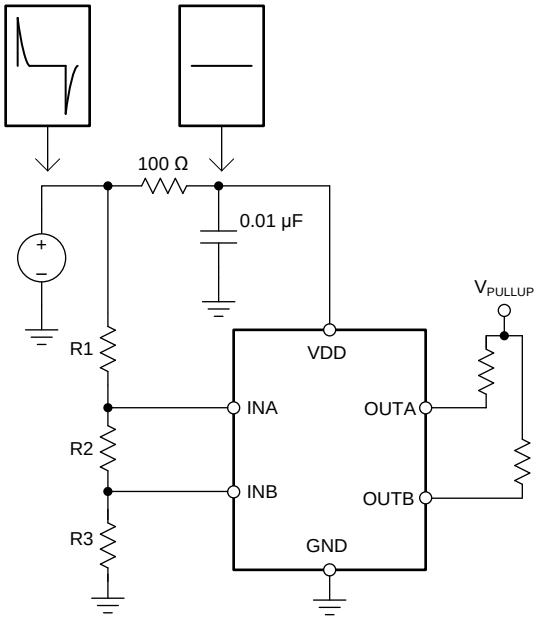


图 27. Using an RC Filter to Remove High-Frequency Disturbances on VDD

10 Layout

10.1 Layout Guidelines

- Place R_1, R_2, and R_3 close to the device to minimize noise coupling into the INA and INB nodes.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, may form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If this is unavoidable, see 图 27 for an example of filtering VDD.

10.2 Layout Example

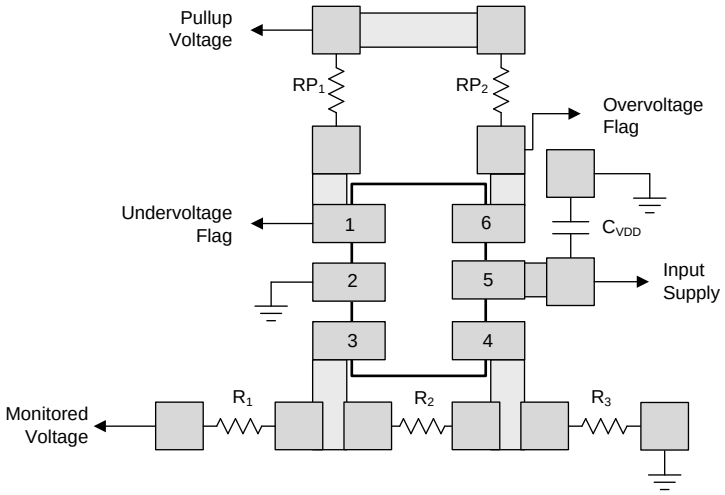


图 28. Recommended Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档，请参见以下应用报告和用户指南（可从 TI 网站获取）：

- 应用报告 SLVA600 —*《使用 TPS3700 作为负轨过压和欠压检测器》*。
- 应用报告 SLVA450 —*《优化比较器输入端的电阻分压器》*。
- 用户指南 SLVU683 —*《TPS3700EVM-114 评估模块》*。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3701DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ZABO	Samples
TPS3701DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ZABO	Samples

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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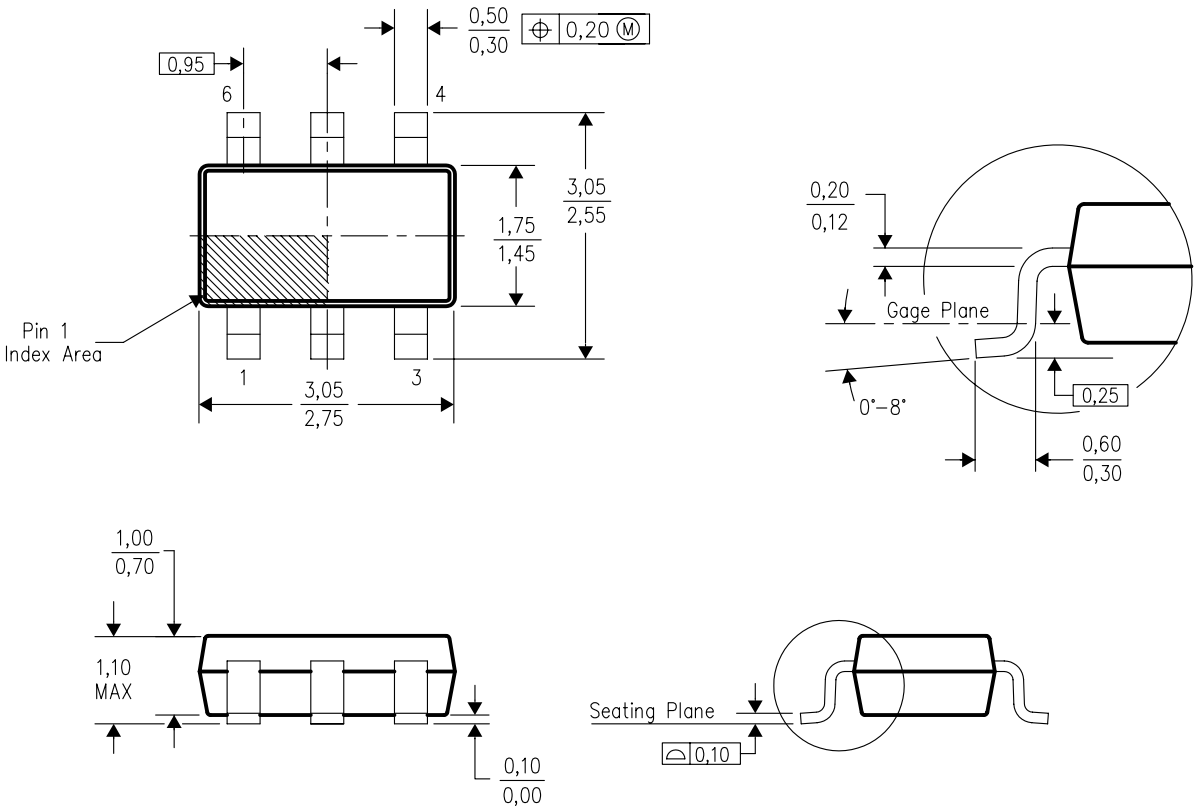
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



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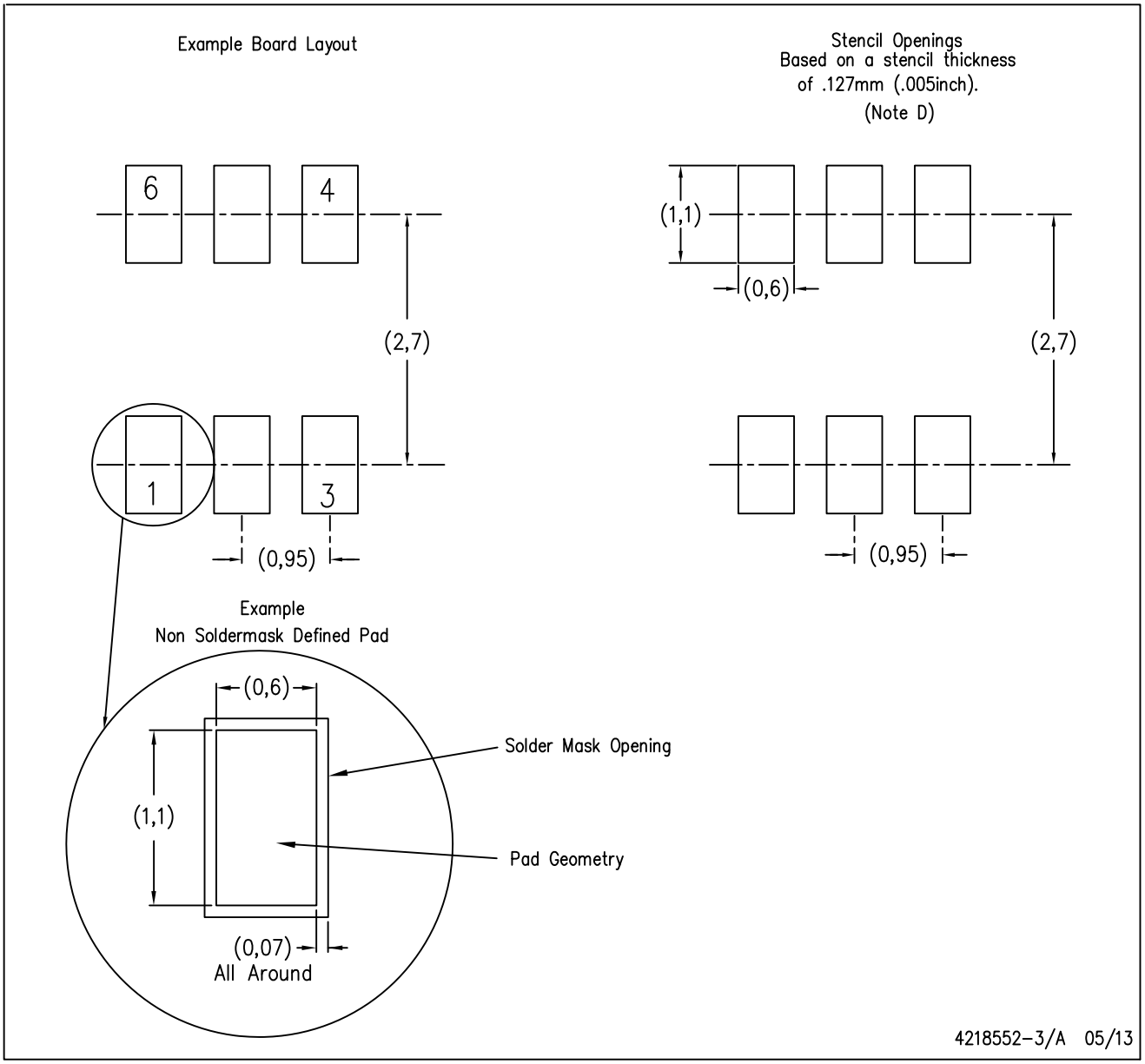
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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