LMS3655 5.5-A, 36-V Synchronous, 400-kHz DC-DC Step-Down Converter

1 Features

- 96% Peak Efficiency While Converting 12 V to 5 V
- Low EMI and Switch Noise
  - Minimized Switch Node Ringing
  - Pseudo-Random Spread Spectrum
- 400-kHz (±10%) Fixed Switching Frequency
- –40°C to +150°C Junction Temperature Range
- External Frequency Synchronization
- $\overline{\text{RESET}}$ Output With Internal Filter and 3-ms Release Timer
- Automatic Light Load Mode for Improved Efficiency
- Pin-Selectable Forced PWM Mode
- Built-In Compensation, Soft Start, Current Limit, Thermal Shutdown, and UVLO
- 0.35-V Dropout With 3.5-A Load at 25°C (Typical)
- 32-µA I_{Q_VIN}: Quiescent Current at 3.3 V_{OUT} and No Load (Typical)
- 5.5-A Continuous Load Current
- Adjustable Output Voltage (1 V to 15 V)
- ±1.5% Reference Voltage Tolerance
- 4-mm × 5-mm, 0.5-mm Pitch SON Package

2 Applications

- Noise-Sensitive Medical Applications
- Telecom
- High Performance Industrial

3 Description

The LMS3655 synchronous buck regulators are optimized for high performance applications, providing an adjustable output of 1 V to 15 V. Seamless transition between PWM and PFM modes, along with a low quiescent current, ensures high efficiency and superior transient responses at all loads.

Advanced high speed circuitry allows the LMS3655 to regulate an input of 24V to an output of 3.3V at a fixed frequency of 400kHz while also enabling a continuous load current of 5.5 A. An innovative frequency foldback architecture allows this device to regulate a 3.3-V output from an input voltage of only 3.5 V. The input voltage can range up to 36 V, with transient tolerance up to 42 V, easing input surge protection design.

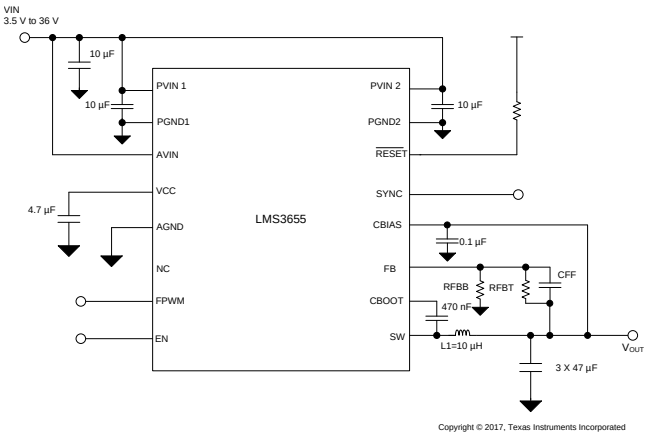
An open-drain reset output, with built-in filtering and delay, provides a true indication of system status. This feature negates the requirement for an additional supervisory component, saving cost and board space.

Device Information(1)

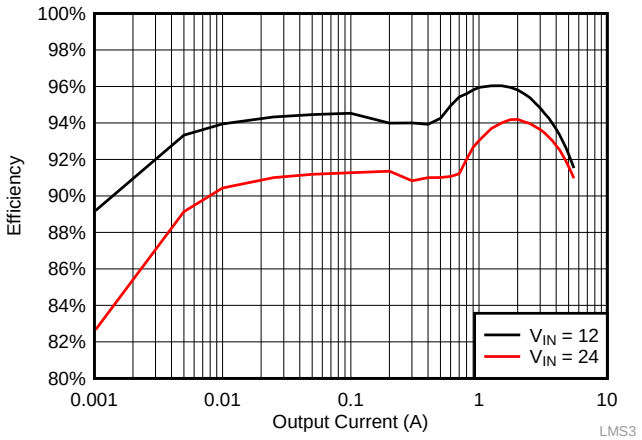
DEVICE NAME	PACKAGE	BODY SIZE
LMS3655	VQFN-HR (22)	4.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



LMS3655 Efficiency: V_{OUT} = 5 V



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

DATE	REVISION	NOTES
July 2017	*	Initial release.

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5 Device Comparison Table

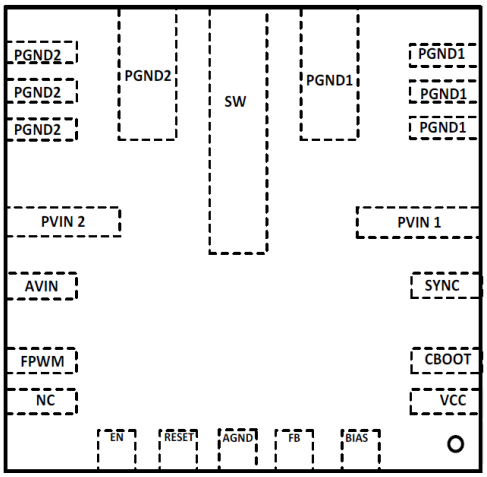
Table 1. LMS3655 Devices (5.5-A Output)

PART NUMBER	OUTPUT VOLTAGE	SPREAD SPECTRUM	PACKAGE QTY
LMS3655AMRNLR	Adjustable	No	3000
LMS3655AMRNLT	Adjustable	No	250
LMS3655MMRNLR	Adjustable	Yes	3000
LMS3655MMRNLT	Adjustable	Yes	250

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6 Pin Configuration and Functions

RNL Package
22-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VCC	A	Internal 3.1-V LDO output. Used as supply to internal control circuits. Connect a high-quality 4.7-µF capacitor from this pin to AGND.
2	CBOOT	P	Bootstrap capacitor connection for gate drivers. Connect a high quality 470-nF capacitor from this pin to the SW pin.
3	SYNC	I	Synchronization input to regulator. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock; frequency must be in the range of 250 kHz and 500 kHz.
4	PVIN1	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
5	PGND1	G	Power ground to internal low-side MOSFET. These pins must be tied together on the PCB. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
6			
7			
8			
9	SW	P	Regulator switch node. Connect to power inductor.
10	PGND2	G	Power ground to internal low-side MOSFET. These pins must be tied together. Connect PGND1 and PGND2 directly together at PCB. Connect to AGND and system ground.
11			
12			
13			
14	PVIN2	P	Input supply to regulator. Connect input bypass capacitors directly to this pin and PGND pins. Connect PVIN1 and PVIN2 pins directly together at PCB.
15	AVIN	A	Analog VIN. Connect to PVIN1 and PVIN2 on PCB.
16	FPWM	I	Mode control input of regulator. High = FPWM, low = Automatic light load mode. Do not float.
17	NC	—	No internal connection.
18	EN	I	Enable input to regulator. High = on, Low = off. Can be connected to VIN. Do not float.
19	$\overline{\text{RESET}}$	O	Open-drain reset output flag. Connect to suitable voltage supply through a current limiting resistor. High = regulator OK, Low = regulator fault. Goes low when EN = low.
20	AGND	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to PGND on PCB.
21	FB	A	Feedback input to regulator. Connect to feedback voltage divider.
22	BIAS	P	Input to auxiliary bias regulator. Connect to output voltage node.

(1) A = Analog, O = Output, I = Input, G = Ground, P = Power

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted). (1)

PARAMETER	MIN	MAX	UNIT
VIN (AVIN, PVIN1, and PVIN2) to AGND, PGND (2)	–0.3	40	V
SW to AGND, PGND (3)	–0.3	V_{IN} + 0.3	V
CBOOT to SW	–0.3	3.6	V
EN to AGND, PGND (2)	–0.3	40	V
BIAS to AGND, PGND	–0.3	16	V
FB to AGND, PGND	–0.3	16	V
$\overline{\text{RESET}}$ to AGND, PGND	–0.3	8	V
$\overline{\text{RESET}}$ sink current (4)		10	mA
SYNC to AGND, PGND (2)	–0.3	40	V
FPWM to AGND, PGND (2)	–0.3	40	V
VCC to AGND, PGND	–0.3	3.6	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A maximum of 42 V can be sustained at this pin for a duration of ≤ 500 ms at a duty cycle of ≤ 0.01%.
(3) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.
(4) Do not exceed the voltage rating on this pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted).

	MIN	NOM	MAX	UNIT
Input voltage after start-up (1)	3.9		36	V
Output adjustment for LMS3655 (2)	3.3		6	V
Extended output adjustment for LMS3655 (3)	1		15	V
Load current for LMS3655			5.5	A
Operating ambient temperature (4)	–40		125	°C

(1) An extended input voltage range to 3.5 V is possible; see *System Characteristics* table. See *Input UVLO* for start-up conditions.
(2) The output voltage must not be allowed to fall below zero volts during normal operation.
(3) Operation below 3.3 V and above 6 V may require changes to the typical application schematic, operation may not be possible over the full input voltage range, and some system specifications will not be achieved for this extended output voltage range. Consult the factory for further information.
(4) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 150°C.

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7.4 Thermal Information

THERMAL METRIC(1)		LMS3655 RNL (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	16.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information (for Device Mounted on PCB)

THERMAL METRIC(1)		LMS3655 RNL (VQFN) 22 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29.4	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	14.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	°C/W

(1) Mounted on a thermally optimized FR4 four layer EVM with a size of 4000 mill × 3000 mill.

7.6 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Initial reference voltage for 5-V and 3.3-V options	V_{IN} = 3.8 V to 36 V, T_J = 25°C	–1%		1%	
		V_{IN} = 3.8 V to 36 V	–1.5%		1.5%	
I_Q	Operating quiescent current; measured at VIN pin when enabled and not switching(1)	V_{IN} = 13.5 V, V_{BIAS} = 5 V		7.5	16	µA
I_B	Bias current into BIAS pin, enabled, not switching	V_{IN} = 13.5 V, V_{BIAS} = 5 V, FPWM = 0 V		53	62	µA
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V, FPWM = 0 V		53	62	
I_{SD}	Shutdown quiescent current; measured at VIN pin	EN ≤ 0.4 V		2	3	µA
$V_{IN-OPERATE}$	Minimum input voltage to operate	Rising	3.2	3.55	3.90	V
		Falling	2.95	3.25	3.55	
		Hysteresis	0.28	0.3	0.4	
V_{RESET}	$\overline{\text{RESET}}$ upper threshold voltage	Rising, % of V_{OUT}	105%	107%	110%	
	$\overline{\text{RESET}}$ lower threshold voltage	Falling, % V_{OUT}	92%	94%	96.5%	
	Magnitude of $\overline{\text{RESET}}$ lower threshold from steady state output voltage	Steady-state output voltage and $\overline{\text{RESET}}$ falling threshold read at the same T_J and V_{IN}			96%	

(1) This is the current used by the device while not switching, open loop on the ATE. It does not represent the total input current from the regulator system.

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Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RESET_HYST}	$\overline{RESET}$ hysteresis as a percent of output voltage setpoint			±1%		
V_{RESET_VALID}	Minimum input voltage for proper $\overline{RESET}$ function	50-µA pullup to $\overline{RESET}$ pin, EN = 0 V, T_J= 25°C			1.5	V
V_{OL}	Low level $\overline{RESET}$ function output voltage	50-µA pullup to $\overline{RESET}$ pin, V_{IN} = 1.5 V, EN = 0 V			0.4	V
		0.5-mA pullup to $\overline{RESET}$ pin, V_{IN} = 13.5 V, EN = 0 V			0.4	
		1-mA pullup to $\overline{RESET}$ pin, V_{IN} = 13.5 V, EN = 3.3 V			0.4	
F_{SW}	Switching frequency	V_{IN} = 13.5 V, center frequency with spread spectrum, PWM operation	360	400	440	kHz
		V_{IN} = 13.5 V, without spread spectrum, PWM operation	360	400	440	
F_{SYNC}	Sync frequency range		250	400	500	kHz
D_{SYNC}	Sync input duty cycle range	High state input < 5.5 V and > 2.3 V	25%		75%	
V_{FPWM}	FPWM input threshold voltage	FPWM input high (MODE = FPWM)	1.5			V
		FPWM input low (MODE = AUTO with diode emulation)			0.4	
		FPWM input hysteresis	0.15		1	
FS_{SS}	Frequency span of spread spectrum operation			±3%		
F_{PSS}	Spread-spectrum pattern frequency(2)				1.2	Hz
I_{FPWM}	FPWM leakage current	V_{IN} = 13.5 V, V_{FPWM} = 3.3 V		1		µA
		V_{IN} = V_{FPWM} = 13.5 V		1		
I_{SYNC}	SYNC leakage current	V_{IN} = 13.5 V, V_{SYNC} = 3.3 V		1		µA
		V_{IN} = V_{SYNC} = 13.5 V		1		
$I_{L\text{-}HS}$	High-side switch current limit	LMS3655	6.7	8.5	9.5	A
$I_{L\text{-}LS}$	Low-side switch current limit	LMS3655	6	7	7.7	A
$I_{L\text{-}ZC}$	Zero-cross current limit FPWM = low			–0.02		A
$I_{L\text{-}NEG}$	Negative current limit FPWM = high			–1.5		
R_{DSON}	Power switch on-resistance	High-side MOSFET R_{DSON}, V_{IN} = 13 V, IL = 1 A		60	130	mΩ
		Low-side MOSFET R_{DSON}, V_{IN} = 13 V, IL = 1 A		40	80	
V_{EN}	Enable input threshold voltage - rising	Enable rising	1.7		2	V
V_{EN_HYST}	Enable threshold hysteresis		0.45		0.55	V
V_{EN_WAKE}	Enable wake-up threshold		0.4			V
I_{EN}	EN pin input current	V_{IN} = V_{EN} = 13.5 V		2	3	µA
V_{CC}	Internal V_{CC} voltage	V_{IN} 13.5 V, V_{BIAS} = 0 V		3.05		V
		V_{IN} = 13.5 V, V_{BIAS} = 3.3 V		3.15		
V_{CC_UVLO}	Internal V_{CC} input undervoltage lockout	V_{IN} rising		2.7		V
		Hysteresis below $V_{CC\text{-}UVLO}$		185		mV

(2) Ensured by Design, Not tested at production.

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Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{FB}	Input current from FB to AGND	FB = 1 V		20		nA
V_{REF}	Reference voltage	T_J = 25°C	0.993	1	1.007	V
		T_J = –40°C to 125°C	0.99	1	1.01	
R_{RESET}	R_{DSON} of $\overline{RESET}$output	Pull FB pin low. Sink 1-mA at RESET pin		50	120	Ω
V_{SYNC}	V_{IH}		1.5			V
	V_{IL}				0.4	
	V_{HYST}		0.15		1	
T_{SD}	Thermal shutdown thresholds(2)	Rising	160		185	°C
		Hysteresis		15		
D_{MAX}	Maximum switch duty cycle	F_{sw} = 400 kHz		96%		
		While in dropout(2)	98%			

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7.7 System Characteristics

The following specifications are ensured by design provided that the component values in the typical application circuit are used. These parameters are not ensured by production testing. Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN-MIN}	Minimum input voltage for full functionality at 3.5-A load, after start-up.	V_{OUT} = 3.3 V +2% or –3% regulation		3.5		V
	Minimum input voltage for full functionality at maximum rated load 5.5 A after start-up.	V_{OUT} = 3.3 V +2% or –3% regulation		3.8		
V_{OUT}	Output voltage for adjustable option	V_{IN} = V_{OUT} + 1 V to 36 V, I_{OUT} = 3.5 A	–2.25%		2.25%	
F_{SW}	Switching frequency	V_{IN} = 24 V, FPWM = 24V, V_{OUT} = 3.3 V, I_{OUT} = 200 mA		400		kHz
I_{Q_VIN}	Input current to VIN pin	V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A , FPWM = 0, RFBT=49.9kΩ, RFBB=21.7kΩ		32		µA
		V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 0 A, FPWM = 0, RFBT=49.9kΩ, RFBB=12.4kΩ		57		
V_{DROP1}	Minimum input to output voltage differential to maintain regulation accuracy without inductor DCR drop	V_{OUT} = 3.3 V or 5 V, I_{OUT}= 3.5 A, +2% or –3% output accuracy		0.35	0.6	V
		V_{OUT} = 3.3 V or 5 V, I_{OUT}= 5.5 A, +2% or –3% output accuracy		0.65	0.85	V
V_{DROP2}	Minimum input to output voltage differential to maintain F_{SW} ≥ 330 kHz without inductor DCR drop	V_{OUT} = 3.3 V or 5 V, I_{OUT} = 3.5 A, F_{SW} = 330 kHz, 2% regulation accuracy		0.5	0.7	V
		V_{OUT} = 3.3 V or 5 V, I_{OUT} = 5.5 A, F_{SW} = 330 kHz, 2% regulation accuracy		0.7	1.2	V
Efficiency	Typical Efficiency	V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 3.5 A		94%		
		V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 3.5 A		92%		
		V_{IN} = 13.5 V, V_{OUT} = 5 V, I_{OUT} = 100 mA		92%		

7.8 Timing Requirements

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5 V.

		MIN	NOM	MAX	UNIT
t_{ON}	Minimum switch on-time, V_{IN} = 18 V, I_L = 1 A		60	84	ns
t_{OFF}	Minimum switch off-time, V_{IN} = 3.8 V, I_L = 1 A		65	80	ns
$t_{RESET-act}$	Delay time to $\overline{RESET}$ high signal	2	3	4	ms
$t_{RESET-filter}$	Glitch filter time for $\overline{RESET}$ function (1)		24		µs
t_{SS}	Soft-start time from first switching pulse to V_{REF} at 90%	2.5	4	5	ms
t_{EN}	Turnon delay, C_{VCC} = 4.7 µF (2)		0.8		ms
t_W	Short-circuit wait time (*hiccup* time) (3)		6		ms
t_{FPWM}	Change transition time from AUTO to FPWM MODE, 10-mA load, V_{IN} = 13.5 V		250		µs
	Change transition time from FPWM to AUTO MODE, 10-mA load, V_{IN} = 13.5 V		450		

(1) See *Detailed Description*.
(2) This is the time from the rising edge of EN to the time that the soft-start ramp begins.
(3) T_w is the wait time between current limit trip and restart. T_w is nominally four times the soft-start time. However, provision must be made to make T_w longer to ensure survivability during an output short circuit.

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7.9 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25ºC. Specified temperatures are ambient.

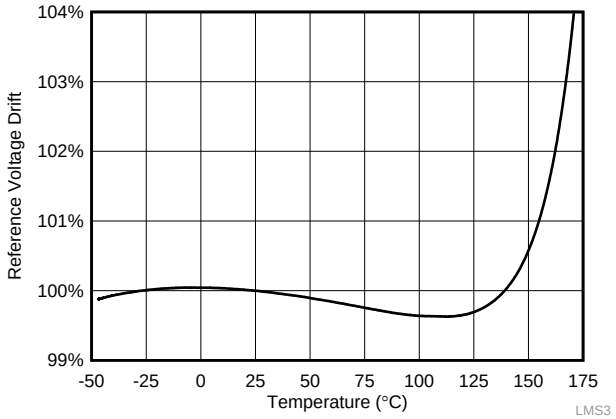


Figure 1. Reference Voltage Drift

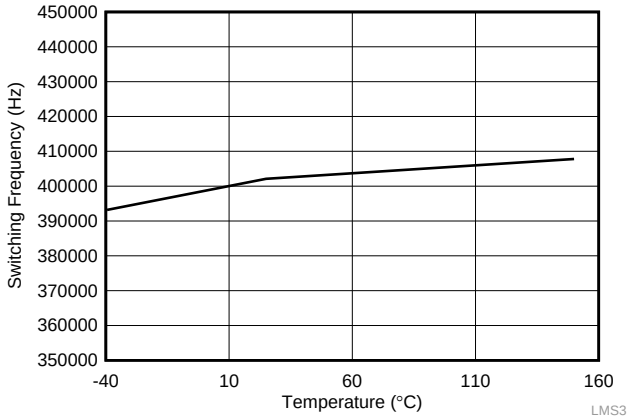


Figure 2. Switching Frequency vs Temperature

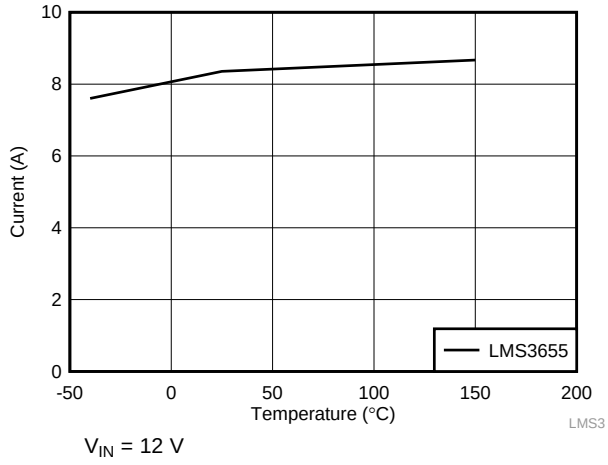


Figure 3. High-Side/Peak Current Limit for LMS3655

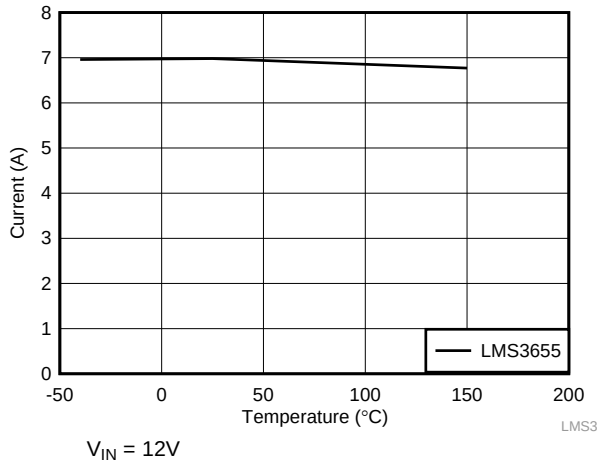


Figure 4. Low-Side/Valley Current Limit for LMS3655

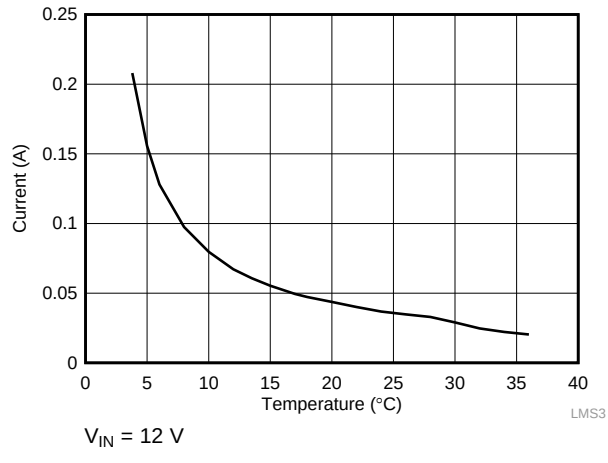


Figure 5. Short Circuit Average Input Current for LMS3655

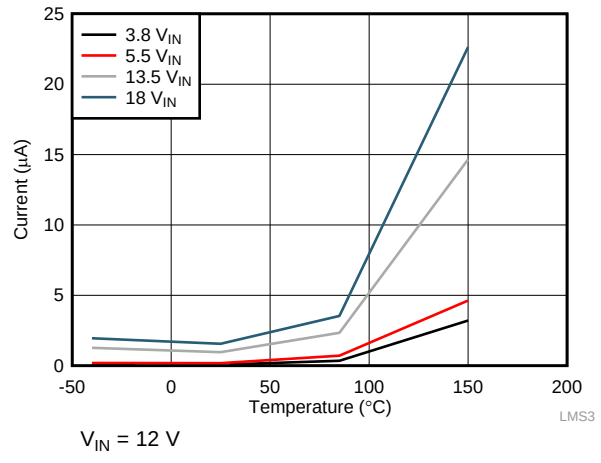


Figure 6. Shutdown Current

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Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, T_A = 25ºC. Specified temperatures are ambient.

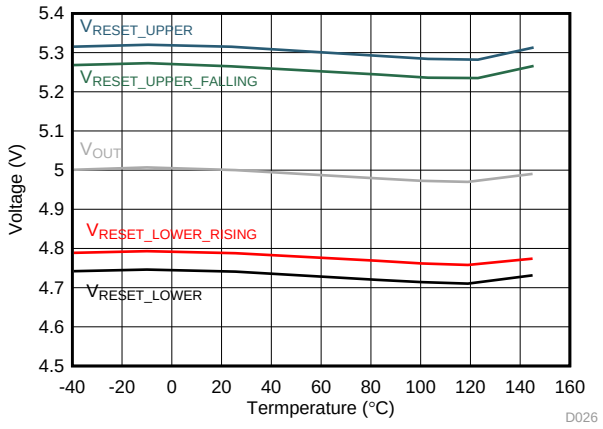


Figure 7. RESET Threshold 5-V Output

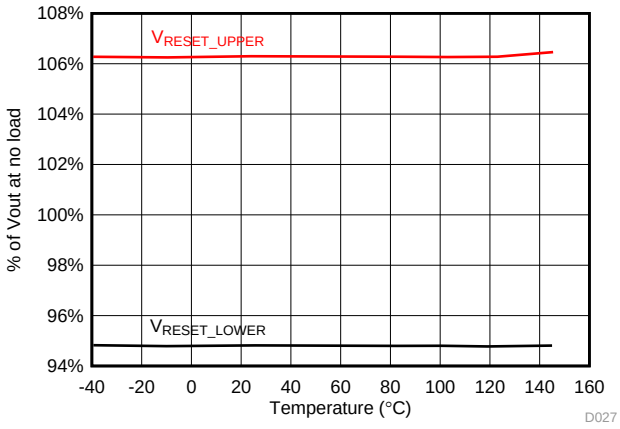


Figure 8. RESET Threshold as Percentage of Output Voltage

8 Detailed Description

8.1 Overview

The LMS3655 devices are wide-input voltage range, low quiescent current, high-performance regulators with internal compensation. This device is designed to minimize end-product cost and size while operating in demanding high-performance industrial environments. Normal operating frequency is 400 kHz allowing the use of small passive components. This device has a low unloaded current consumption, eliminating the need for an external backup LDO. The LMS3655 low shutdown current and high maximum operating voltage also allow for the elimination of an external load switch. To further reduce system cost, an advanced reset output is provided, which can often eliminate the use of an external reset or supervisor device.

The LMS3655 family is designed with a flip-chip or HotRod™ technology, greatly reducing the parasitic inductance of the pins. In addition, the layout of the device allows for partial cancellation of the current generated magnetic field which reduces the radiated noise generated by the switching action.

As a result the switch-node waveform exhibits less overshoot and ringing.

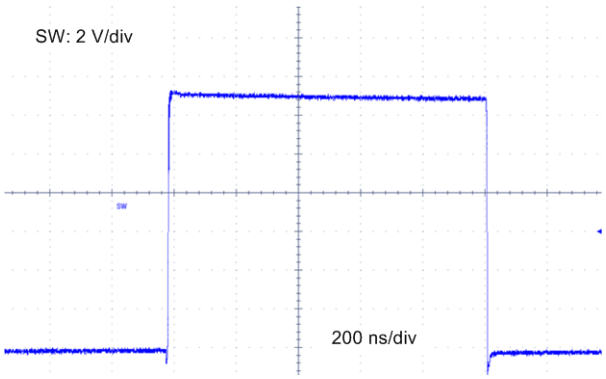
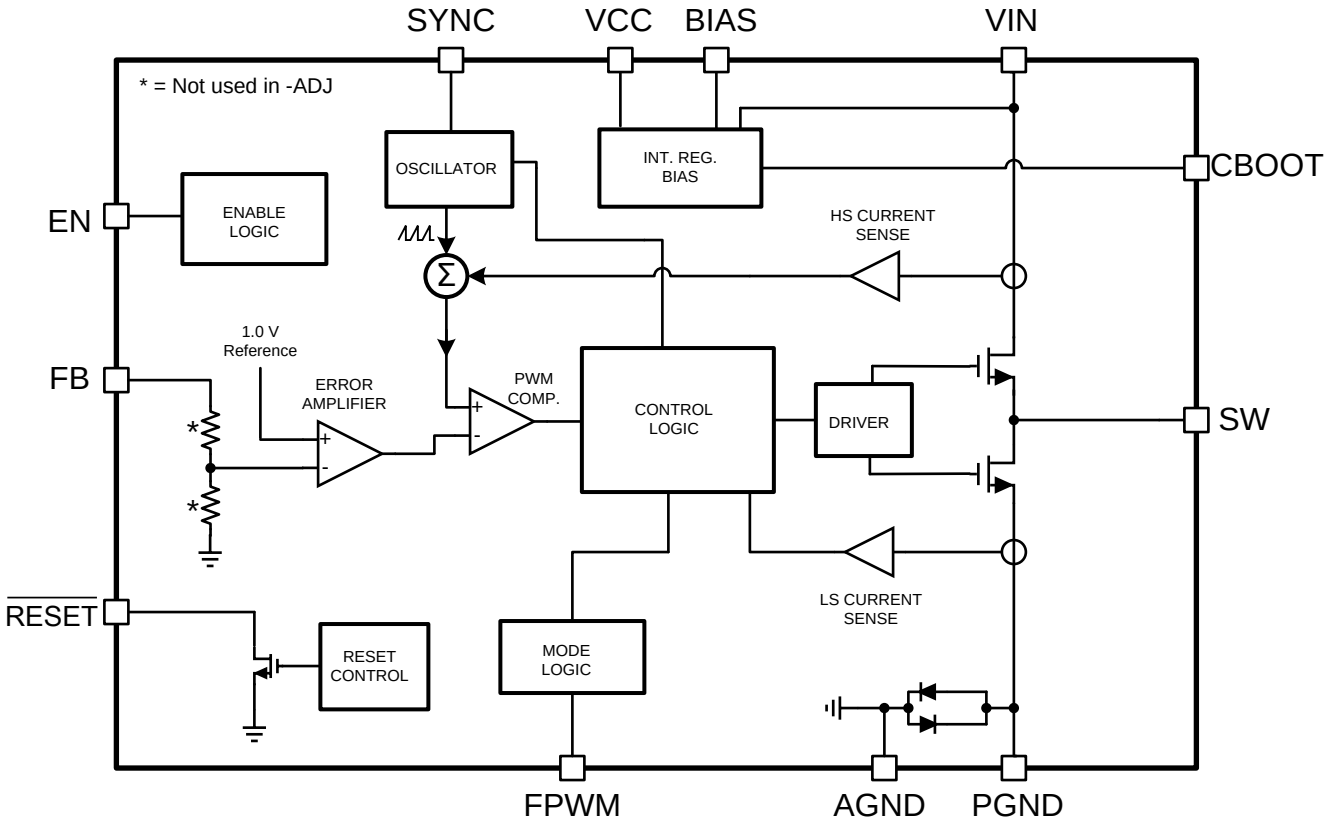


Figure 9. Switch Node Waveform (V_{IN} = 13.5 V, I_{OUT} = 5.5 A)

The LMS3655 is available in a VQFN package with wettable flanks which allows easy inspection of the soldering without the requirement of x-ray checks.

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8.2 Functional Block Diagram



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Functional Block Diagram (continued)

8.2.1 Control Scheme

The LMS3655 control scheme allows this device to operate under a wide range of conditions with a low number of external components. Peak current mode control allows a wide range of input voltages and output capacitance values while maintaining a constant switching frequency. Stable operation is maintained while output capacitance is changed during operation as well. This allows use in systems that require high performance during load transients and which have load switches that remove loads as the operating state changes. Short minimum on and off times ensure constant frequency regulation over a wide range of conversion ratios.

This architecture uses frequency spreading to achieve low dropout voltage maintaining output regulation as the input voltage falls close to output voltage. The frequency spreading is smooth and continuous, and activated as the off time approaches its minimum. Under these conditions, the LMS3655 operates like a constant off-time converter, allowing the maximum duty cycle to reach 98% and output voltage regulation with 650-mV dropout. As load current is reduced, the LMS3655 transitions to light load mode. In this mode, diode emulation is used to reduce RMS inductor current and switching frequency. Average output voltage increases slightly while lightly loaded as well.

8.3 Feature Description

8.3.1 $\overline{\text{RESET}}$ Flag Output

While the LMS3655 reset function resembles a standard Power-Good function, its functionality is designed to replace a discrete reset device, reducing additional component cost. There are three major differences between the reset function and the normal power good function seen in most regulators.

- A delay has been added between the point at which the output voltage is within specified limits and the flag asserts Power Good. A glitch filter prevents false flag operation for short excursions in the output voltage, such as during line and load transients. See Figure 11 and Figure 12 for more detail.
- $\overline{\text{RESET}}$ output signals a fault (pulls its output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ continues to operate with input voltage as low as 1.5 V. Below this input voltage, $\overline{\text{RESET}}$ output may be high impedance.

Because the $\overline{\text{RESET}}$ comparator and the regulation loop share the same reference, the thresholds track with the output voltage. When EN is pulled low, the $\overline{\text{RESET}}$ flag output is forced low. When the device is disabled, $\overline{\text{RESET}}$ remains valid as long as the input voltage is ≥ 1.5 V. $\overline{\text{RESET}}$ operation can best be understood by reference to Figure 10 and Figure 11. Output voltage excursions lasting less than $T_{RESET\text{-}filter}$ do not trip $\overline{\text{RESET}}$. Once the output voltage is within the prescribed limits, a delay of $T_{RESET\text{-}act}$ is imposed before $\overline{\text{RESET}}$ goes high. This enables tighter tolerance than is possible with an external supervisor device while also expanding the system allowance for transient response without the need for extremely accurate internal circuitry.

This output consists of an open-drain NMOS; requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT}, through an appropriate resistor, as desired. The pin can be left floating or grounded if the $\overline{\text{RESET}}$ function is not used in the application. The maximum current into this pin must be limited to 10 mA, and the maximum voltage must be less than 8 V.

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Feature Description (continued)

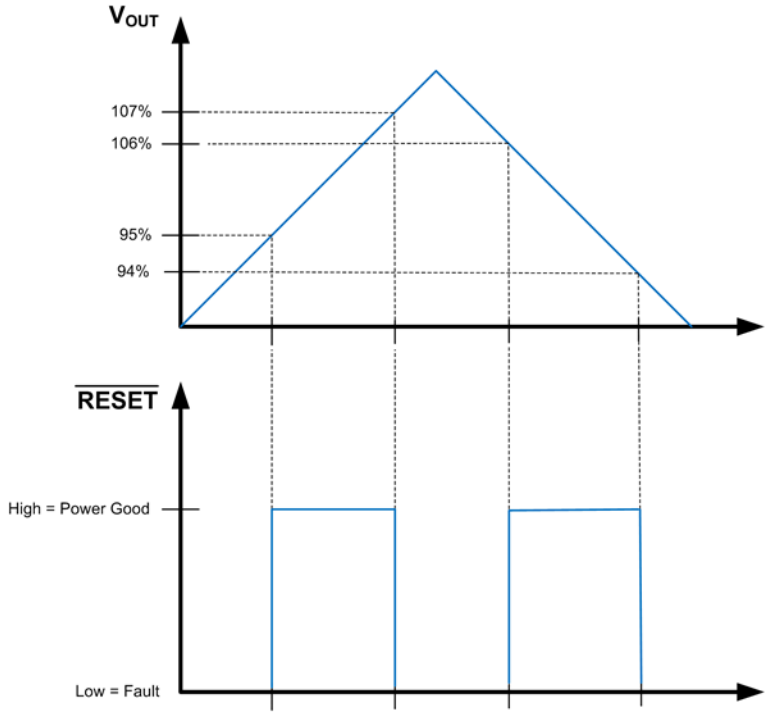


Figure 10. Static $\overline{\text{RESET}}$ Operation

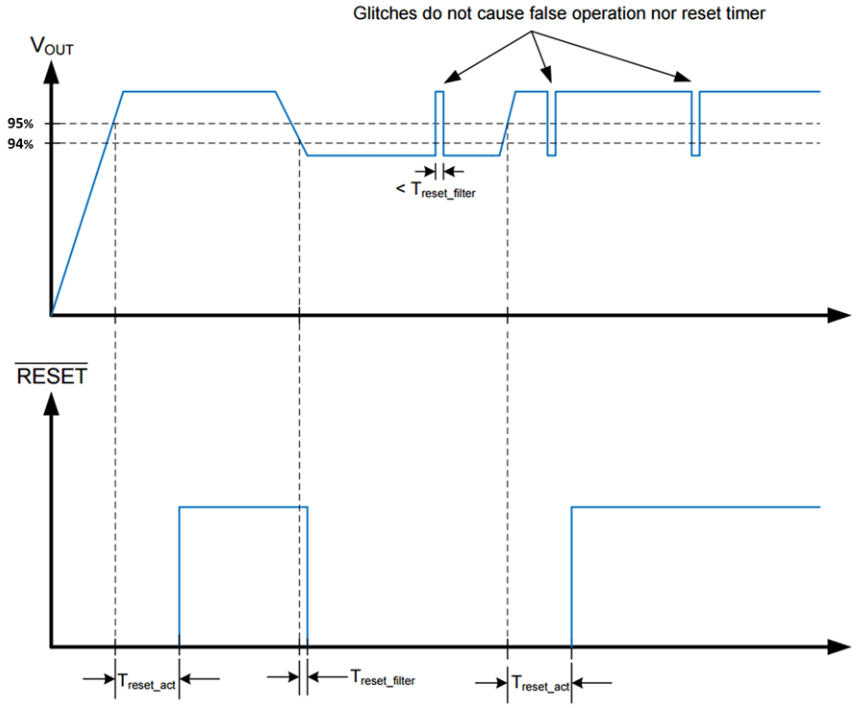


Figure 11. RESET Timing Behavior

Feature Description (continued)

The threshold voltage for the $\overline{\text{RESET}}$ function takes advantage of the availability of the LMS3655 internal feedback threshold to the $\overline{\text{RESET}}$ circuit. This allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual set point.

8.3.2 Enable and Start-Up

Start-up and shutdown of the LMS3655 are controlled by the EN input. Applying a voltage of ≥ 2 V activates the device, while a voltage of ≤ 1.45 V is required for shutdown. The EN input may also be connected directly to the input voltage supply. This input must not be left floating. The LMS3655 uses a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up.

A typical start-up waveform is shown in Figure 12 along with timing definitions. This waveform indicates the sequence and timing between the enable input, output voltage, and $\overline{\text{RESET}}$. From the figure, the user can define several different start-up times depending on what is relevant to the application. Table 2 lists the timing definitions and typical values.

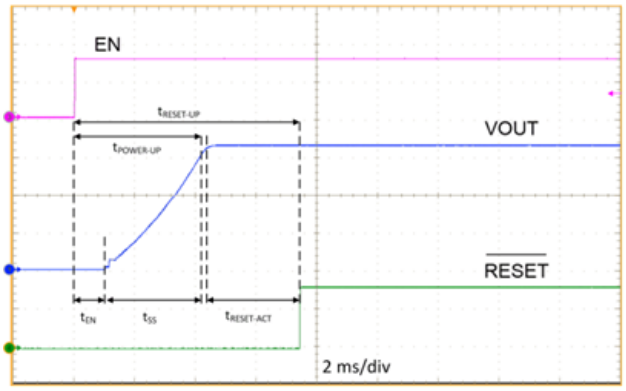


Figure 12. Typical Start-Up Waveform

Table 2. Typical Start-Up Times

PARAMETER		DEFINITION	VALUE	UNIT
$t_{RESET-READY}$	Total start-up sequence time	Time from EN to $\overline{\text{RESET}}$ released	7.5	ms
$t_{POWER-UP}$	Start-up time	Time from EN to 90% of V_{OUT}	4	ms
t_{SS}	Soft-start time	Rise time of V_{OUT} from 10% to 90%	3.2	ms
t_{EN}	Delay time	Time from EN to start of V_{OUT} rising	1	ms
$t_{RESET-ACT}$	$\overline{\text{RESET}}$ time	Time from output voltage within 94% and $\overline{\text{RESET}}$ released	3	ms

8.3.3 Soft-Start Function

Soft-start time is fixed internally at about 4 ms. Soft start is achieved by ramping the internal reference. The LMS3655 operates correctly even if there is a voltage present on the output before activation of the LMS3655 (prebiased start-up). The device operates in AUTO mode during soft start, and the state of the FPWM pin is ignored during that period.

8.3.4 Current Limit

The LMS3655 incorporates a valley current limit for normal overloads and for short-circuit protection. A precision low-side current limit prevents excessive average output current from the buck converter of the LMS3655. A high-side peak-current limit is employed for protection of the top NMOS FET and inductors. The two current limits enable use of smaller inductors than a system with a single current limit. This scheme allows use of inductors with saturation current rated less than twice the operating current of the LMS3655.

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During overloads the low-side current limit, $I_{L\text{-}LS}$ (see *Electrical Characteristics*), determines the maximum load current that the LMS3655 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below $I_{L\text{-}LS}$ before the next turnon cycle, then that cycle is skipped, and the low-side FET is left on until the current falls below $I_{L\text{-}LS}$. This is different than the more typical peak current limit, and results in Equation 1 for the maximum load current.

$$I_{OUT}\big|_{max} = I_{LS} + \frac{(V_{IN} - V_{OUT})}{2 \cdot F_S \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

If the converter continues triggering valley current limit for more than about 64 clock cycles, the device turns off both high and low side switches for approximately 6 ms (see T_W in *Timing Requirements*). If the overload is still present after the hiccup time, another 64 cycles is counted, and the process is repeated. If the current limit is not tripped for two consecutive clock cycles, the counter is reset. The hiccup time allows the inductor current to fall to zero, resetting the inductor volt-second balance. Of course the output current is greatly reduced in this condition (see *Typical Characteristics*). A typical short-circuit transient and recovery is shown in Figure 13.

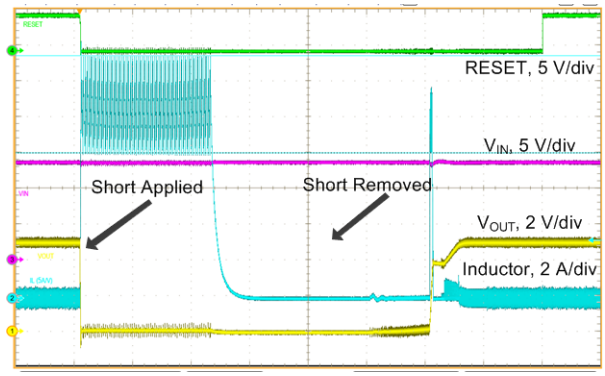


Figure 13. Short-Circuit Transient and Recovery

The high-side current limit trips when the peak inductor current reaches $I_{L\text{-}HS}$ (see *Electrical Characteristics*). This is a cycle-by-cycle current limit and does not produce any frequency or current foldback. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltage, this current limit may trip before the low-side protection. The peak value of this current limit varies with duty cycle.

In response to a short circuit, the peak current limit prevents excessive peak current while valley current limit prevents excessive average inductor current and keeps the power dissipation low during a fault. After a small number of cycles of valley current limit triggers, hiccup mode is activated.

In addition, the I_{NEG} current limit also protects the low-side switch from excessive negative current when the device is in FPWM mode. If this current exceeds I_{NEG}, the low-side switch is turned off until the next clock cycle. When the device is in AUTO mode, the negative current limit is increased to about I_{ZC} (about 0 A). This allows the device to operate in DCM.

8.3.5 Hiccup Mode

Hiccup mode prevents excessive heating and power consumption under sustained short-circuit conditions. If an overcurrent condition is maintained, the LMS3655 shuts off its output and waits for T_W (approximately 6 ms), after which the LMS3655 restarts operation by activating soft start.

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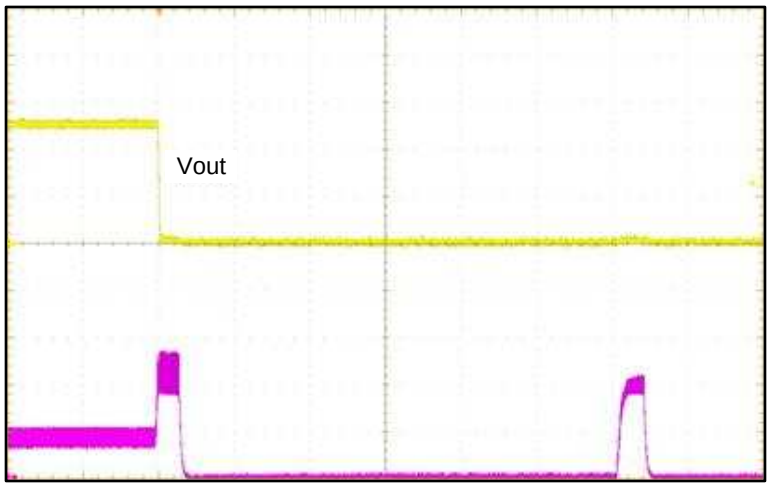


Figure 14. Hiccup Operation

During hiccup mode operation, the switch node of the LMS3655 is high impedance after a short circuit or overcurrent persists for a short duration. Periodically, the LMS3655 attempts to restart. If the short has been removed before one of these restart attempts, the LMS3655 operates normally.

8.3.6 Synchronizing Input

It is often desirable to synchronize the operation of multiple regulators in a single system. This technique results in better-defined EMI and can reduce the need for capacitance on some power rails. The LMS3655 provides a SYNC input which allows synchronization with an external clock. The LMS3655 implements an in-phase locking scheme—the rising edge of the clock signal provided to the SYNC input corresponds to turning on the high-side device within the LMS3655. The SYNC mode operation is implemented using phase locking over a limited frequency range eliminating large glitches upon initial application of an external clock. The clock fed into the LMS3655 replaces the internal free running clock but does not affect frequency foldback operation. Output voltage continues to be well regulated with duty factors outside of the normal 4% through 96% range though at reduced frequency.

The SYNC input recognizes a valid high level as that ≥ 1.5 V, and a valid low as that ≤ 0.4 V. The frequency synchronization signal must be in the range of 250 kHz to 500 kHz with a duty cycle of 10% to 90%. The internal clock is synced to the rising edge of the external clock. Ground this input if not used; this input must not be allowed to float. See *Device Functional Modes* to determine which modes are valid for synchronizing the clock.

The device remains in FPWM mode and operates in CCM for light loads when a synchronization input is provided. To prevent frequency foldback behavior at low duty cycles, provide a 200mA load.

8.3.7 Undervoltage Lockout (UVLO) and Thermal Shutdown (TSD)

The LMS3655 incorporates an input UVLO function. The device accepts an EN command when the input voltage rises above about 3.64 V and shuts down when the input falls below about 3.3 V. See *Electrical Characteristics* under $V_{IN\text{-}OPERATE}$ for detailed specifications.

TSD is provided to protect the device from excessive temperature. When the junction temperature reaches about 165°C, the device shuts down; restart occurs at a temperature of about 150°C.

8.3.8 Input Supply Current

The LMS3655 is designed to have very low input supply current when regulating light loads. This is achieved by powering much of the internal circuitry from the output. The BIAS pin is the input to the LDO that powers the majority of the control circuits. By connecting the BIAS input to the output of the regulator, this current acts as a small load on the output. This current is reduced by the ratio of V_{OUT} / V_{IN}, just like any other load.

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I_{Q_VIN} is defined as the current consumed by a converter using a LMS3655 device while regulating without a load. To calculate the theoretical total quiescent current, the below equation can be used with the open loop parameters from the *Electrical Characteristics* table. While operating without a load, the LMS3655 only powers itself. The device draws power from three sources: the V_{IN} pin (I_Q), the EN pin (I_{EN}), and the BIAS pin (I_B). Because the BIAS input is connected to the output of the circuit, the power consumed is converted from input power with an effective efficiency, ηeff. Here, effective efficiency is the added input power needed when lightly loading the converter of the LMS3655 devices and is divided by the corresponding additional load. This allows unloaded current to be calculated in Equation 2:

$$I_{Q_VIN} = I_Q + I_{EN} + \left(I_B + I_{div}\right)\frac{\text{Output Voltage}}{\eta_{eff} \times \text{Input Voltage}} \quad (2)$$

where

- I_{Q_VIN} is the current consumed by the operating (switching) buck converter while unloaded.
- I_Q is the current drawn by the LMS3655 from its V_{IN} terminal. See I_Q in *Electrical Characteristics*.
- I_{EN} is current drawn by the LMS3655 from its EN terminal. Include this current if EN is connected to VIN. See I_{EN} in *Electrical Characteristics*. Note that this current drops to a very low value if connected to a voltage less than 5 V.
- I_B is bias or feedback current drawn by the unloaded LMS3655. See I_B in *Electrical Characteristics*.
- I_{div} is the current drawn by the feedback voltage divider used to set output voltage.
- η_{eff} is the light load efficiency of the Buck converter with I_{Q_VIN} removed from the input current of the buck converter.

NOTE

The EN pin consumes a few micro-amperes when tied to high; see I_{EN}. Add I_{EN} to I_Q as shown in Equation 2 if EN is tied to V_{IN}. If EN is tied to a voltage less than 5 V, virtually no current is consumed allowing EN to be used as an UVLO pin once a voltage divider is added.

8.4 Device Functional Modes

Refer to Table 3 and the following paragraphs for a detailed description of the functional modes for the LMS3655.

These modes are controlled by the FPWM input as listed in Table 3. This input can be controlled by any compatible logic while the regulator is operating. If it is desired to fix the mode for a given application, the input can be either connected to ground, a logic supply, the VIN pin, or the VCC pin, as desired. The FPWM pin must not be allowed to float.

Table 3. Mode Selection

FPWM INPUT VOLTAGE	OPERATING MODE
> 1.5 V	**Forced PWM**: The regulator operates as a constant frequency, current mode, full-synchronous converter for all loads; without diode emulation.
< 0.4 V	**AUTO**: The regulator moves between PFM and PWM as the load current changes, using diode-emulation mode to allow DCM (see the *Glossary*).

8.4.1 AUTO Mode

In AUTO mode the device moves between PWM and PFM as the load changes. At light loads, the regulator operates in PFM. At higher loads, the mode changes to PWM. The load currents at which the mode changes can be found in the *Application Curves*.

In PWM, the converter operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple. When in PWM, the converter synchronizes to any valid clock signal on the SYNC input (see *Synchronizing Input*); during PFM operation, the SYNC input is ignored.

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In PFM, the high-side FET is turned on in a burst of one or more cycles to provide energy to the load. The frequency of these bursts is adjusted to regulate the output, while diode emulation is used to maximize efficiency (see the *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. A small increase in the output voltage occurs in PFM. This trades off very good light load efficiency for larger output voltage ripple and variable switching frequency. The actual switching frequency and output voltage ripple depend on the input voltage, output voltage, and load. See the *Application Curves* for output voltage variation in AUTO mode. A typical switching waveform for PFM is shown in Figure 15.

A unique feature of this device is that a minimum input voltage is required for the regulator to switch from PWM to PFM at light load. This feature is a consequence of the advanced architecture employed to provide high efficiency at light loads. Figure 16 indicates typical values of input voltage required to switch modes at no load. Also, once the regulator switches to PFM at light load, it remains in that mode if the input voltage is reduced.

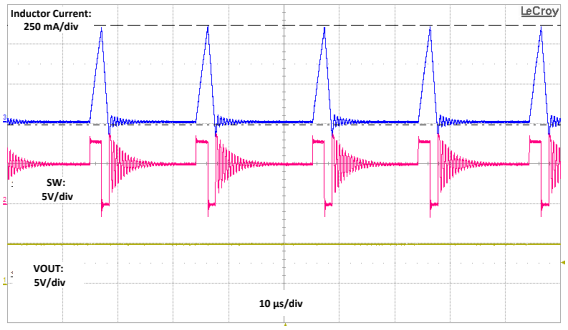


Figure 15. Typical PFM Switching Waveforms

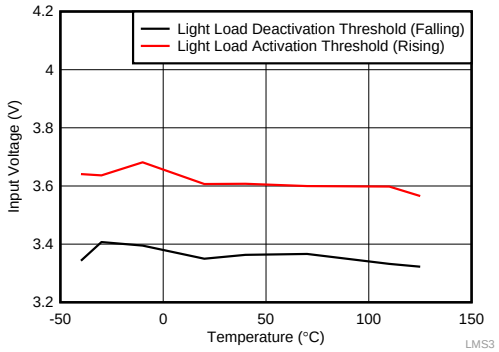


Figure 16. Input Voltage for Mode Change — 3.3-V Output, 10-µH Inductor

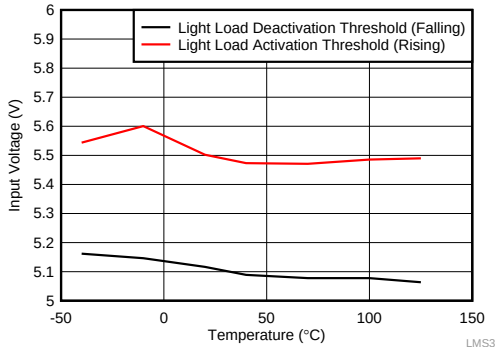


Figure 17. Input Voltage for Mode Change — 5-V Output, 10-µH Inductor

8.4.2 FPWM Mode

With a logic high on the FPWM input, the device is locked in PWM mode. This operation is maintained, even at no load, by allowing the inductor current to reverse its normal direction. To prevent frequency foldback behavior at low duty cycles, provide a 200mA load. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{NEG} is imposed to prevent damage to the low-side FET of the regulator. When in PWM, the converter synchronizes to any valid clock signal on the SYNC input (see *Synchronizing Input*).

When constant frequency operation is more important than light load efficiency, pull the LMS3655 FPWM input high or provide a valid synchronization input. Once activated, the diode emulation feature is turned off in this mode. This means that the device remains in CCM under light loads. Under conditions where the device must reduce the on time or off time below the ensured minimum, the frequency reduces to maintain the effective duty cycle required for regulation. This can occur for high input or output voltage ratios.

With the FPWM pin pulled low (*normal* mode), the diode emulation feature is activated. Device operation is the same as above; however, the regulator goes into DCM operation when the valley of the inductor current reaches zero.

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This feature may be activated and deactivated while the part is regulating without removing the load. This feature activates and deactivates gradually preventing perturbation of output voltage. When in FPWM mode, a limited reverse current is allowed through the inductor allowing power to pass from the regulator's output to its input. In this case, ensure that a large enough input capacitor is used to absorb the reverse current.

NOTE

While FPWM is activated, larger currents pass through the inductor than in AUTO mode when lightly loaded. This may result in more EMI, though at a predictable frequency. Once loads are heavy enough to necessitate CCM operation, FPWM has no measurable effect on the operation of the regulator.

8.4.3 Dropout

The minimum off time influences the dropout performance of the buck regulator. As the input voltage is reduced, to near the output voltage, the off-time of the high-side switch starts to approach the minimum value (see *Electrical Characteristics*). Beyond this point the switching may become erratic or the output voltage falls out of regulation. To avoid this problem, the LMS3655 automatically reduces the switching frequency to increase the effective duty cycle. This results in two specifications regarding dropout voltage, as shown in *System Characteristics*. One specification indicates when the switching frequency drops to 330 kHz. The other specification indicates when the output voltage has fallen to 3% of nominal. See the *Application Curves* for typical dropout values. Figure 18 and Figure 19 show the overall dropout characteristic for the 5-V option. Additional dropout information is discussed in *Application Curves* for 5-V output and in *Application Curves* for 3.3-V output.

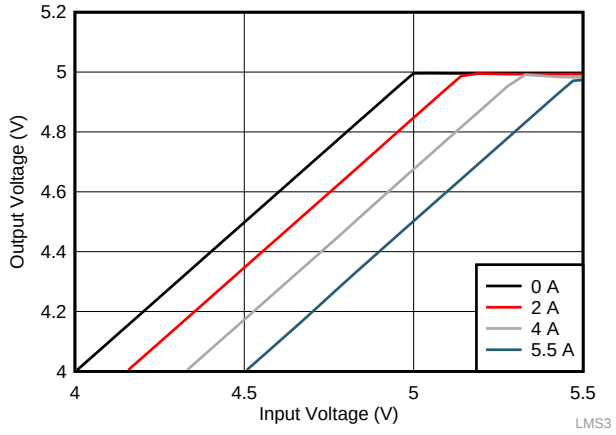


Figure 18. Overall Dropout Characteristics (V_{OUT} = 5 V)

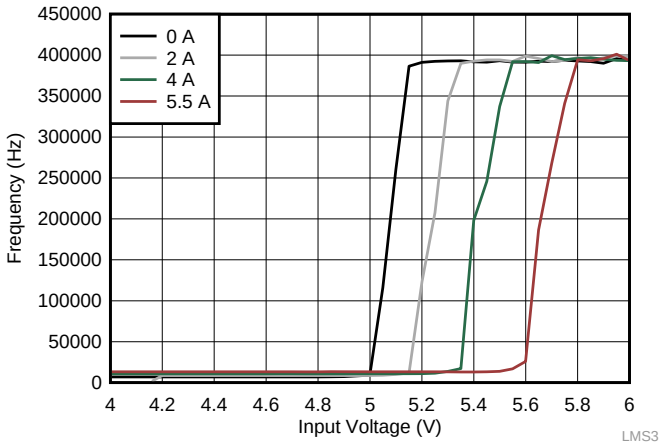


Figure 19. Frequency Dropout Characteristics (V_{OUT} = 5 V)

8.4.4 Spread-Spectrum Operation

The spread spectrum is a factory option. In order to find which parts have spread spectrum enabled, see *Device Comparison Table*.

The purpose of the spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies. In most systems containing the LMS3655 devices, low frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node. The LMS3655 devices use a ±3% spread of frequencies which spread energy smoothly across the FM band but is small enough to limit sub-harmonic emissions below its switching frequency. Peak emissions at the part's switching frequency are only reduced by slightly less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The LMS3655 devices use a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). Intelligent pseudo random generator limits cycle to cycle frequency changes to limit output ripple. Pseudo random pattern repeats by approximately 1.2 Hz which is below the audio band.

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The spread spectrum is only available while the clock of the LMS3655 devices is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the SYNC/MODE terminal.
- The clock is slowed due to operation at low input voltage; this is operation in dropout.
- The clock is slowed under light load in Auto mode; this is normally not seen above 200 mA of load. In FPWM mode, spread spectrum is active even if there is no load.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMS3655 is a step-down DC-DC converter, typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 5.5 A. The following design procedures can be used to select components for the LMS3655. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool uses an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various design options.

9.2 Typical Applications

9.2.1 General Application

Figure 20 shows a general application schematic. FPWM, SYNC, and EN are digital inputs. $\overline{\text{RESET}}$ is an open-drain output.

- The FPWM pin can be connected to GND to enable light-load PFM operation. Select this option if current consumption at light load is critical. The pin can be connected to VCC or VIN for forced 400-kHz operation. Select this option if constant switching frequency is critical. The pin can also be driven by an external signal and can be toggled while the part is in operation (by an MCU, for example). Refer to the *Device Functional Modes* for more details on the operation and signal requirements of the FPWM pin.
- The SYNC pin can be used to control the switching frequency and the phase of the converter. If the function is not needed, tie the SYNC pin to GND, VCC, or VIN.
- The $\overline{\text{RESET}}$ pin can be left floating or tied to ground if the function is not required. If the function is needed, the pin must be connected to a DC rail through a pullup resistor (100 kΩ is the typical recommended value). Check *$\overline{\text{RESET}}$ Flag Output* for the details of the $\overline{\text{RESET}}$-pin function.
- Connect the output to the FB pin through a voltage divider. See *Detailed Design Procedure* for details on component selection.
- The BIAS pin can be connected directly to the output voltage. In applications that can experience inductive shorts (such as cases with long leads on the output), a 3 Ω or so is necessary between the output and the BIAS pin, and a small capacitor to GND is necessary close to the BIAS pin (C_{BIAS}). Alternatively, a Schottky diode can be connected between OUT and GND to limit the negative voltage that can arise on the output during inductive shorts. In addition, BIAS can also be connected to an external rail if necessary and if available. The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 400-kHz.
- Power components must be chosen carefully for proper operation of the converter. *Detailed Design Procedure* discusses the details of the process of choosing the input capacitors, output capacitors, and inductor for the application.

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Typical Applications (continued)

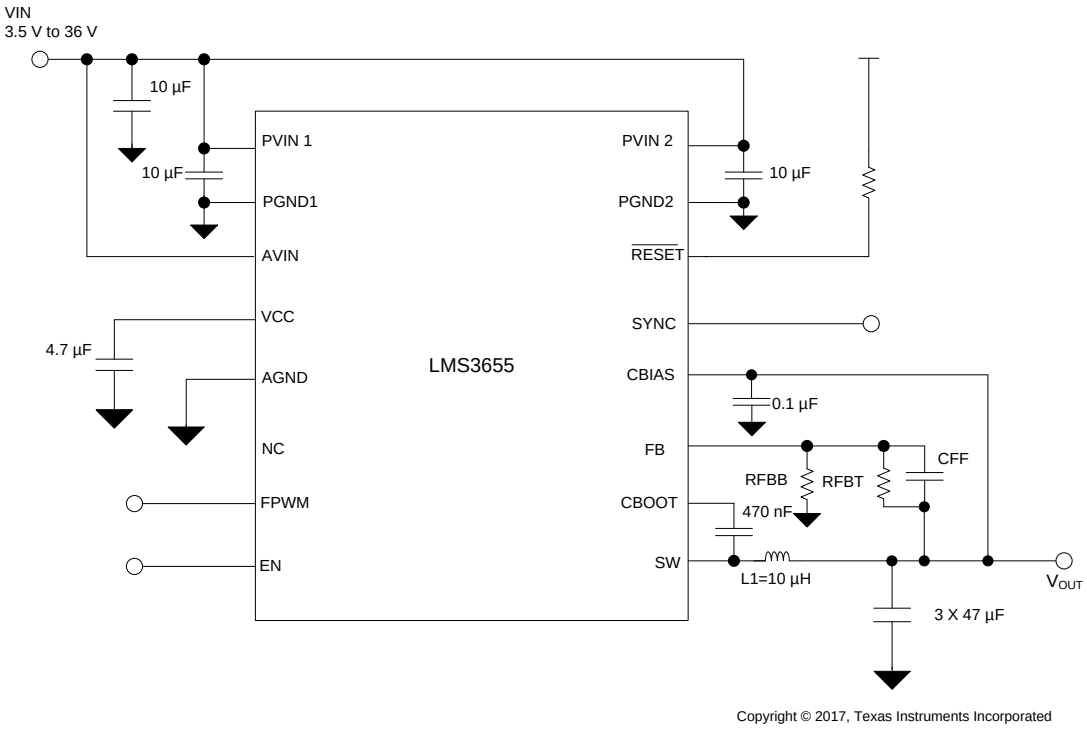


Figure 20. General Application Circuit

9.2.1.1 Design Requirements

Three sets of application-specific design requirements are outlined in Table 8, Table 9, and Table 10. The minimum input voltage shown in Figure 20 is not the minimum operating voltage of the LMS3655. Rather, it is a typical operating range for the systems. For the complete information regarding minimum input voltage see *Electrical Characteristics*.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 External Components Selection

The device requires input capacitors and an output inductor-capacitor filter. These components are critical to the performance of the device.

9.2.1.2.1.1 Input Capacitors

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The device is designed to be used with ceramic capacitors on the input of the buck regulator. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature.

The device requires a minimum of 20 µF of ceramic capacitance at the input. TI recommends 2 × 10 µF, 10 µF for PVIN1 and 10 µF for PVIN2. Place these capacitors close to the PVIN1, PGND1, PVIN2, and the PGND2 pads. The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying ripple current and isolating switching noise from other circuits. Table 4 shows the nominal and minimum values of total input capacitance recommended for the LMS3655. Also shown are the measured values of *effective* capacitance for the indicated capacitor.

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Typical Applications (continued)

In addition, it is especially important to have small ceramic bypass capacitors of 10 nF to 100 nF very close to the PVIN1 and PVIN2 inputs to minimize ringing and EMI generation due to the high-speed switching of the device coupled with trace inductance. TI recommends that a small case size 10-nF ceramic capacitor be placed across the input, as close to the device as possible. Additional high-frequency capacitors can be used to help manage conducted EMI or voltage spike issues that may be encountered.

Many times it is desirable to use an additional electrolytic capacitor on the input, in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Table 4. Recommended Input Capacitors

NOMINAL INPUT CAPACITANCE		MINIMUM INPUT CAPACITANCE		PART NUMBER
RATED CAPACITANCE	MEASURED CAPACITANCE(1)	RATED CAPACITANCE	MEASURED CAPACITANCE(1)	
3 × 10 µF	22.5 µF	2 × 10 µF	15 µF	CL32B106KBJNNNE

(1) Measured at 14 V and 25°C.

9.2.1.2.1.2 Output Inductors and Capacitors

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Overcurrent ruggedness

The device has been optimized for use with nominal LC values as shown in the Figure 20.

9.2.1.2.1.2.1 Inductor Selection

The LMS3655 devices run in current mode and with internal compensation. The compensation of the adjustable 5-V and 3.3-V configurations is stable with inductance between 6.5 µH and 20 µH. For most applications, the adjustable 5-V and 3.3-V configurations of the LMS3655 devices are optimized for a nominal inductance of 10 µH. This gives a ripple current that is approximately 20% to 30% of the full load current of 5.5 A. If applying a synchronization clock signal, the designer should appropriately size the inductor for the converter's operating switching frequency. For output voltages greater than 5 V, a proportionally larger inductor can be used, thus keeping the ratio of inductor current slope to internal compensating slope constant. Inductance that is too high is not recommended because it can result in poor load transient behavior and instability.

The inductor must be rated to handle the peak load current plus the ripple current—carefully review the different saturation current ratings specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. For the LMS3655, TI recommends a saturation current of 10 A or higher. Carefully review the inductor parasitic resistance; the inductor parasitic resistance must be as low as possible to minimize losses at heavy loads. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

Table 5 gives a list of several possible inductors that can be used with the LMS3655.

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, and so forth. In general, inductors of smaller physical size have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. TI recommends finding the best compromise between system performance and cost.

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Table 5. Recommended Inductors

MANUFACTURER	PART NUMBER	SATURATION CURRENT	DC RESISTANCE
Würth	7443251000	8.5 A	16 mΩ
Würth	7447709100	10.5 A	21 mΩ
Vishay	IHLP4040DZER100M01	12 A	36.5 mΩ

9.2.1.2.1.2.2 Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor, reduces the output voltage ripple, and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can be usually neglected at the converter's operating frequency range.

The LMS3655 is designed to work with low-ESR ceramic capacitors. TI recommends X5R and X7R type capacitors. The *effective* value of these capacitors is defined as the actual capacitance under voltage bias and temperature. All ceramic capacitors have a large voltage coefficient, in addition to normal tolerances and temperature coefficients. Under DC bias, the capacitance value drops considerably. Larger case sizes or higher voltage capacitors are better in this regard. To help mitigate these effects, multiple small capacitors can be used in parallel to bring the minimum *effective* capacitance up to the desired value. This can also ease the RMS current requirements on a single capacitor. Table 6 shows the nominal and minimum values of total output ceramic capacitance recommended for the LMS3655.The values shown also provide a starting point for other output voltages. More output capacitance can be used to improve transient performance and reduce output voltage ripple.

In order to minimize ceramic capacitance, a low ESR electrolytic capacitor can be used in parallel with minimal ceramic capacitance. As a starting point for designing with an output electrolytic capacitor, Table 7 shows the minimum ceramic capacitance recommended when paired with a 120µF Aluminum-polymer (ESR=25mΩ) in order to maintain stable operation. Depending on load transient design requirements, the designer may choose to add additional capacitance.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and should always be completed before the application goes into production. Make a careful study of temperature and bias voltage variation of any candidate ceramic capacitor in order to ensure that the minimum value of *effective* capacitance is provided. The best way to obtain an optimum design is to use the Texas Instruments WEBENCH Design Tool.

In adjustable applications the feed-forward capacitor, C_{FF}, provides another degree of freedom when stabilizing and optimizing the design. Refer to *Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor* (SLVA289) for helpful information when adjusting the feed-forward capacitor.

In addition to the capacitance shown in Table 6, a small ceramic capacitor placed on the output can help to reduce high frequency noise. Small case-size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor parasitics.

Limit the maximum value of total output capacitance to between 800 µF and 1200 µF. Large values of output capacitance can prevent the regulator from starting up correctly and adversely effect the loop stability. If values greater than the given range are to be used, then a careful study of start-up at full load and loop stability must be performed.

Table 6. Recommended Output Ceramic Capacitors (1)

OUTPUT VOLTAGE	NOMINAL OUTPUT CERAMIC CAPACITANCE	MINIMUM OUTPUT CERAMIC CAPACITANCE	PART NUMBER
	RATED CAPACITANCE	RATED CAPACITANCE	
3.3 V	4 × 47 µF	3 × 47µF	GRM32ER71A476KE15L
5 V	4 × 47 µF	3 × 47µF	GRM32ER71A476KE15L
6 V	4× 47 µF	3 × 47µF	GRM32ER71A476KE15L

(1) L = 10µH

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Table 6. Recommended Output Ceramic Capacitors (0) (continued)

OUTPUT VOLTAGE	NOMINAL OUTPUT CERAMIC CAPACITANCE	MINIMUM OUTPUT CERAMIC CAPACITANCE	PART NUMBER
	RATED CAPACITANCE	RATED CAPACITANCE	
10 V(2)	4 × 47 µF	3 × 47 µF	GRM32ER71A476KE15L

(2) L = 20µH

Table 7. Recommended Output Al-Polymer and Ceramic Capacitors (1)

OUTPUT VOLTAGE	OUTPUT AL-POLYMER CAPACITANCE	PART NUMBER	MINIMUM OUTPUT CERAMIC CAPACITANCE
	RATED CAPACITANCE		RATED CAPACITANCE
3.3 V	120 µF	APXE160ARA121MH70G	1 × 47µF + 1 x 20µF
5 V	120 µF	APXE160ARA121MH70G	1 × 47µF

(1) L = 10µH

Consult *Output Ripple Voltage for Buck Switching Regulator* (SLVA630) for more details on the estimation of the output voltage ripple for this converter.

9.2.1.2.2 FB for Adjustable Output

The LMS3655 devices regulate output voltage to a level that results in the FB node being V_{REF}, which is approximately 1 V (see *Electrical Characteristics*). Output voltage given a specific feedback divider can be calculated using Equation 3:

$$\text{Output Voltage} = V_{ref} \times \frac{R_{FBB} + R_{FBT}}{R_{FBB}} \tag{3}$$

To ensure proper behavior for all modes of operation, a 50-kΩ resistor is recommended for R_{FBT}. R_{FBB} can then be determined using Equation 4:

$$R_{FBB} = \frac{V_{ref} \times R_{FBT}}{\text{Output Voltage} - V_{ref}} \tag{4}$$

In addition, a feed-forward capacitor C_{FF} may be required to optimize the transient response. For output voltages greater than 6 V, the WEBENCH Design Tool can be used to optimize the design.

9.2.1.2.3 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the LMS3655. This output requires a 4.7-µF, 10-V ceramic capacitor connected from VCC to GND for proper operation. X7R type is recommended. In general, this output must not be loaded with any external circuitry. However, the output can be used to supply a logic level to the FPWM input or for the pullup resistor used with the $\overline{\text{RESET}}$ output. The nominal output of the LDO is 3.15 V.

9.2.1.2.4 BIAS

The BIAS pin is the input to the internal LDO. As detailed in *Input Supply Current*, this input is connected directly to V_{OUT} to provide the lowest possible supply current at light loads. Because this input is connected directly to the output, it must be protected from negative voltage transients. Such transients may occur when the output is shorted at the end of a long PCB trace or cable. If this is likely in a given application, then place a small resistor in series between the BIAS input and V_{OUT} as shown in Figure 23.

Size the resistor to limit the current out of the BIAS pin to < 100 mA. Values in the range of 2 Ω to 5 Ω are typically sufficient. Values greater than 5 Ω are not recommended. As a rough estimate, assume that the full negative transient appears across R_{BIAS} and design for a current of < 100 mA. In severe cases, a Schottky diode can be placed in parallel with the output to limit the transient voltage and current.

When a resistor is used between the output and the BIAS pin, a 0.1-µF capacitor is required close to the BIAS pin. In general, TI recommends having a 0.1-µF capacitor near the BIAS pin, regardless of the presence of the resistor, unless the trace between the output capacitors and the BIAS pin is very short.

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The typical current into the bias pin is 15 mA when the device is operating in PWM mode at 400 kHz.

9.2.1.2.5 CBOOT

The LMS3655 requires a *boot-strap* capacitor between the CBOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A ceramic capacitor of 0.47 µF, ≥ 6.3 V is required.

9.2.1.2.6 Maximum Ambient Temperature

As with any power conversion device, the LMS3655 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMS3655 is 150°C, thus establishing a limit on the maximum device power dissipation and therefore load current at high ambient temperatures. Equation 5 shows the relationships between the important parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \tag{5}$$

The device uses an advanced package technology that uses the pads and pins as heat spreading paths. As a result, the pads must be connected to large copper areas to dissipate the heat from the IC. All pins provide some heat relief capability but the PVINs, PGNDs, and SW pins are of particular importance for proper heat dissipation. Utilization of all the board layers for heat dissipation and using vias as heat pipes is recommended. The *Layout Guidelines* includes example that shows layout for proper heat management.

9.2.1.3 Application Curves

These parameters are not tested and represent typical performance only. Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

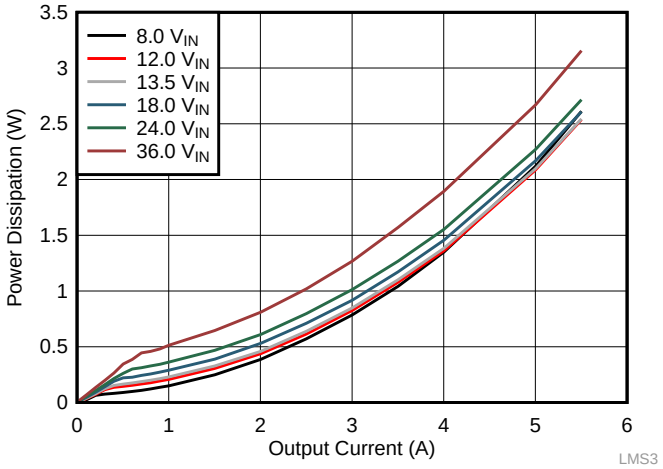


Figure 21. Power Dissipation 5-V Output

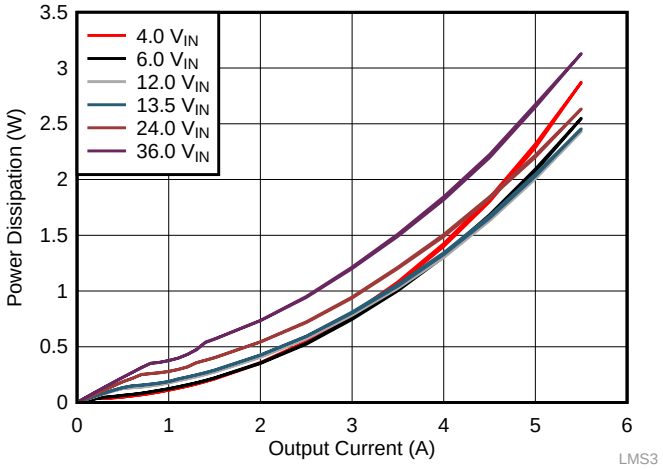
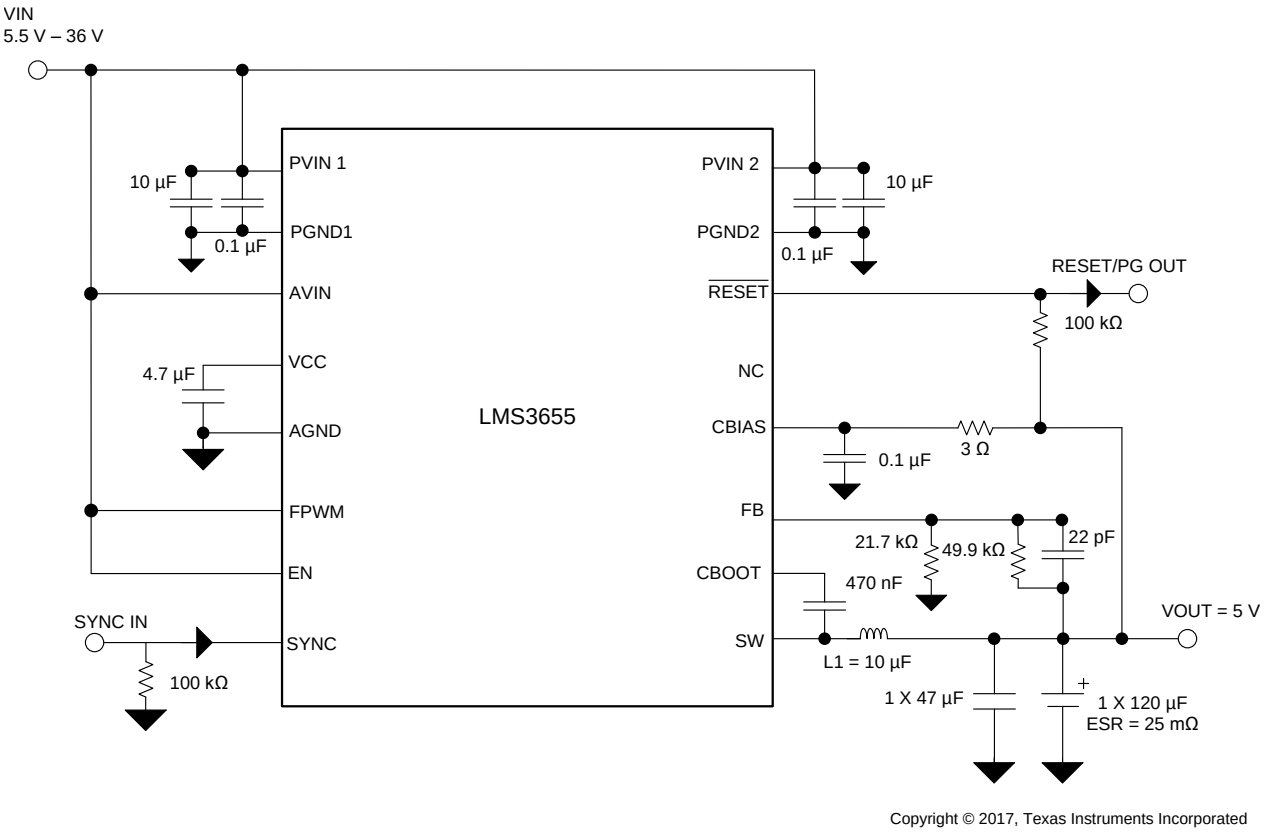


Figure 22. Power Dissipation 3.3-V Output

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9.2.2 Adjustable 5-V Output



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Figure 23. 5-V, 5.5-A Output Power Supply

9.2.2.1 Design Requirements

Example requirements for a typical 5-V application. The input voltages are here for illustration purposes only. See *Electrical Characteristics* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See Figure 29 for typical drop-out behavior.

Table 8. Example Requirements for 5-V Typical Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8 V to 18 V steady state, 5.5 V to 36 V transients
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	Critical: must have > 250 kHz
Current Consumption at 0-A load	Not critical: < 100 mA acceptable
Synchronization	Yes: 300 kHz supplied by MCU

9.2.2.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is connected to the output through long wires so a 3-Ω resistor is inserted to minimize risks of damage to the part during load shorts. In addition 0.1-µF capacitor is required close to the bias pin.
- FB is connected to the output through a voltage divider in order to create a voltage of 1 V at the FB pin when the output is at 5 V. A 22-pF capacitance is added in parallel with the top feedback resistor in order to improve transient behavior. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performance. See *Layout Guidelines* for more details on the proper layout method.
- SYNC is connected to ground through a pulldown resistor, and an external synchronization signal can be

applied. The pulldown resistor ensures that the pin is not floating when the SYNC pin is not driven by any source.

- EN is connected to VIN so the device operates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.
- FPWM is connected to VIN. This causes the device to operate in FPWM mode. In this mode, the device remains in CCM operation regardless of the output current and is ensured to be within the boundaries set by F_{SW}. To prevent frequency foldback behavior at low duty cycles, provide a 200mA load. The drawback is that the efficiency is not optimized for light loads. See *Device Functional Modes* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to the output in this example. A pullup resistor is necessary. A 100-kΩ is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult *Absolute Maximum Ratings* for the maximum current allowed. In addition, a low pullup resistor could lead to an incorrect logic level due to the value of R_{RESET}. Consult *Electrical Characteristics* for details on the $\overline{\text{RESET}}$ pin.
- Input capacitor selection is detailed in *Input Capacitors*. It is important to connect small high-frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible.
- Output capacitor selection is detailed in *Output Capacitor Selection*.
- Inductor selection is detailed in *Inductor Selection*. In general, a 10-µH inductor is recommended for the nominal adjustable output range of 3.3V to 5V. The inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.2.3 Application Curves

The following characteristics apply only to the circuit of *Adjustable 5-V Output*. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in FPWM mode. The mode is specified under each following graph.

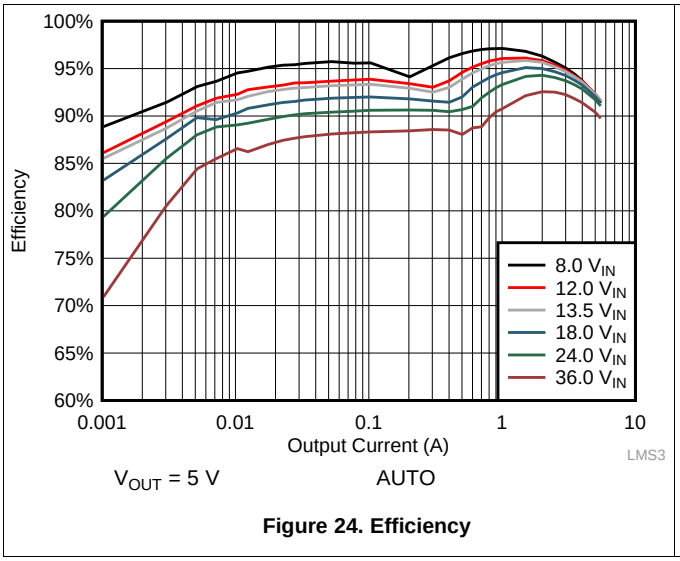


Figure 24. Efficiency

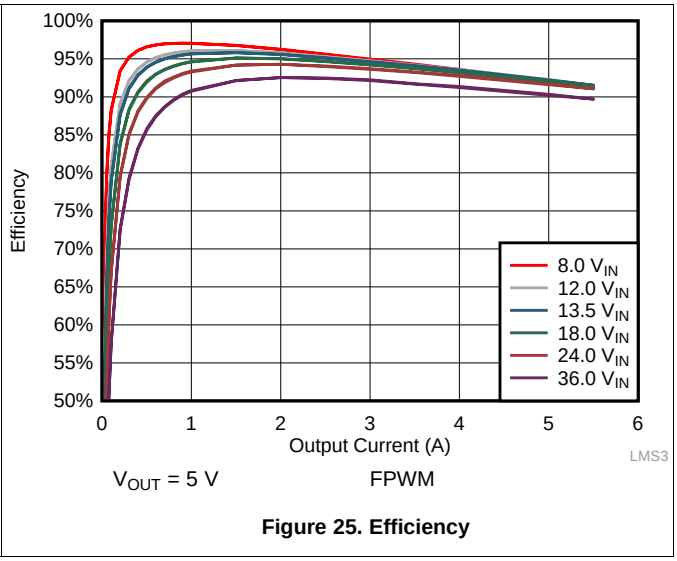


Figure 25. Efficiency

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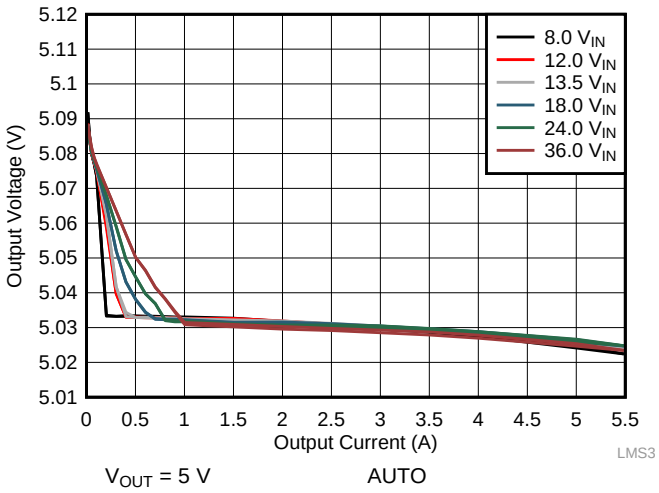


Figure 26. Load and Line Regulation

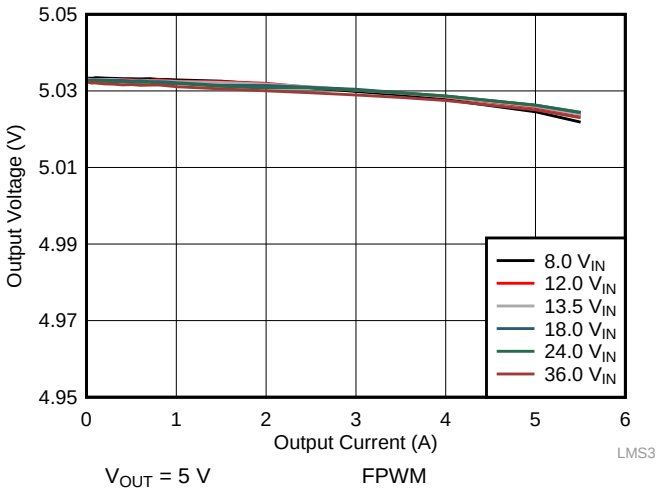


Figure 27. Load and Line Regulation

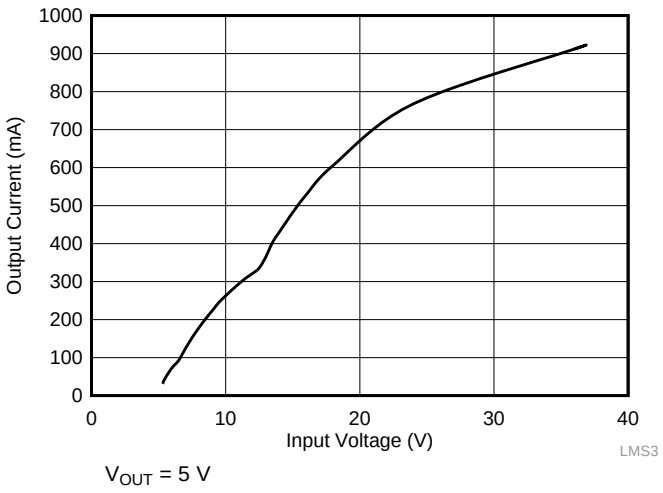


Figure 28. Load Current for PFM-to-PWM Transition

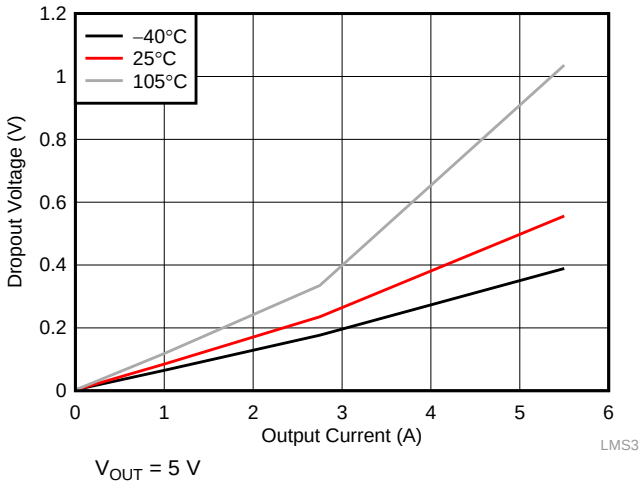


Figure 29. Dropout for –3% Regulation

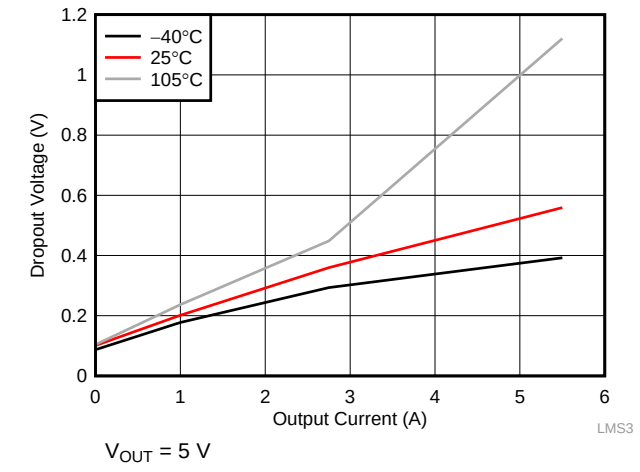


Figure 30. Dropout for ≥ 330 kHz

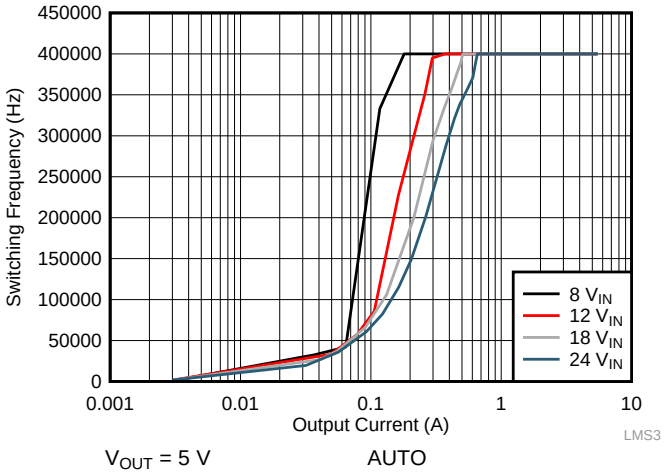
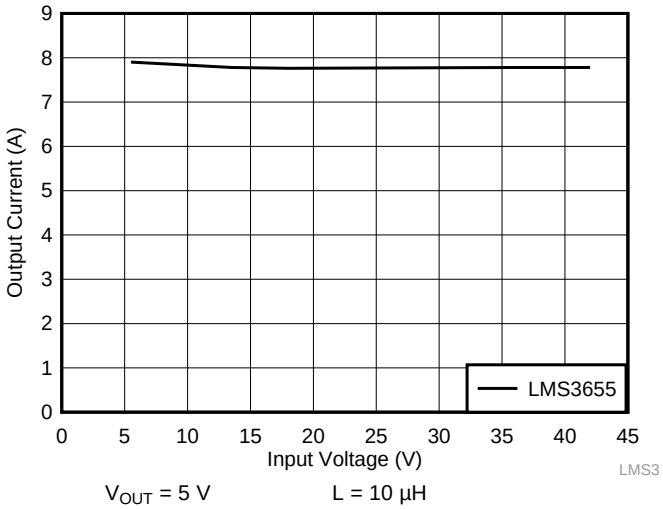


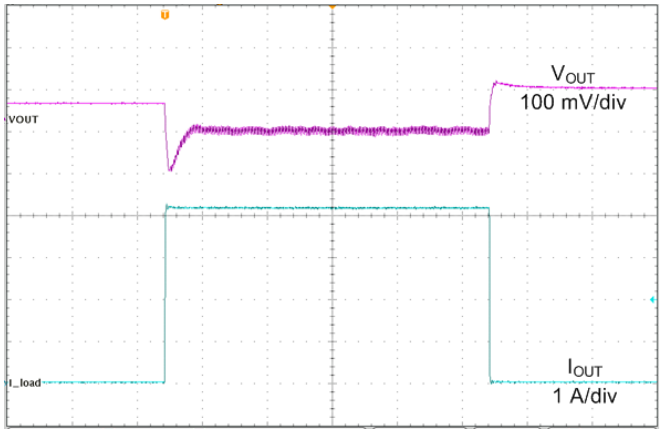
Figure 31. Switching Frequency vs Load Current

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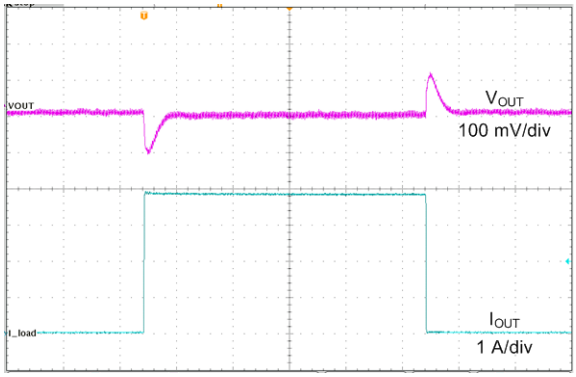
V_{OUT} = 5 V L = 10 µH

Figure 32. Output Current Level Limit Before Overcurrent Protection



AUTO V_{OUT} = 5 V L = 10 µH
C_{OUT} = 170 µF I_{OUT} = 10 mA to 3.5 A $T_R = T_F$ = 1 µs

Figure 33. Load Transients



FPWM V_{OUT} = 5 V L = 10 µH
C_{OUT} = 170 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

Figure 34. Load Transient

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9.2.3 Adjustable 3.3-V Output

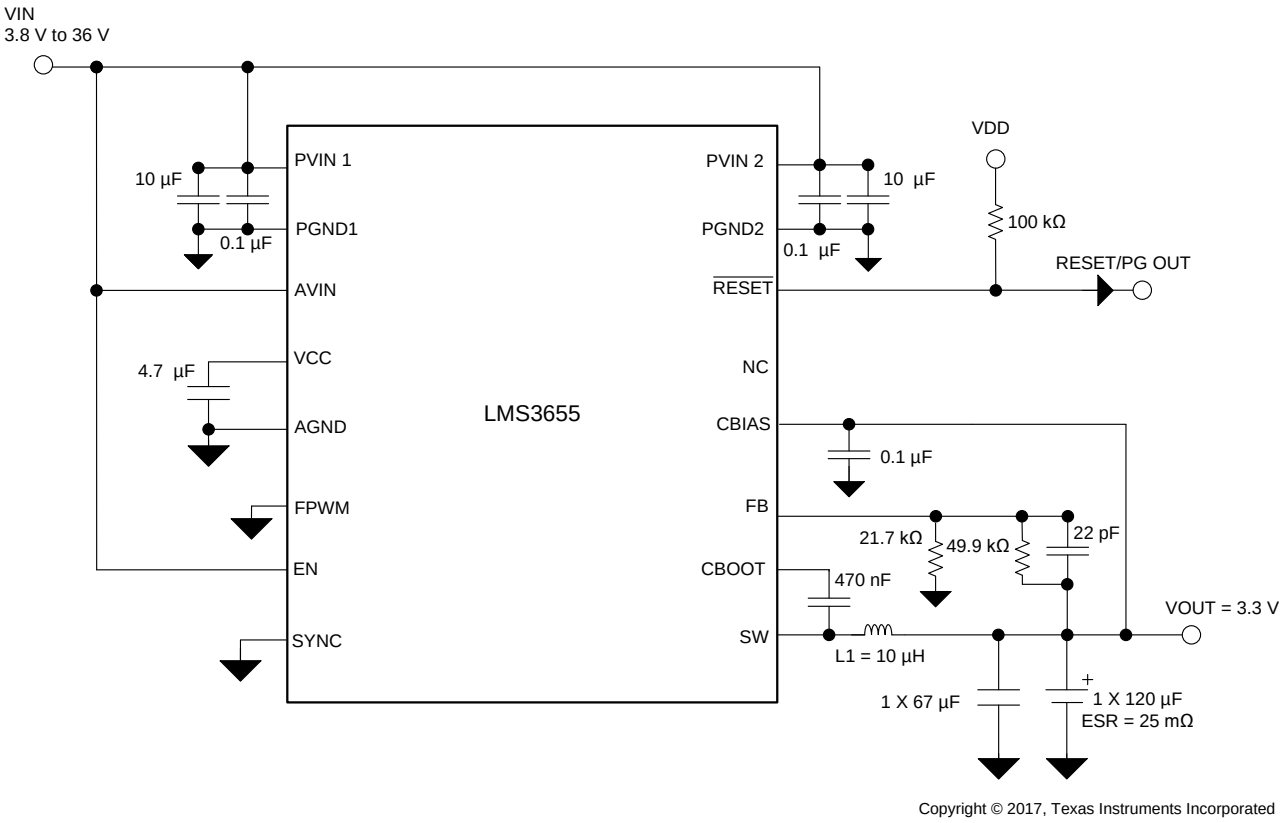


Figure 35. Adjustable 3.3-V, 5.5-A Output Power Supply

9.2.3.1 Design Requirements

Example requirements for a typical 3.3-V application. The input voltages are here for illustration purposes only. See *Electrical Characteristics* for minimum operating input voltage. The minimum input voltage necessary to achieve proper output regulation depends on the components used. See Figure 41 for typical drop-out behavior.

Table 9. Example Requirements for 3.3-V Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady state, 4.0-V to 36-V transients
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	Not critical: Need >330 kHz at high load only
Current Consumption at 0-A load	Critical: Need to ensure low current consumption to reduce battery drain
Synchronization	No

9.2.3.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that the load is close to the output so no bias resistance is necessary. A 0.1-µF capacitor is still recommended close to the bias pin.
- FB is connected to the output through a voltage divider in order to create a voltage of 1 V at the FB pin when the output is at 3.3 V. A 22-pF capacitance is added in parallel with the top feedback resistor in order to improve transient behavior. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performance. See *Layout Guidelines* for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is connected to VIN so the device operates as soon as the input voltage rises above the $V_{IN-OPERATE}$ threshold.

- FPWM is connected to GND. This causes the device to operate in AUTO mode. In this mode, the switching frequency is adjusted at light loads to optimize efficiency. As a result the switching frequency changes with the output current until medium load is reached. The part will then switch at the frequency defined by F_{SW}. See *Device Functional Modes* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensures stable operation of the internal LDO.
- $\overline{\text{RESET}}$ is biased to an external rail in this example. A pullup resistor is necessary. A 100-kΩ pullup resistor is selected for this application and is generally sufficient. The value can be selected to match the needs of the application but must not lead to excessive current into the $\overline{\text{RESET}}$ pin when $\overline{\text{RESET}}$ is in a low state. Consult *Absolute Maximum Ratings* for the maximum current allowed. In addition, a low pullup resistor could lead to an incorrect logic level due to the value of R_{RESET}. Consult *Electrical Characteristics* for details on the $\overline{\text{RESET}}$ pin.
- It is important to connect small high frequency capacitors C_{IN_HF1} and C_{IN_HF2} as close to both inputs PVIN1 and PVIN2 as possible. For the detailed process of choosing input capacitors, refer to *Input Capacitors*.
- Output capacitor selection is detailed in *Output Capacitor Selection*.
- Inductor selection is detailed in *Inductor Selection*. In general, a 10-µH inductor is recommended for the nominal adjustable output range of 3.3V to 5V. The inductance can vary with the output voltage due to ripple and current limit requirements.

9.2.3.3 Application Curves

The following characteristics apply only to the circuit of Figure 35. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C. For the purpose of offering more information to the designer, information for the application with FPWM pin high (FPWM mode) and FPWM pin low (AUTO mode) is included, although the schematic shows the application running specifically in AUTO mode. The mode is specified under each of the following graphs.

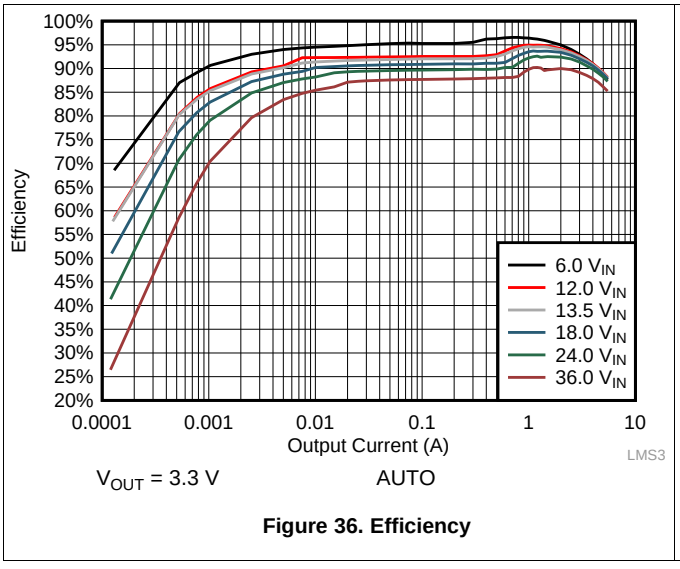


Figure 36. Efficiency

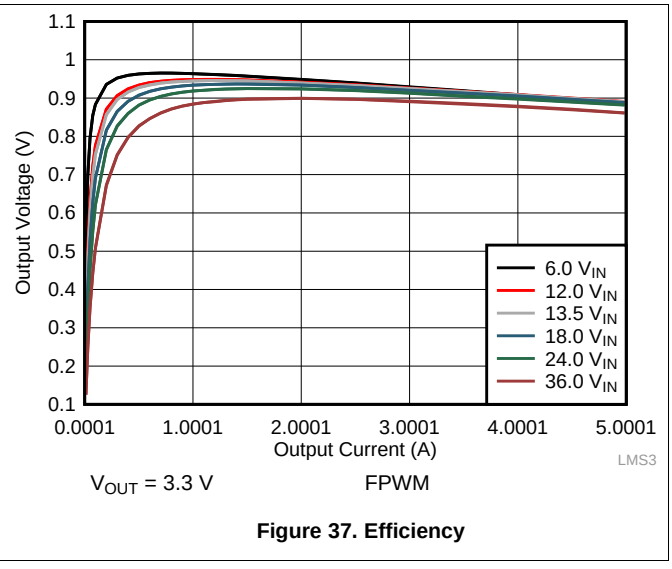


Figure 37. Efficiency

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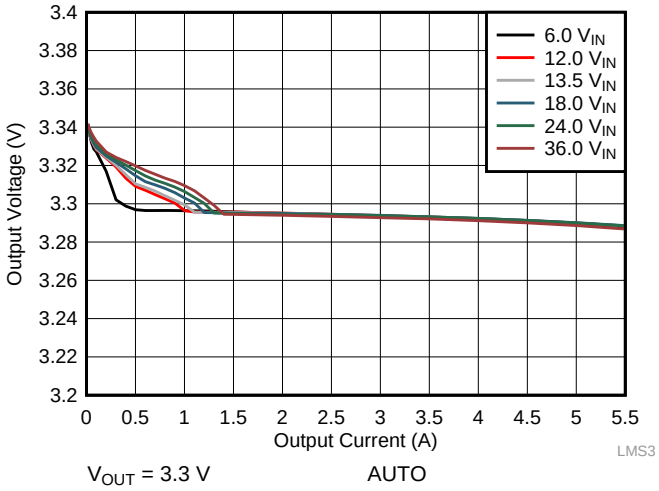


Figure 38. Load and Line Regulation

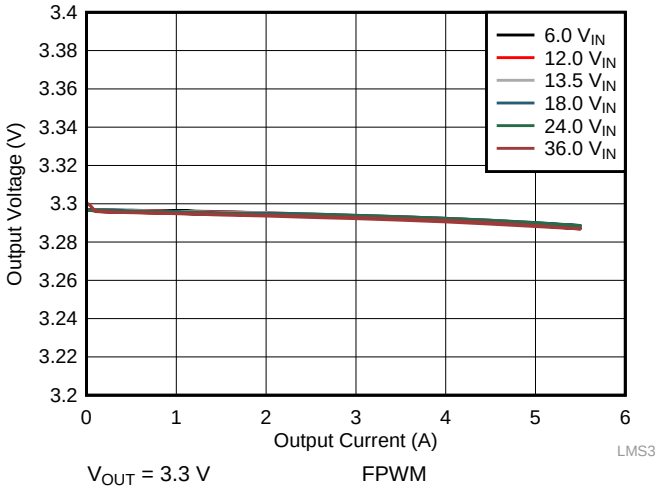


Figure 39. Load and Line Regulation

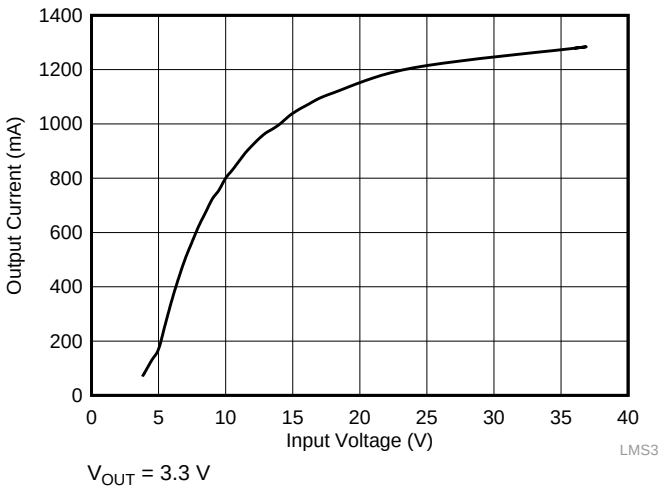


Figure 40. Load Current for PFM-to-PWM Transition

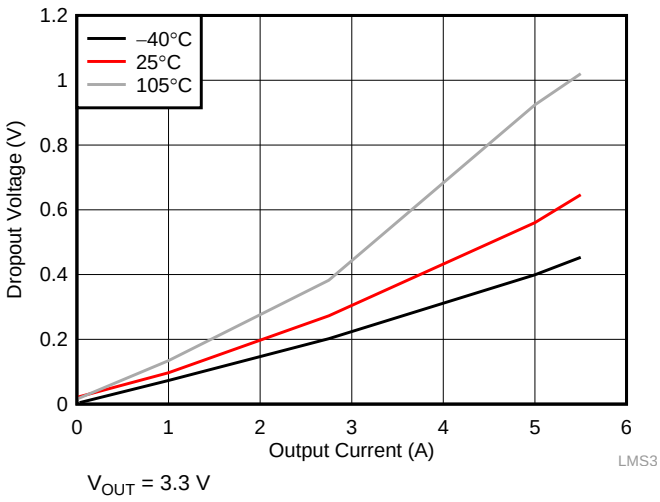


Figure 41. Dropout for –3% Regulation

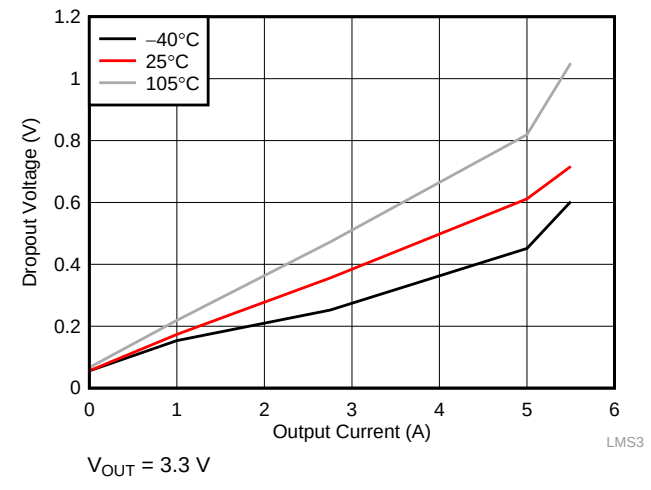


Figure 42. Dropout for ≥ 330 kHz

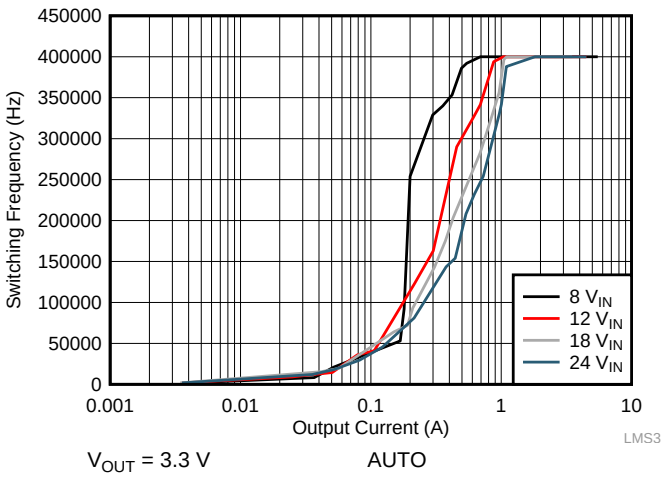
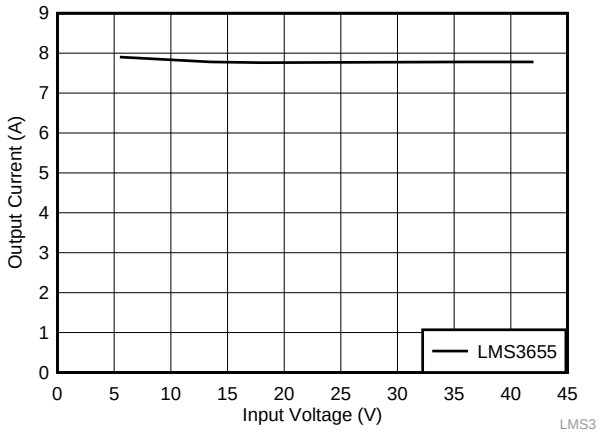


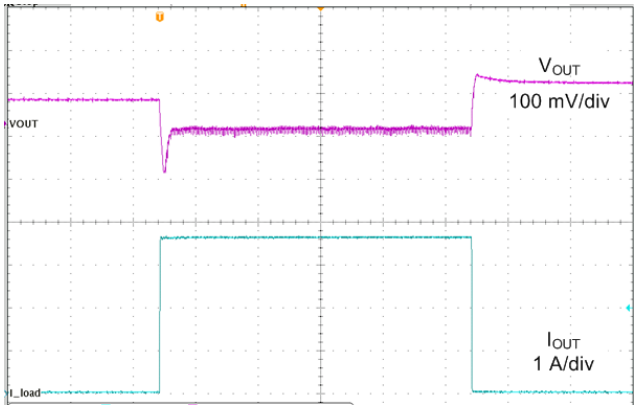
Figure 43. Switching Frequency vs Load Current

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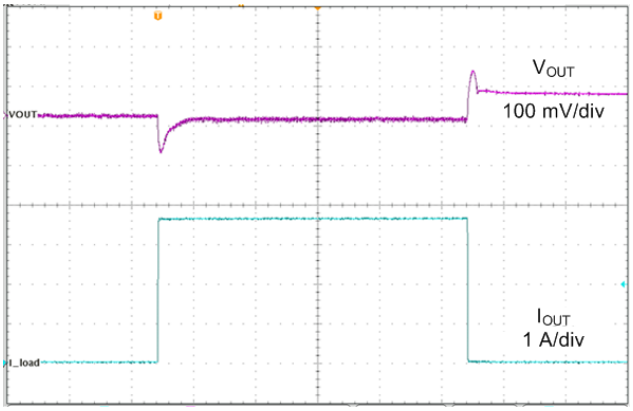
V_{OUT} = 3.3 V L = 10 µH

Figure 44. Output Current Level for Overcurrent Protection Trip



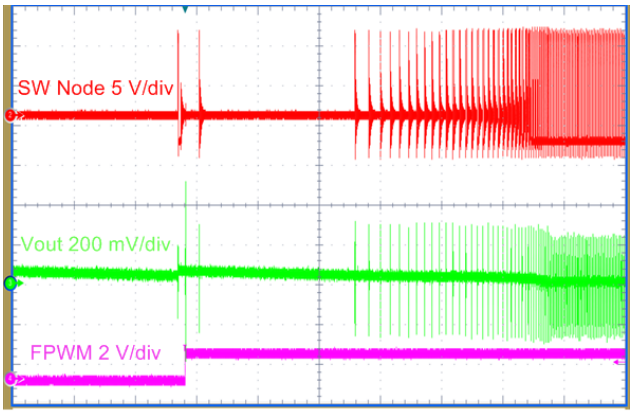
AUTO V_{OUT} = 3.3 V L = 10 µH,
C_{OUT} = 190 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

Figure 45. Load Transient



FPWM V_{OUT} = 3.3 V L = 10 µH,
C_{OUT} = 190 µF I_{OUT} = 0 A to 3.5 A $T_R = T_F$ = 1 µs

Figure 46. Load Transient



V_{OUT} = 3.3 V I_{OUT} = 10 mA

Figure 47. Mode Change Transient AUTO to FPWM mode

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9.2.4 6-V Adjustable Output

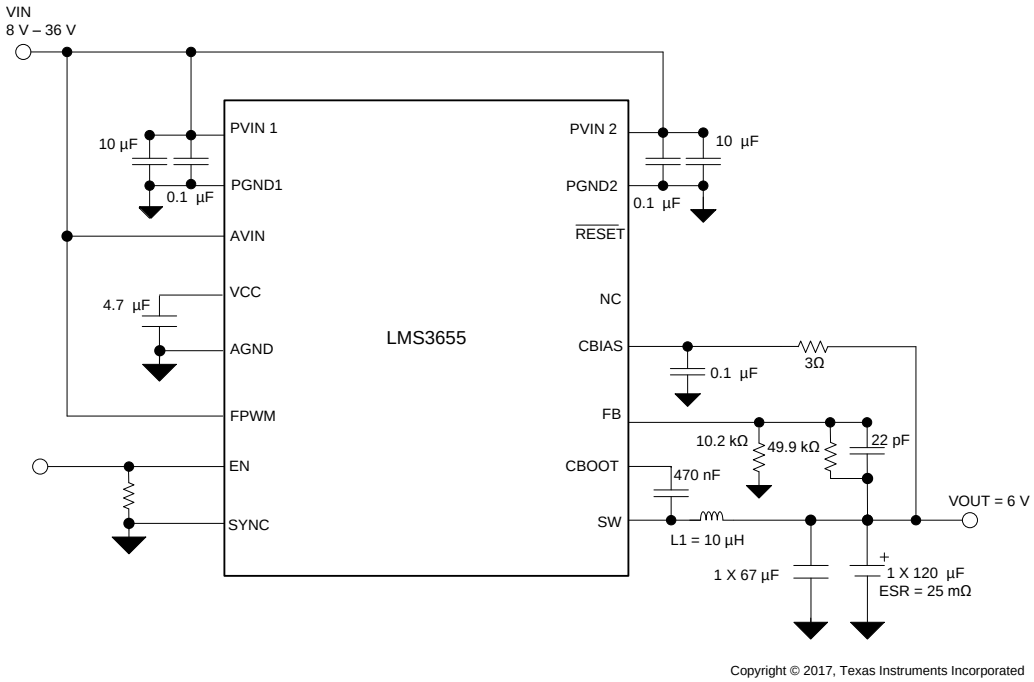


Figure 48. 6-V Output Power Supply

9.2.4.1 Design Requirements

The application highlighted in this section is for a typical 6-V system. The input voltages are here for illustration purposes only. See *Electrical Characteristics* for minimum operating input voltage.

Table 10. Example Requirements for 6-V Application

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	8-V to 18-V steady-state
Output current	0 A to 5.5 A
Switching Frequency at 0-A load	> 250 kHz preferred
Current Consumption at 0-A load	Not critical
Synchronization	No

9.2.4.2 Detailed Design Procedure

- BIAS is connected to the output. This example assumes that inductive short are a risk for this application so a 3-Ω resistor is added between BIAS and the output. A 0.1-µF capacitor is added close the BIAS pin.
- FB is connected to the output through a voltage divider in order to create a voltage of 1 V at the FB pin when the output is at 6 V. A 22-pF capacitance is added in parallel with the top feedback resistor in order to improve transient behavior. BIAS and FB are connected to the output through separate traces. This is important to reduce noise and achieve good performances. See *Layout Guidelines* for more details on the proper layout method.
- SYNC is connected to ground directly as there is no need for this function in this application.
- EN is toggled by an external device (like an MCU for example). A pulldown resistor is placed to ensure the part does not turn on if the external source is not driving the pin (Hi-Z condition).
- FPWM is connected to VIN. This causes the device to operate in FPWM mode. To prevent frequency foldback behavior at low duty cycles, provide a 200mA load. In this mode, the device remains in CCM operation regardless of the output current and is ensured to be within the boundaries set by F_{SW}. The drawback is that the efficiency is not optimized for light loads. See *Device Functional Modes* for more details.
- A 4.7-µF capacitor is connected between VCC and GND close to the VCC pin. This ensure stable operation

of the internal LDO.

- $\overline{\text{RESET}}$ is not used in this example so the pin has been left floating. Other possible connections can be seen in the previous typical applications and in *RESET Flag Output*.
- Power components (input capacitor, output capacitor, and inductor) selection can be found here in *External Components Selection*.

9.2.4.3 Application Curves

The following characteristics apply only to the circuit of Figure 48. *These parameters are not tested and represent typical performance only.* Unless otherwise stated, the following conditions apply: V_{IN} = 12 V, T_A = 25°C.

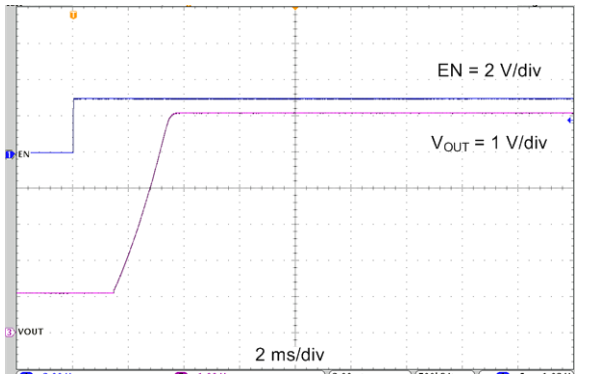


Figure 49. Start-Up Waveform

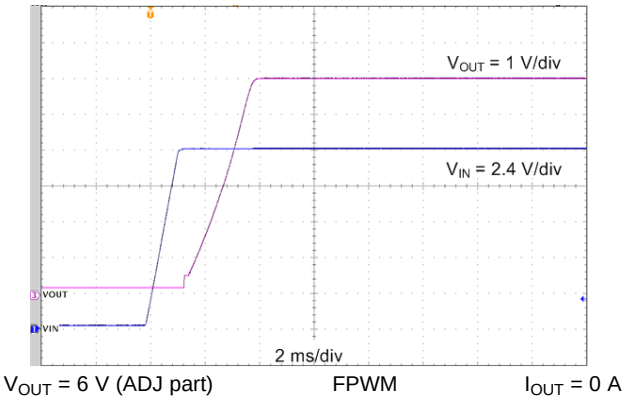


Figure 50. Start-Up Waveform (EN Tied to VIN)

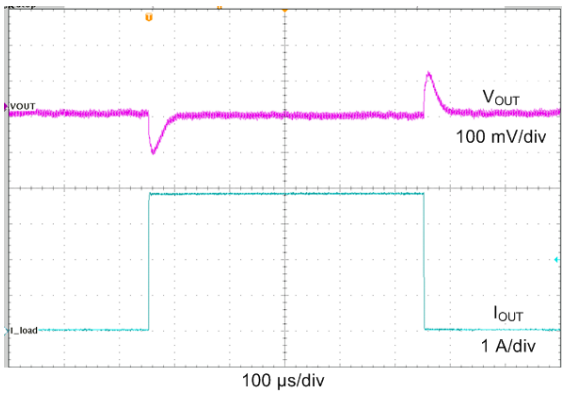


Figure 51. Load Transient

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9.3 Do's and Don't's

- **Don't:** Exceed the *Absolute Maximum Ratings*.
- **Don't:** Exceed the *Recommended Operating Conditions*.
- **Don't:** Allow the EN, FPWM or SYNC input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the thermal data given in the *Thermal Information* table to design your application.
- **Do:** Follow all of the guidelines and/or suggestions found in this data sheet before committing a design to production. TI Application Engineers are ready to help critique designs and PCB layouts to help ensure successful projects.
- **Do:** Refer to the helpful documents found in *Related Documentation*.

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 6:

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (6)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause overvoltage transients at the VIN pin, each time the input supply is cycled on and off. The parasitic resistance causes the voltage at the VIN pin to dip when the load on the regulator is switched on or exhibits a transient. If the regulator is operating close to the minimum input voltage, this dip may cause the device to shut down or reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. *LP3913 Power Management IC for Flash Memory Based Portable Media Players* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* V-I characteristic (thyristor type). The use of a device with this type of characteristic is not recommend. When the TVS fires, the clamping voltage drops to a very low value. If this holding voltage is less than the output voltage of the regulator, the output capacitors are discharged through the regulator back to the input. This uncontrolled current flow could damage the regulator.

11 Layout

11.1 Layout Guidelines

The PCB layout of a DC-DC converter is critical for optimal performance of the application. For a buck converter the input loop formed by the input capacitors and power grounds are very critical. The input loop carries fast transient currents that cause larger transient voltages when reacting with a parasitic loop inductance. The IC uses two input loops in parallel IN1 and IN2 as shown in Figure 52 that cuts the parasitic input inductance in half. To get the minimum input loop area two small high frequency capacitors CIN1 and CIN2 are placed as close as possible.

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Layout Guidelines (continued)

To further reduce inductance, an input current return path should be placed underneath the loops IN1 and IN2. The closest metal plane is MID1 Layer2, and there is a solid copper plane placed right under the IN1 and IN2 loop the parasitic loop inductance is minimized. Connecting this MID1 Layer2 plane to GND provides a nice bridge connection between GND1 and GND2 as well. Minimizing the parasitic input loop inductance will minimize switch node ringing and EMI.

The output current loop can be optimized as well by using two ceramic output caps COUT1 and COUT2, one on each side. They form two parallel ground return paths OUT1 from COUT1 back to the low-side FET PGND1 pins 5, 6, 7, 8, and a second symmetric ground return path OUT2 from COUT2 back to low-side FET PGND2 pins 10, 11, 12, and 13. Having two parallel ground return paths yield reduced ground bouncing and reduced sensitivity of surrounding circuits.

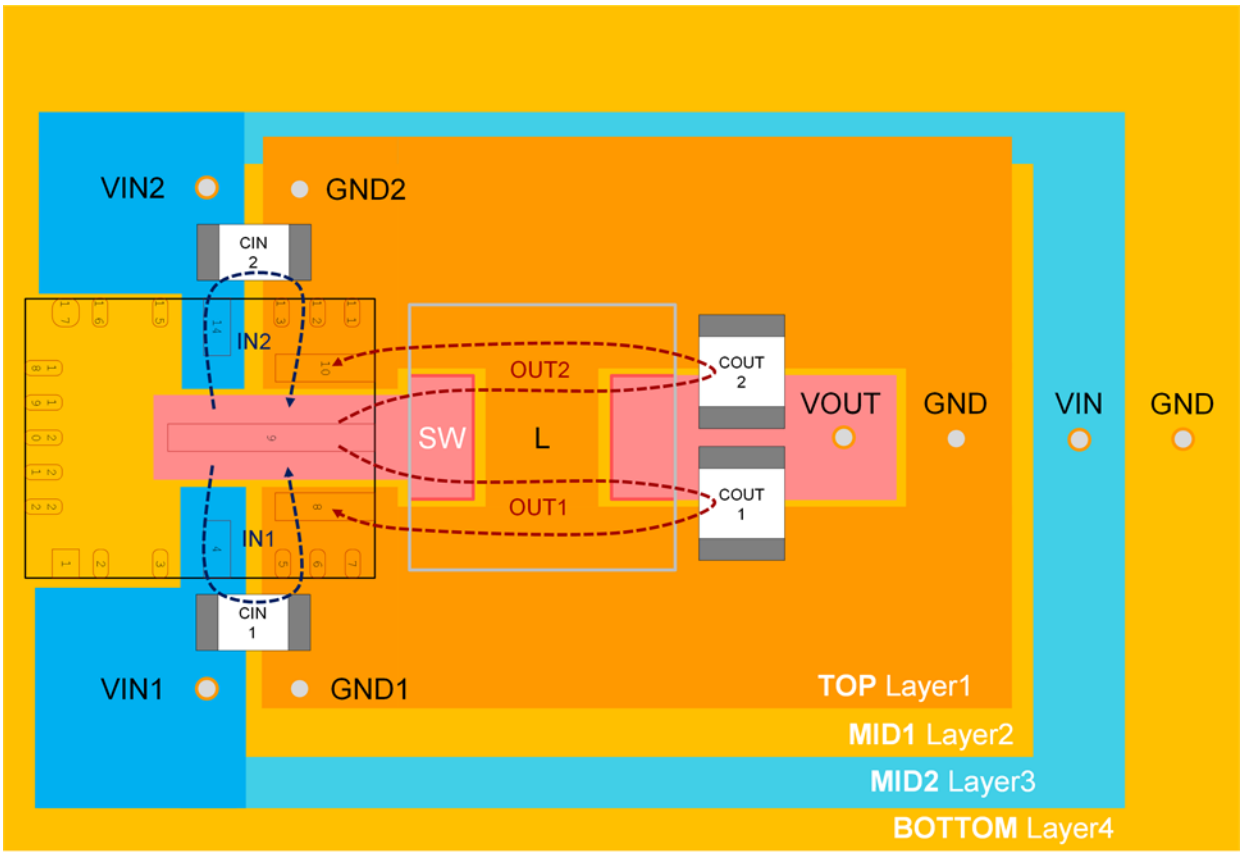


Figure 52. Layout of the Power Components and Current Flow

Providing adequate thermal paths to dissipate heat is critical for operation at full current. The recommended method for heat dissipation is to use large solid 2-oz copper planes well connected to the power pins VIN1, VIN2, GND1, and GND2 which transfer the heat out of the IC over the TOP Layer1 copper planes. It is important to leave the TOP Layer1 copper planes as unbroken as possible so that heat is not trapped near the IC. The heat flow can be further optimized by thermally connecting the TOP Layer1 plane to large BOTTOM Layer 4 2-oz copper planes with vias. MID2 Layer3 is then open for all other signal routing. A fully filled or solid BOTTOM Layer4 ground plane without any interruptions or ground splitting is beneficial for EMI as well. Most important for low EMI is to use the smallest possible switch node copper area. The switch node including the C_{BOOT} cap has the largest dV/dt signal causing common-mode noise coupling. Using any kind of grounded shield around the switch node *shortens* and reduces this e-field.

All these DC-DC converter descriptions can be transformed into layout guidelines:

1. Place two 0.047-µF, 50-V high frequency input capacitors C_{IN1} and C_{IN2} as close as possible to the VIN1, VIN2, PGND1, PGND2 pins to minimize switch node ringing.

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Layout Guidelines (continued)

2. Place bypass capacitors for VCC and BIAS close to their respective pins. Make sure AGND pin *sees* the C_{VCC} and C_{BIAS} capacitors first before a connection to PGND.
3. Place C_{BOOT} capacitor with smallest parasitic loop. Shielding the C_{BOOT} capacitor and switch node has the biggest impact to reduce common-mode noise. Placing a small R_{BOOT} resistor (less than 3 Ω is recommended) in series to C_{BOOT} slows down the dV/dt of the switch node and reduce EMI.
4. Place the feedback resistor divider as close as possible to the FB pin and to AGND pin of the device. Use a dedicated feedback trace, and route away from switch node and C_{BOOT} capacitor to avoid any cross coupling into sensitive analog feedback.
5. Use a dedicated BIAS trace to avoid noise into feedback trace.
6. Use a 3-Ω to 5-Ω resistor between the output and BIAS if the load is far from the output of the converter or inductive shorts on the output are possible.
7. Use well connected large 2-oz. TOP and BOTTOM copper planes for all power pins VIN1/2 and PGND1/2.
8. Minimize switch node and C_{BOOT} area for lowest EMI common mode noise.
9. Place input and output wires on the same side of the PCB using an EMI filter and away from the switch node for lowest EMI.

The resources in *Device and Documentation Support* provide additional important guidelines.

11.2 Layout Example

This example layout is the one used in the LMS3655 EVM. It shows the C_{IN} and C_{IN_HF} capacitors placed symmetrically on either side of the device.

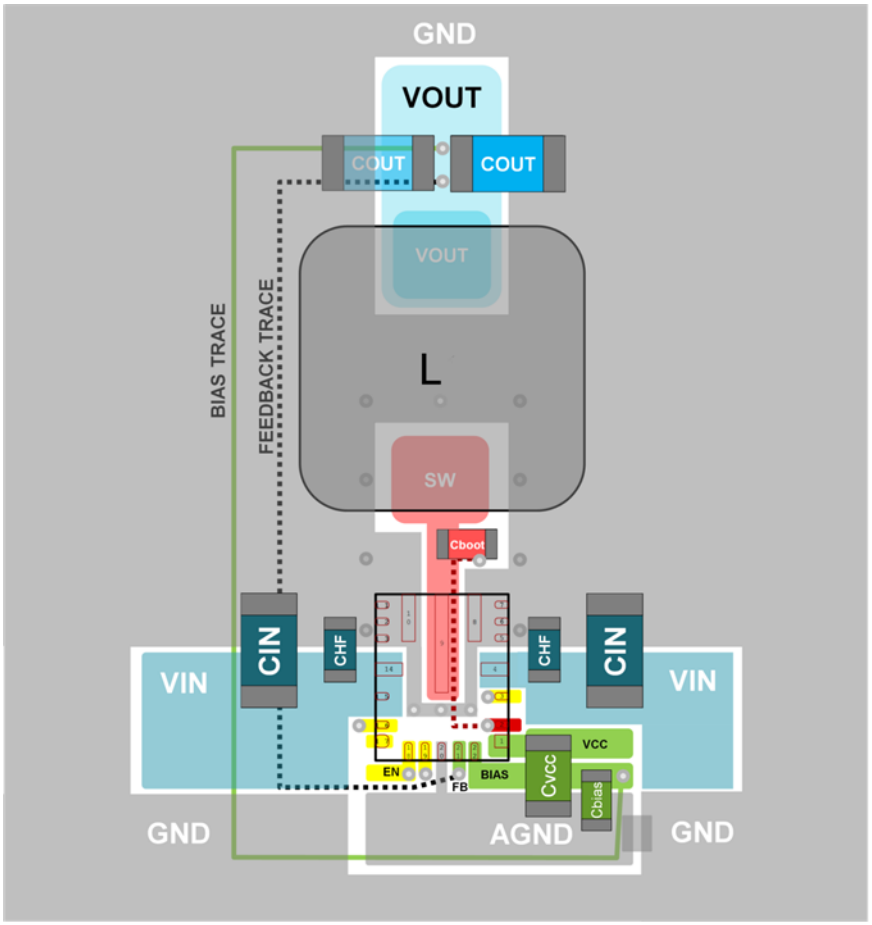


Figure 53. Recommended Layout for LMS3655

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following:

- *Optimizing Transient Response of Internally Compensated DC-DC Converters With Feedforward Capacitor* (SLVA289)
- *Output Ripple Voltage for Buck Switching Regulator* (SLVA630)
- *AN-1149 Layout Guidelines for Switching Power Supplies* (SNVA021)
- *AN-1229 Simple Switcher® PCB Layout Guidelines* (SNVA054)
- *Constructing Your Power Supply- Layout Considerations* (SLUP230)
- *AN-2020 Thermal Design By Insight, Not Hindsight* (SNVA419)
- *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

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WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMS3655MMRNLR	PREVIEW	VQFN-HR	RNL	22	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	LM3655M	
LMS3655MMRNLT	PREVIEW	VQFN-HR	RNL	22	250	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	LM3655M	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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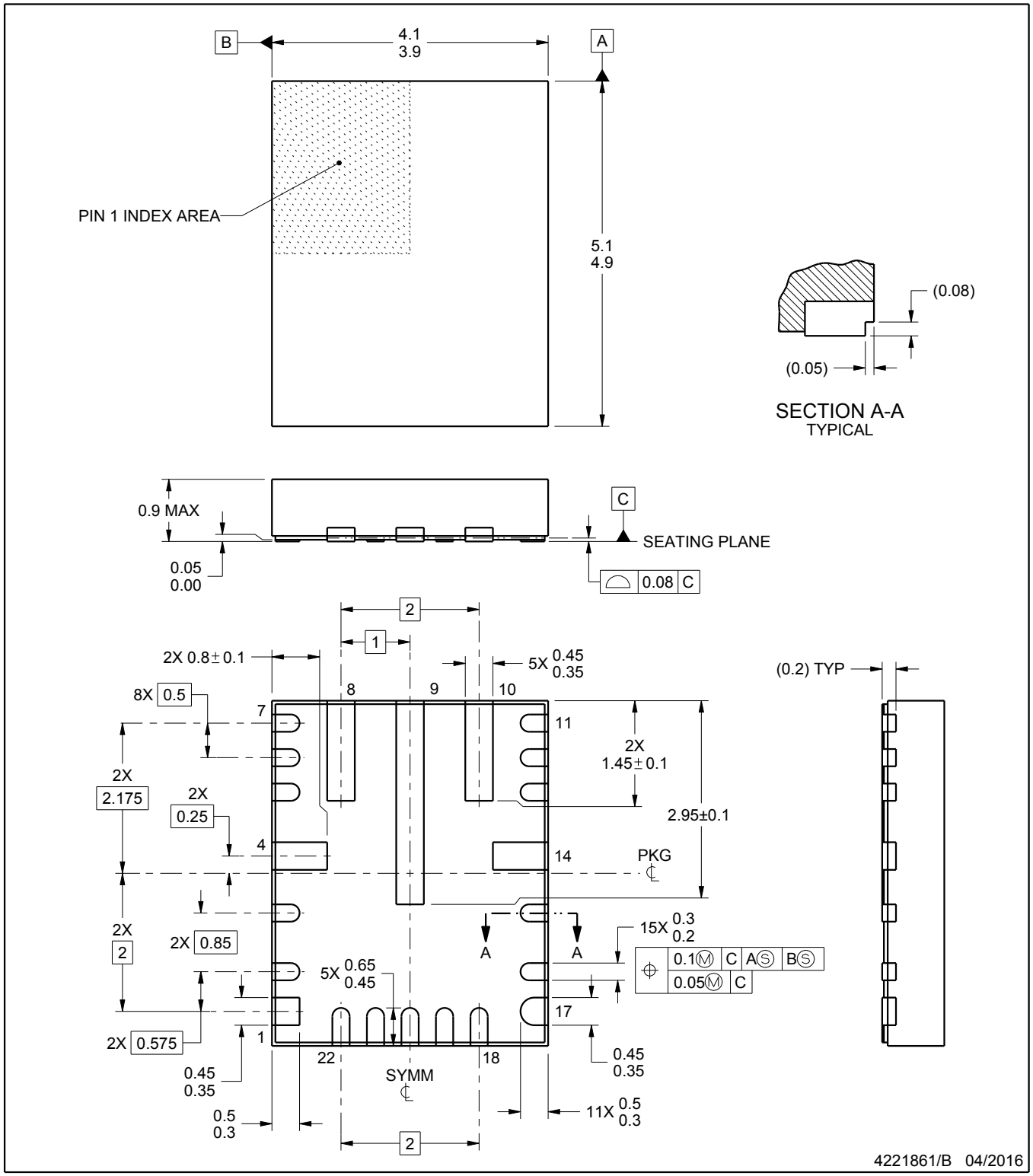
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RNL0022A

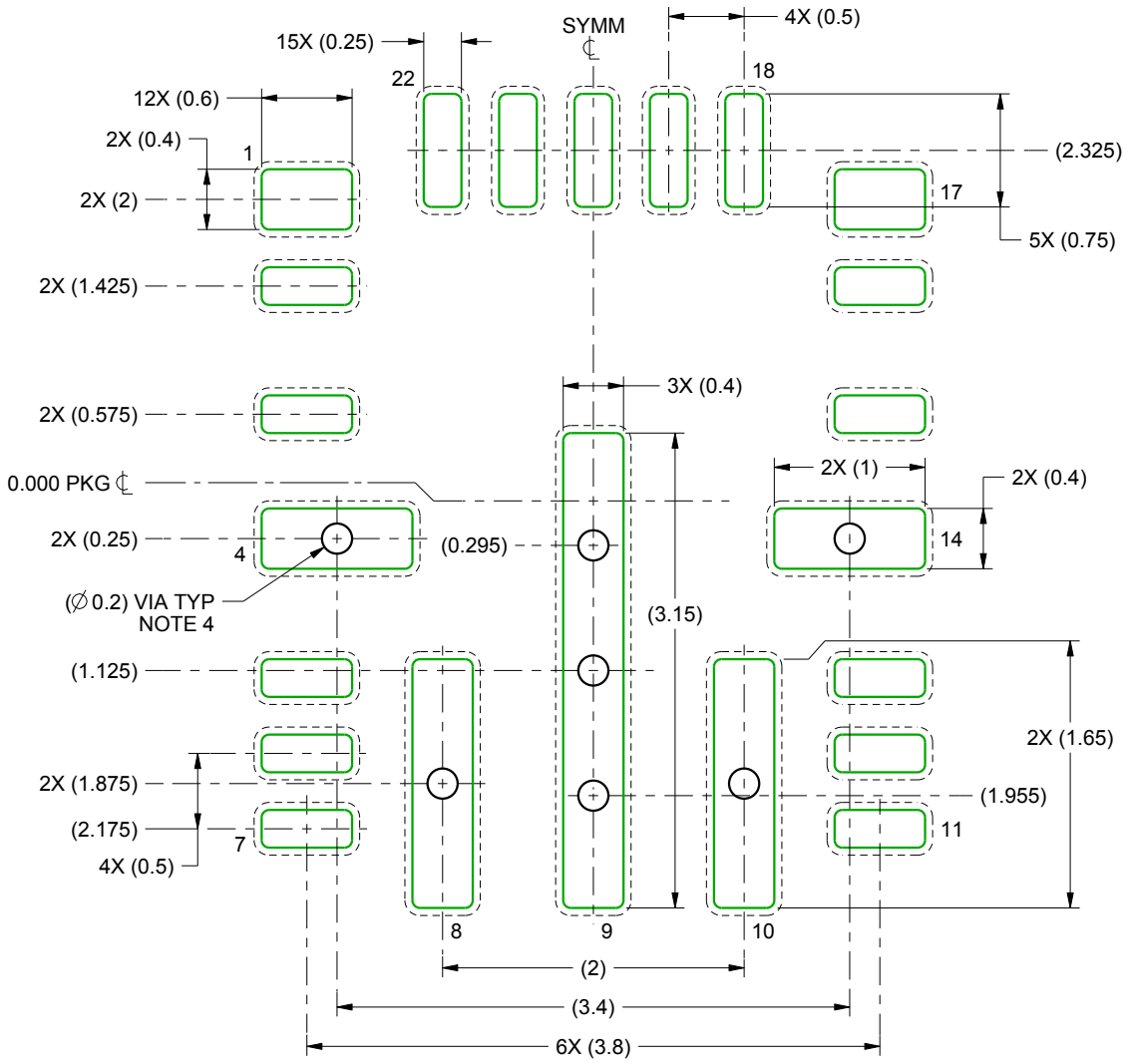
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

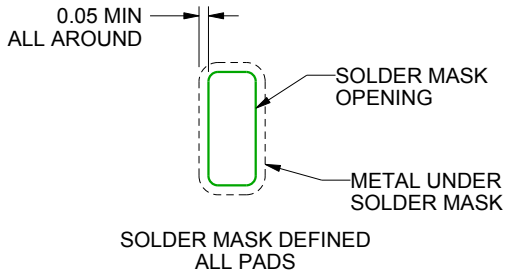


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DEFINED
ALL PADS

4221861/B 04/2016

NOTES: (continued)

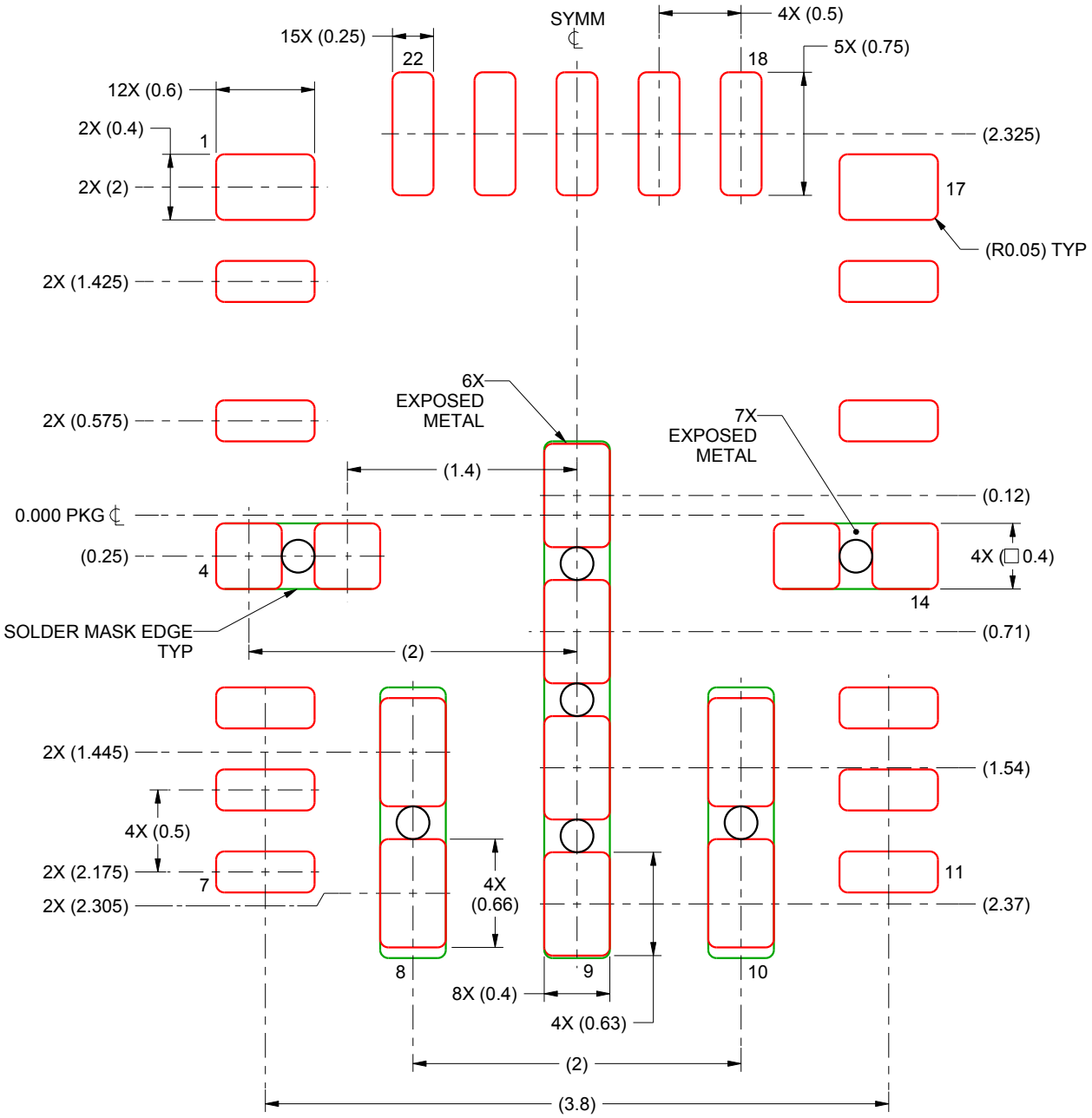
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RNL0022A

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PADS 4,8,9,10 & 14
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221861/B 04/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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